Si12T

Low power 14 channels Capacitive touch sensor

1. Introduction

Si12T is a 12-channel capacitive sensor with automatic sensitivity calibration function, its operating voltage range is 1.8~5.0V.

Si12T can set idle mode to save power consumption. At this time, the power consumption current is 3.5 μA @3.3 V.

Si12T has two special functions: the embedded power button function on channel 1 can be applied to mobile. The second function is synchronization available for multiple chips. In addition, the chip has a touch pause detection function through pin SCT with the cooperation of SI512/522/523, the chance of false triggering is greatly reduced, which is very suitable for applications such as smart door locks.

The I2C serial interface can detect the results of touch sensing, and the touch intensity can be detected, divided into 3 results: low, medium and high.

Contents

2. Features

- Power-on reset
- 12-channel capacitive sensor with automatic calibration sensitivity function
- Optional output mode
- External touch pause detection
- 8 kinds of sensitivity are independently adjustable
- Adjustable internal frequency with external resister
- Support I2C serial interface
- Embedded high frequency noise elimination circuit
- Power consumption current 69.7 μA (@3.3V) in operating mode
- Power consumption current 3.5 μA (@3.3V) in sleep mode

3. Chip block diagram

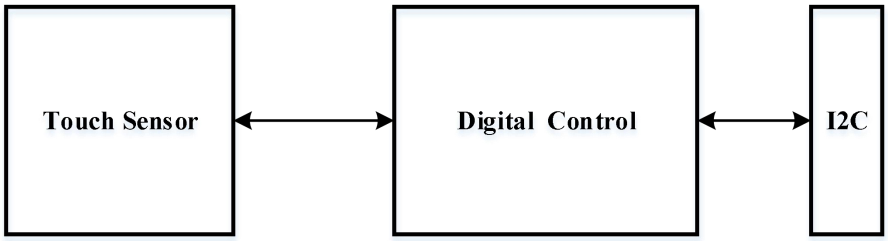


Figure3.1 Simplified block diagram of Si12T

4. Applications

- Mobile applications (mobile phone/PDA/PMP, etc)
- Membrane switch
- Control panel, keyboard
- Door lock application
- Touch screen application

5. Pin definition

The schematic diagram of the Si12T pin package is as follows：

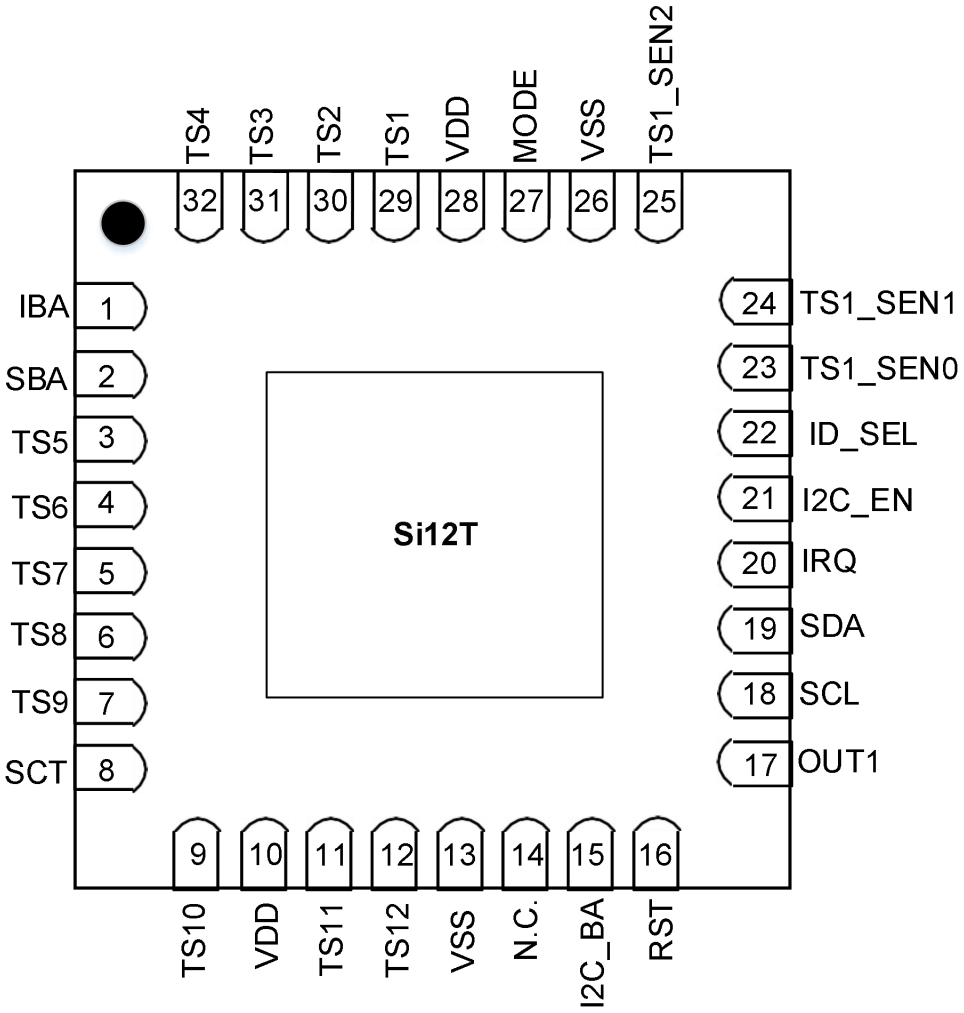


figure5.1 Schematic diagram of Si12T pin (5x5 mm QFN32)

6. Pin Description

Number	Name	I/O	Description	Protection
1	IBA	analog input	Internal bias adjustment	VDD/GND
2	SBA	analog input	Internal bias adjustment in sleep mode	VDD/GND
3	TS5	analog input	Touch sensor 5 input	VDD/GND
4	TS6	analog input	Touch sensor 6 input	VDD/GND
5	TS7	analog input	Touch sensor 7 input	VDD/GND
6	TS8	analog input	Touch sensor 8 input	VDD/GND
7	TS9	analog input	Touch sensor 9 input	VDD/GND
8	SCT	digital input	Touch detection suspension control (high level suspension, 0, or floating)	VDD/GND
9	TS10	analog input	Touch sensor 10 input	VDD/GND
10	VDD	digital input	-	VDD/GND
11	TS11	analog input	Touch sensor 11 input	VDD/GND
12	TS12	analog input	Touch sensor 12 input	VDD/GND
13	VSS	ground	-	VDD
14	N.C.	-	Floating	-
15	I2C_BA	analog input	Internal I2C clock adjustment	VDD/GND

16	RST	digital input	System reset（high level reset）	VDD/GND
17	OUT1	digital output	Channel1output（open drain）	VDD/GND
18	SCL	digital input	I2C clock	VDD/GND
19	SDA	digital input /output	I2C data	VDD/GND
20	IRQ	digital output	Interrupt output（open drain）	VDD/GND
21	I2C_EN	digital input	I2C enable（low valid）	VDD/GND
22	ID_SEL	digital input	I2C device address select	VDD/GND
23	TS1_SEN0	digital input	TS1 sensitivity control bit 0	VDD/GND
24	TS1_SEN1	digital input	TS1 sensitivity control bit 1	VDD/GND
25	TS1_SEN2	digital input	TS1 sensitivity control bit 2	VDD/GND
26	VSS	digital input	-	VDD/GND
27	MODE	digital input /output	Output mode control （ high single channel output， low multi-channeloutput）	VDD/GND
28	VDD	power	1.8V~5.0V	GND
29	TS1	analog input	Touch sensor 1 input	VDD/GND
30	TS2	analog input	Touch sensor 2 input	VDD/GND
31	TS3	analog input	Touch sensor 3 input	VDD/GND
32	TS4	analog input	Touch sensor 4 input	VDD/GND

7. Rating value

Battery supply power	5.0 V
The maximum voltage on any of the pin	VDD+0.3
The maximum current on any of the PAD	100 mA
Dissipated power	800 mW
Storage temperature	-50 ~150 ℃
Operating temperature	-20 ~ 75 ℃
Junction temperature	150 ℃

8. ESD and Latch-up features

8.1 ESD feature

Mode	Polarity	Max	Min
H.B.M	Pos/Neg	5000V	VDD
		5000V	VSS
		5000V	P to P
M.M	Pos/Neg	350V	VDD
		350V	VSS
		350V	P to P
C.D.M	-	800V	DIRECT

8.2 Latch-up features

Mode	Polarity	Max	Reference
I Test	Positive	100mA	25 mA
	Negative	100mA	
V supply over 5.0V	Positive	8.25V	1.0V

9. Electrical features

V_{DD} = 3.3 V，typical system frequency（unless specifically labeled ），T_A = 25℃

Item	Symbol	Test condition		Min	Typical	Max	Unit
Operating voltage	V_{DD}			1.8	3.3	5.0	V
Power consumption current[1]	I_{DD}	V_{DD} = 3.3 V R_B = 510 K R_SB=0		-	67.68	-	μA
		V_{DD} = 5.0 V R_B = 510 K R_SB=0		-	145	-	
		Non-Sensing time	V_{DD} = 3.3 V R_B = 510 K R_SB=6 M	-	3.48	-	
			VDD = 5.0 V RB = 510 K R_SB=6 M	--	10.44	-	
	I_{DD_I2C}	V_{DD} = 3.3 V R_B = 510 K R_{I2C}=20 k		-	0.67	-	mA
		V_{DD} = 5.0 V R_B = 510 K R_{I2C}=20 k		-	1.1	-	
		IDD_I2C Disable		-	-	0.04	nA
Input induction capacitance range [2]	C_S			-	10	110	pF
Input induction resistance range	R_S			-	200	2000	Ω
Minimum detectable	ΔC	C_S = 10 pF, C_{DEG} = 200 pF （I2C default sensitivity）		0.2	-	-	pF

capacitance						
Output impedance(drain opening)	Z_O	ΔC > 0.2 pF(Inaccuracy measurement), C_S = 10 pF, （I2C default sensitivity）	-	71	-	Ω
		ΔC < 0.2 pF(Inaccuracy measurement), C_S = 10 pF, （I2C default sensitivity）	-	41.25 M	-	
The time of self-examination after reset	T_{CAL}	V_{DD} = 3.3 V R_B = 510 K	-	120	-	ms
		V_{DD} = 5.0 V R_B = 510 K	-	98	-	
Recommended offset range [3]	R_B	V_{DD} = 3.3 V	100	510	1500	KΩ
		V_{DD} = 5.0 V	100	510	1500	
Maximum offset capacitance	C_{B_MAX}		-	820	1500	pF
Recommended synchronous resistance range	R_{SYNC}		0.91	2	20	MΩ

NOTE： [1] When SCL frequency is 500 kHz；

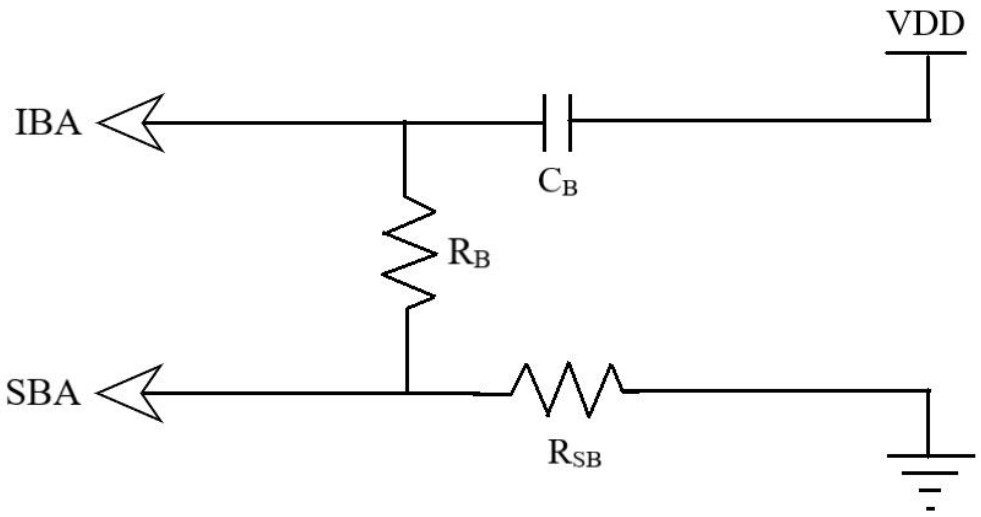
[2] When C_S is lower，sensitivity is higher；

*When using the 3t PC overlay and 10 mm * 7 mm touch graphics, the recommended Cs value is 10 pF；*

[3] Lower rates for R_B is recommended in noise.

10. Si12T implementation

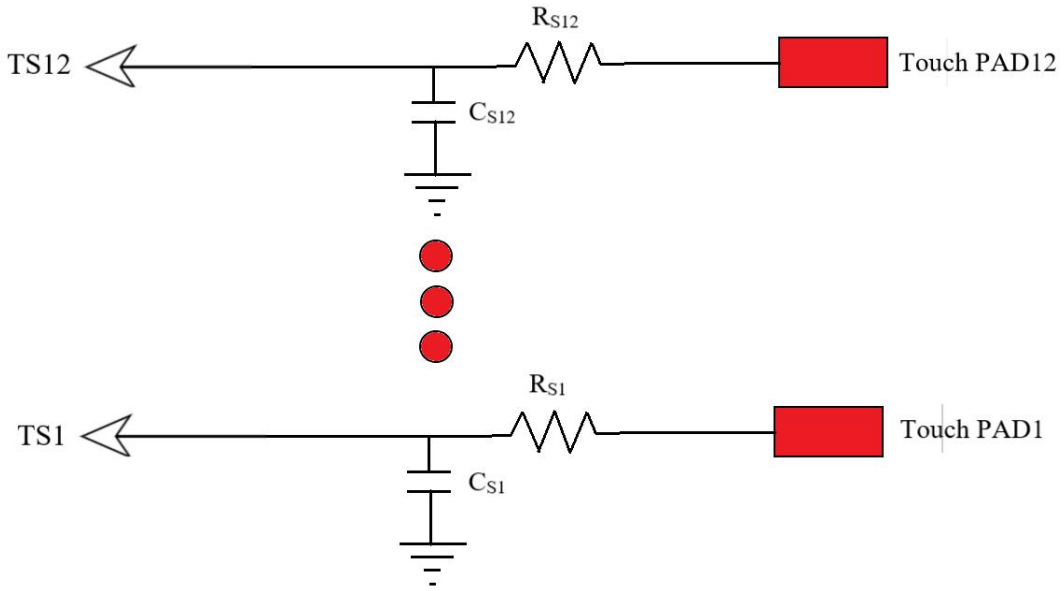
10.1 IBA and SBA implementation



IBA is connected to resistors to determine the oscillator and internal bias current, so it can be adjusted by R_B sensing frequency, internal clock frequency, and power dissipation current. Voltage fluctuations on the IBA can cause severe internal error, so it is recommended to connect C_B to VDD (non-GND). (A typical value for C_B is 820 pF, the Largest value is 1.5 nF.）

When the Si12T is operating in the sleep mode, the R_{SB} should be connected as shown above to save power current. In this case, the power dissipation depends on the sum of the serial resistors, and the response time may be longer.

10.2 TS implementation



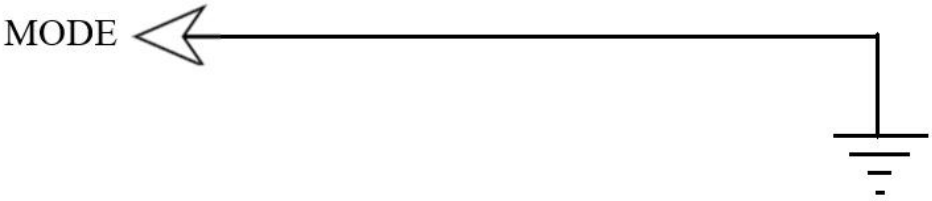
Si12T has a total of 8 sensitivity, which can be obtained by the I2C interface control internal register. Parallel capacitance Cs1~Cs12 is used for sensitivity of TS1~ TS12. As the Cs value decreases, the touch of each channel in the inside is determined to separate each other, so using a Si12T can design 12 channels to touch keyboard applications without coupling problems. The Rs is a serial connection resistance, which is used to avoid the failure of external electric surge and the problem caused by ESD, and the Rs proposal from 200 to 1 kΩ. The size and shape of the PAD may affect sensitivity, when the size of the pad is about 10 mm * 7 mm, the sensitivity will be the best. It is recommended that the TS1~ TS12 to the touch pad's connection line be as short as possible, in case of abnormal touch detection caused by the connection line. The unused Cs tube must be grounded to prevent the failure of the floating Cs to be unpredictable.

10.3 MODE implementation

10.3.1 Output mode select

This pin is assigned to selecting output mode to determine Si12T works in a single or multiple touch detection mode and through the following circuit implementation.

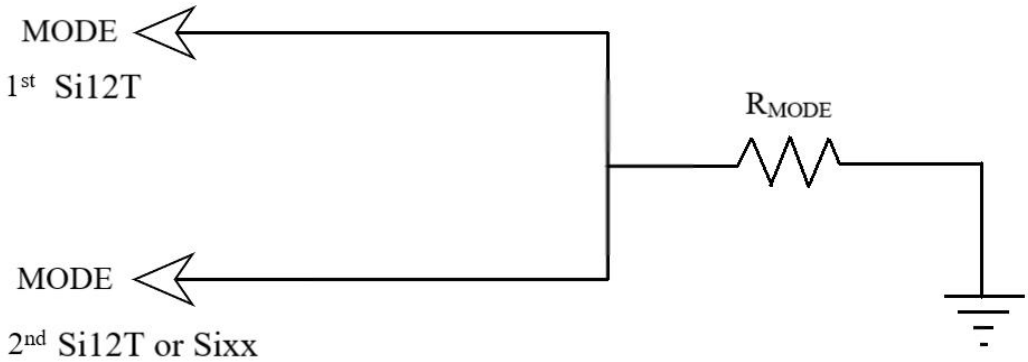
Single Output Mode Implementation



Multi Output Mode Implementation

10.3.2 Multiple chips application

With the MODE function of this pin, two or more Si12T chips can work on one application at the same time. MODE pulses prevent more than two induction signals from interfering with each other. R_{MODE} is the pull-down resistor of the MODE pin. If the value of R_{MODE} is too large, the falling pulse of MODE will be delayed, while if the value of R_{MODE} is small, the rising pulse will be delayed. The typical value of RMODE is 2M2. The synchronization pin should be implemented in the following way. The Si12T can also be used with other Sixx series by using the MODE feature, but the Si12T's multiple output mode can only be used in this configuration. The external circuit is recommended below.



10.4 TS1_SEN0, TS1_SEN1, TS1_SEN2 implenentation

TS1_SEN0,1 and 2 only controls the sensitivity of TS1, and if TS_SEN[2:0] = 011, the sensitivity of channel 1 is controlled by the register as well as other channels, but if not equal,the sensitivity should be fixed in the table below.

TS1_SEN<2:0>	Channel 1 sensitivity(@Cs = 0 pF)		
	low	medium	high
011	Determines the register value (refer to the I2C register Description)		
000	0.35%	0.50%	0.65%
001	0.50%	0.70%	0.90%
010	0.60%	0.90%	1.20%
100	1.05%	1.50%	2.00%
101	1.40%	2.05%	2.65%
110	1.80%	2.55%	3.30%
111	2.45%	3.55%	4.65%

10.5 RST implementation

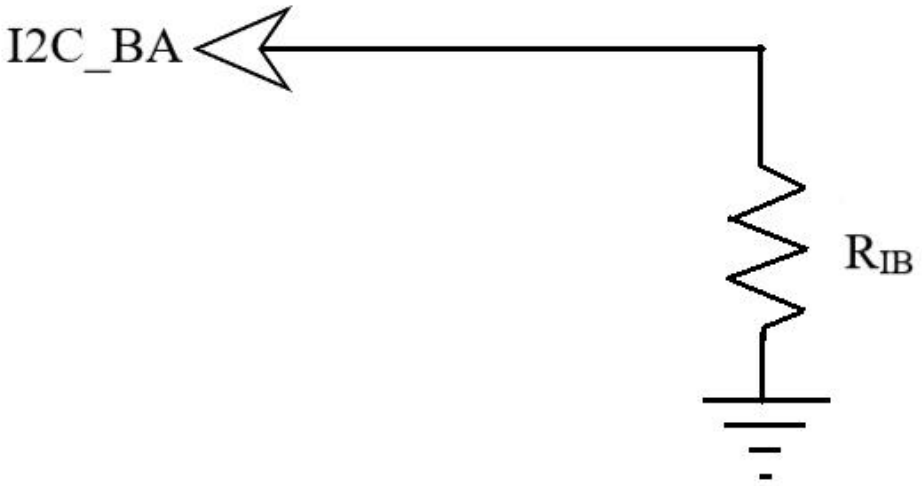
Control chip reset, high level reset。

10.6 SCT implementation

Si12T work normally when SCT is floating or low, while touching will be paused when SCT is high.

11. I2C interface

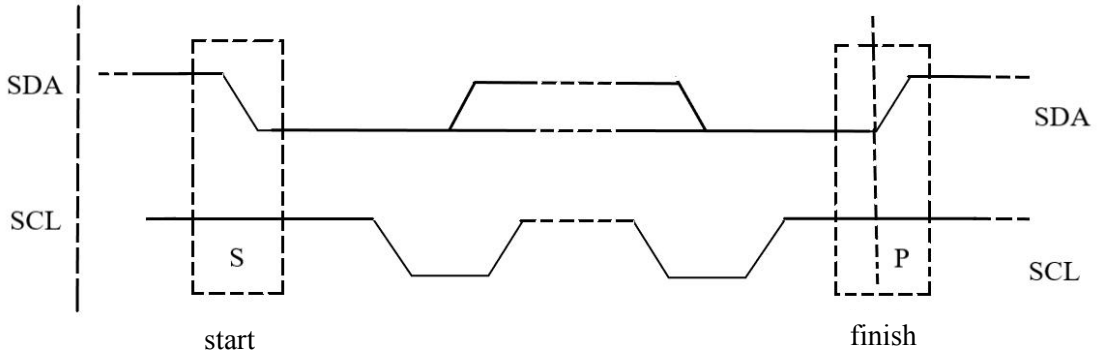
11.1 I2C_BA implementation



The R_{IB} controls only I2C internal clock and implemented through the circuit above. The smaller the R_{IB}, the more internal clock frequency and the power current of the I2C。

11.2 Start and end

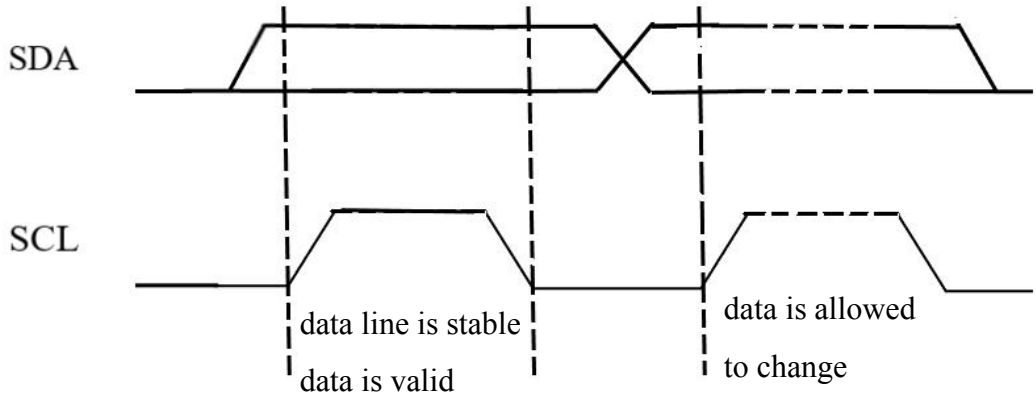
- start（S）
- end（P）
- restart（Sr）



11.3 Validity of data

When the SCL is high, the SDA is stable, and when the SCL is low, the SDA can

be changed.

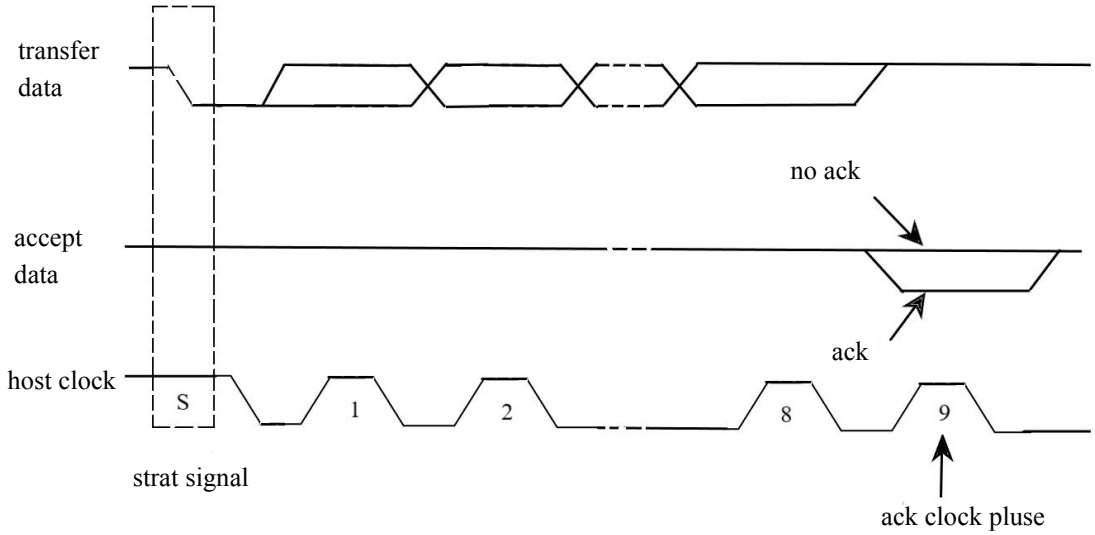


11.4 Byte format

The byte structure consists of 8 bit data and a response signal.

11.5 Acknowledge

The acknowlege signal detects whether the receiver is correct in the sender's data, and if correct, the receiving party writes 0, otherwise writes 1.。



11.6 First byte

11.6.1 Slave address

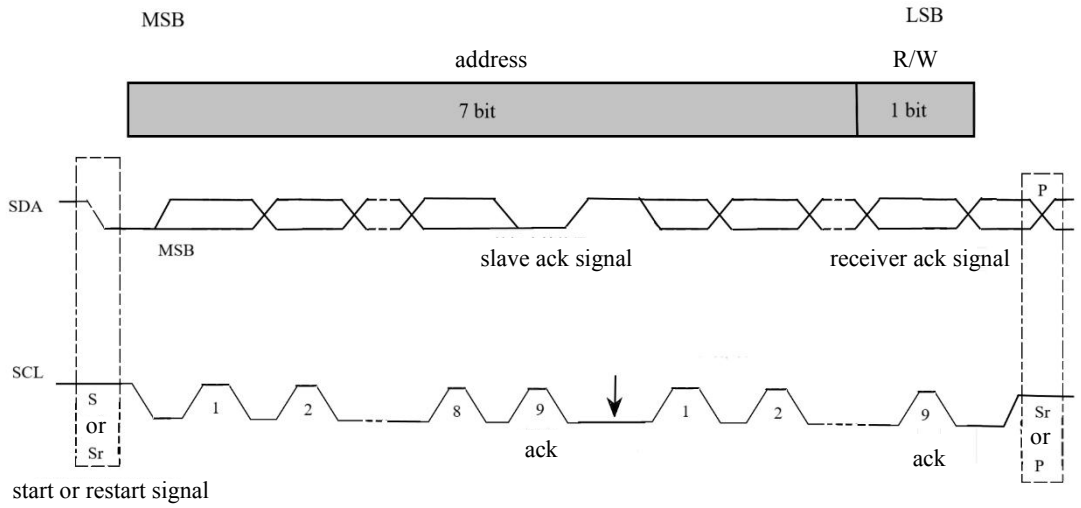
The first byte after the start of the machine is used to access the machine. Si12T

chip address：

ID_SEL	Address
GND	0xD0
VDD	0xF0

11.6.2 R/ $\overline{W}$

This bit determines the direction of the data, which follows the address data.



11.7 Transfer data

11.7.1 Write opration

The sequence of bytes is as follows：

- The first byte gives the device address and direction bits ；(R/W=0）
- The second byte contains the internal address of the first register to be accessed;
- The next byte is written to the internal register, and the subsequent bytes are written to subsequent internal registers;
- Until the end of the stop signal transmission is encountered;
- Si12T confirms the transmission of each byte.

S	Device address	0	A	Data 1	A	。。。	Data n	$\bar{A}$	P

Note: The shaded part is transferred from the host to the slave; the blank part is transferred from the slave to the host;

A = No ack (SDA pulls high); A = ack (SDA pulls low); S = start signal.。

11.7.2 Read operation

The address of the first register is programmed to be programmed to read the address of the first register without data, and the termination of the condition is received. Then, the other starting position follows the device address and R/W = 1. After that, all subsequent bytes begin to read the data continuously from the beginning address.

S	Device address	1	A	Data 1	A	….	Data n	$\bar{A}$	P

11.7.3 Read/write operation

S	Device address	R/W	A	N byte data +ack	Sr	Device address	read/write	A	N byte data +ack	P

11.8 I2C read/write operation in normal mode

The following figure indicates that the I2C write and read register in normal mode

- Data AA and BB writes register 0x00 to 0x01

S	Device address 0xD0/F0	ack	Register address 0x00	ack	AA	ack	BB	ack	P

- read register 0x00 to 0x01

S	Device address 0xD0/F0	ack	Register address0x00	ack	P

S	Device address 0xD1/F1	ack	Read data AA	ack	Read data BB	No ack	P

12. Si12T control register lists

Note 1: Unused bit bits (defined as reserved bits) in I2C registers must hold bit 0;

Note 2: HS (high sensitivity) / MS (medium sensitivity) / LS (low sensitivity);

Note 3: Low Output / Middle Output / High Output.。

12.1 I2C register mapping

Name	Address (Hex)	Reset value (Bin)	Bit name of each byte							
			Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SEN1	02h	1011 1011	Ch2HL	Ch2M			Ch1HL	Ch1M		
SEN2	03h	1011 1011	Ch4HL	Ch4M			Ch3HL	Ch3M		
SEN3	04h	1011 1011	Ch6HL	Ch6M			Ch5HL	Ch5M		
SEN4	05h	1011 1011	Ch8HL	Ch8M			Ch7HL	Ch7M		
SEN5	06h	1011 1011	Ch10HL	Ch10M			Ch9HL	Ch9M		
SEN6	07h	1011 1011	Ch12HL	Ch12M			Ch11HL	Ch11M		
CFIG	08h	0010 0010	MS	FTC[1:0]		ILC[1:0]		RTC[2:0]		
CTRL	09h	0000 01xx	0	0	0	0	SRST	SLEEP	1	1
Ref_rst1	0Ah	1111 1110	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Ref_rst2	0Bh	0000 1111	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Ch_on1	0Ch	1111 1110	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Ch_on2	0Dh	0011 1111	0	0	1	1	Ch12	Ch11	Ch10	Ch9
Cal_on1	0Eh	0000 0000	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
Cal_on2	0Fh	0000 0000	0	0	0	0	Ch12	Ch11	Ch10	Ch9
Output1	10h	0000 0000	OUT4		OUT3		OUT2		OUT1	
Output2	11h	0000 0000	OUT8		OUT7		OUT6		OUT5	
Output3	12h	0000 0000	OUT12		OUT11		OUT10		OUT9	
UnLock_ CTRL2	3Bh	0000 0000	UnLock_CTRL2							
CTRL2	3Dh	0000 0000	Reserved							FTC_ Skip

12.2 Detailed Description

12.2.1 Sensitivity control register

type：R/W

address	register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	SEN1	Ch2HL	Ch2M			Ch1HL	Ch1M		

03h	SEN2	Ch4HL	Ch4M	Ch3HL	Ch3M
04h	SEN3	Ch6HL	Ch6M	Ch5HL	Ch5M
05h	SEN4	Ch8HL	Ch8M	Ch7HL	Ch7M
06h	SEN5	Ch10HL	Ch10M	Ch9HL	Ch9M
07h	SEN6	Ch12HL	Ch12M	Ch11HL	Ch11M

Description：

The sensitivity of channel 1~ 12 can be adjusted by SEN1~ SEN6 register. The ChxM[2:0] allows different medium sensitivity, and the sensitivity of the high and low sensitivity is determined by ChxHL。

<table>
<tr><td>Bit name</td><td>Reset value</td><td colspan="2">function</td></tr>
<tr><td>ChxM[2:0]</td><td>011</td><td colspan="2">Medium sensitivity
◊ 000 ： 0.50% ◊ 100 ： 1.50%
◊ 001 ： 0.70% ◊ 101 ： 2.05%
◊ 010 ： 0.90% ◊ 110 ： 2.55.%
◊ 011 ： 1.20% ◊ 111 ： 3.55%</td></tr>
<tr><td rowspan="3">ChxHL</td><td rowspan="3">1</td><td colspan="2">Channel x choose sensitivity</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>Lowsensitivity high sensitivity
◊ 000 ： 0.40% ◊ 000 ： 0.60%
◊ 001 ： 0.55% ◊ 001 ： 0.85%
◊ 010 ： 0.70% ◊ 010 ： 1.10%
◊ 011 ： 0.95% ◊ 011 ： 1.45%
◊ 100 ： 1.20% ◊ 100 ： 1.85%
◊ 101 ： 1.60% ◊ 101 ： 2.45%
◊ 110 ： 2.05% ◊ 110 ： 3.05%
◊ 111 ： 2.85% ◊ 111 ： 4.30%</td><td>Lowsensitivity high sensitivity
◊ 000 ：0.35% ◊ 000 ：0.65%
◊ 001 ：0.50% ◊ 001 ：0.90%
◊ 010 ：0.60% ◊ 010 ：1.20%
◊ 011 ：0.85% ◊ 011 ：1.60%
◊ 100 ：1.05% ◊ 100 ：2.00%
◊ 101 ：1.40% ◊ 101 ：2.65%
◊ 110 ：1.80% ◊ 110 ：3.30%
◊ 111 ：2.45% ◊ 111 ：4.65%</td></tr>
</table>

NOTE：High medium low sensitivity and touch strength are relative should (such as SENx= 0000, the touch strength is 0.40%~ 0.50%, while low strength touch; The touch strength is 0.50%~ 0.60 %, and the strength is touched. When the touch strength is above 0.60%, the touch is high. 0.40%, 0.50% and 0.60% are shown above）

12.2.2 General setting register

type： R/W

address	register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0

08h	CFIG	MS	FTC[1:0]	ILC[1:0]	RTC[2:0]

Description：

The calibration speed after the last time is very high in the time of the FTC[1:0] definition, which can be very good for the unstable external environment。

Bit name	Reset value	function
MS	0	mode select 0 ： autoselect(fast/slow)mode 1 ： fast mode
FTC[1:0]	01	first touch control 00 ： 5 sec 01 ： 10 sec 10 ： 15 sec 11 ： 20 sec
ILC[1:0]	00	interrupt level control 00 ： output the interrupt when medium or high 01 ： output the interrupt when medium or high or low 10 ： output the interrupt when medium or high 11 ： output the interrupt when high
RTC[2:0]	011	response time control response cycle = RTC[2:0] + 2

12.2.3 General control register

type：R/W

address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
09h	CTRL	0	0	0	0	SRST	SLEEP	1	1

Description：

When the SRST is set, all the digital modules outside the simulation and the I2C module will be reset. When set to dormant mode, the power consumption current becomes very low, but the response time will be longer than normal.

Bit name	Reset value	function
SRST	0	software reset 0 ： not enable 1 ： enable
SLEEP	1	sleep mode enable 0 ： not enable 1 ： enable

12.2.4 Channel reference value reset control register

type：R/W

address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ah	Ref_rst1	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
0Bh	Ref_rst2	0	0	0	0	Ch12	Ch11	Ch10	Ch9

Description：

When Chx is set, the reference value for each channel will be updated.

Bit name	Reset value	function
Ch1	0	0 ： not enable reference value reset 1 ： enable reference value reset
Ch2~Ch12	1	0 ： not enable reference value reset 1 ： enable reference value reset

12.2.5 Channel sense control register

type：R/W

address	register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Ch	Ch_on1	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
0Dh	Ch_on2	0	0	1	1	Ch12	Ch11	Ch10	Ch9

NOTE: Bit 4 and Bit 5 shall hold logic 1 in address 0x0D.

Description：

Each channel operation can be controlled independently. When a certain path is set, the corresponding channel will not work and the calibration will be suspended。

Bit name	Reset value	function
Ch1	0	0 ： enable operation(sensing+ calibrating) 1 ： hold operations(no sensing+ stop calibrating)
Ch2~Ch14	1	0 ： enable operation (sensing+ calibrating) 1 ： hold operations (no sensing+ stop calibrating)

12.2.6 Channel calibrate control register

type：R/W

address	Register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0Eh	Cal_on1	Ch8	Ch7	Ch6	Ch5	Ch4	Ch3	Ch2	Ch1
0Fh	Cal_on2	0	0	0	0	Ch12	Ch11	Ch10	Ch9

Description：

Calibration of each channel can be controlled independently. Even if a channel is

set, each channel is still working

bit name	reset value	function
Ch1~Ch12	0	0 ： enable reference value reset (sensing+ calibrating) 1 ： not enable reference value reset (no sensing+ calibrating)

12.2.7 Output register

type：R

address	register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
10h	output1	OUT4[1:0]		OUT3[1:0]		OUT2[1:0]		OUT1[1:0]	
11h	output2	OUT8[1:0]		OUT7[1:0]		OUT6[1:0]		OUT5[1:0]	
12h	output3	OUT12[1:0]		OUT11[1:0]		OUT10[1:0]		OUT9[1:0]	

Description：

Each channel output of Si12T is compressed into 2bits, and has low, medium, high level output information

bit name	reset value	function
OUT1[1:0] ~ OUT12[1:0]	00	channel output 00 ： no output 01 ： low output 10 ： medium output 11 ： high output

12.2.8 CTRL2 unlock register

type: R/W

address	register name	reset value	function
3Bh	Unlock_CTRL2	00h	CTRL2 lock A5h：CTRL2 writable other：CTRL2 not writable

12.2.9 General control register 2

type: R/W

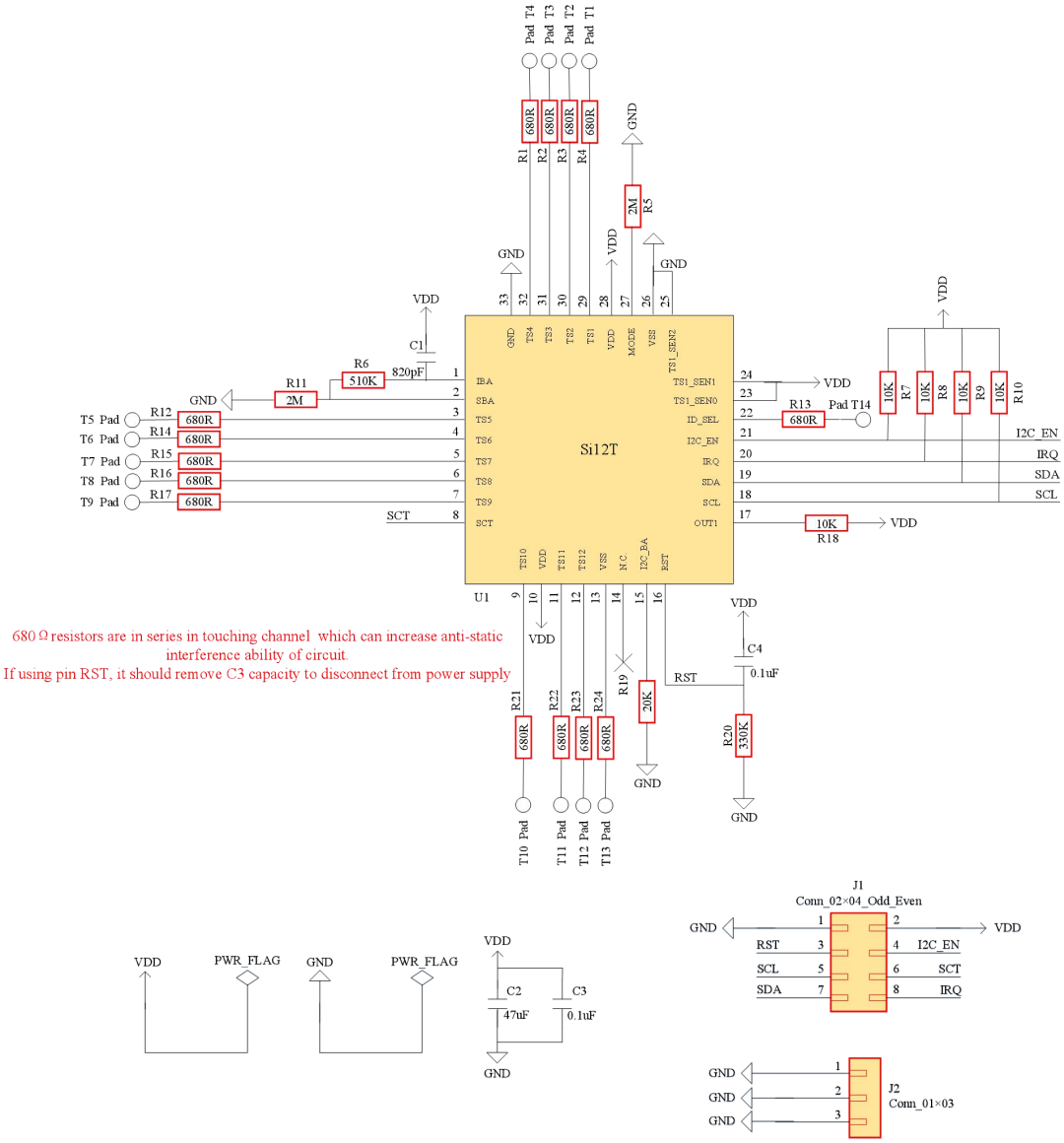
address	register name	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3Dh	CTRL2	resevered							FTC_ Skip

Description:

In FTC time, Si12T will not enter into sleep mode. When external environment is complicated, Si12T will calibre itself quickly. It is not recommended to skip FTC time.

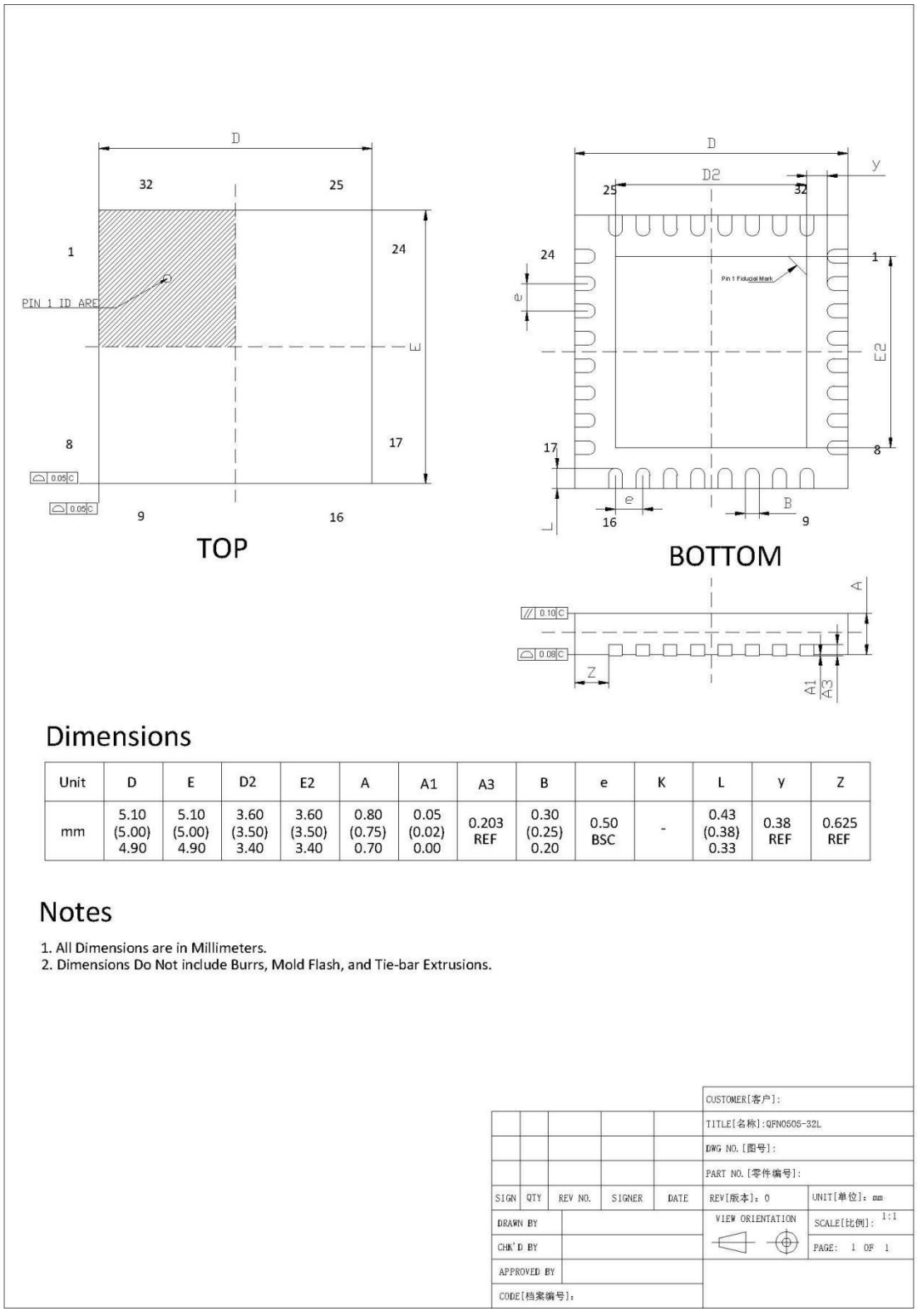
Bit name	Reset value	Function
FTC_Skip	0	0：Do not skip FTC time after power on or reset 1：Kkip FTC time after power on or reset

13. Typical application diagram



14. Package outline

The chip is packaged in 5x5mm QFN32.



Dimensions

Unit	D	E	D2	E2	A	A1	A3	B	e	K	L	y	Z
mm	5.10 (5.00) 4.90	5.10 (5.00) 4.90	3.60 (3.50) 3.40	3.60 (3.50) 3.40	0.80 (0.75) 0.70	0.05 (0.02) 0.00	0.203 REF	0.30 (0.25) 0.20	0.50 BSC	-	0.43 (0.38) 0.33	0.38 REF	0.625 REF

Notes

1. All Dimensions are in Millimeters.
2. Dimensions Do Not include Burrs, Mold Flash, and Tie-bar Extrusions.

					CUSTOMER[客户]:	
					TITLE[名称]:QFN05O5-32L	
					DWG NO.[图号]:	
					PART NO.[零件编号]:	
SIGN	QTY	REV NO.	SIGNER	DATE	REV[版本]: 0	UNIT[单位]: mm
DRAWN BY					VIEW ORIENTATION	SCALE[比例]: 1:1
CHK'D BY						PAGE: 1 OF 1
APPROVED BY						
CODE[档案编号]:						

15. Version information

Version	Modified date	Modified content
V0.1	2023/11/13	First draft

16. Order information

Package sign

Si12T
ABBCDEE

Si12T:chip code

A: Serial number of packaging year, such as 5 means 2020.

BB:Serial number of processing week，such as 42 means the 42nd week of yearA .

C:Packaging factory code，A、HT、NJ or WA，also briefly asA、H、N or W.

D:Testing factory code，A、Z or H.

EE:Production batch code.

Table 16-1 order information

Order code	package	package	Min unit
Si12T-Sample	5×5mm 32-pin QFN	Box/Tube	5
Si12T	5×5mm 32-pin QFN	Tape and reel	4K

17. Technical Support and Contact Information

Nanjing Zhongke Microelectronic Industry Technology Research Institute Co., Ltd
Technical Support Center
Phone: 025-68517780
Address: Room 201, Building B, Research Zone 3, Xuzhuang Software Park, Xuanwu District, Nanjing, Jiangsu, China
Website: http://www.csm-ic.com

Sales and Marketing
Phone: 13645157034, 13645157035
Email: sales@csmic.ac.cn

Technical Support
Phone: 13645157034
Email: supports@csmic.ac.cn