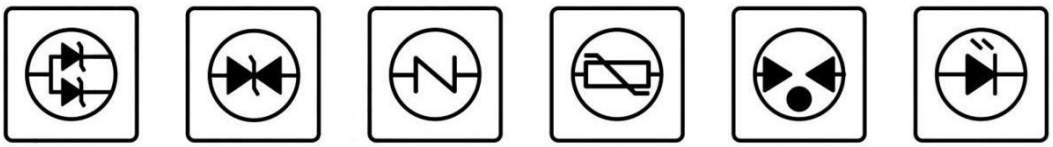
MSKSEMI 美森科
SEMICONDUCTOR



MSKESD5V0V1BCSF

Product specification

MSKESD5V0V1BCSF

Features

- 40Wpeakpulsepowerperline(t_P=8/20μs)
- DFN0603-2Lpackage
- ReplacementforMLV(0201)
- Bidirectionalconfigurations
- Responsetimeistypically<1ns
- HighESDprotection
- Lowclampingvoltage
- RoHScompliant
- Transientprotectionfordatalinesto IEC61000-4-2(ESD)±12KV(air),±10KV(contact); IEC61000-4-4(EFT)40A(5/50ns)

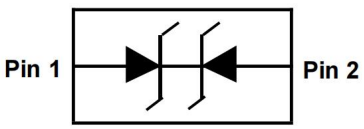
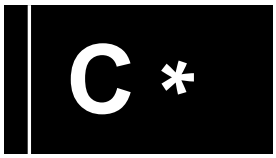
Applications

- Cellularphones
- Portabledevices
- Digitalcameras
- Powersupplies

MechanicalCharacteristics

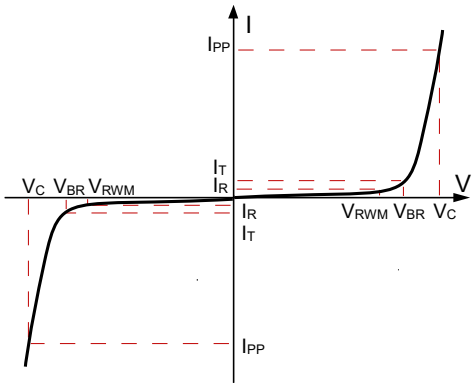
- Mountingposition:Any
- Qualifiedmaxreflowtemperature:260℃
- DevicemeetsMSL 1 requirements

Reference News

PACKAGE OUTLINE	Circuit Diagram	Marking
 0201		

Electronics Parameter

Symbol	Parameter
V_{RWM}	Peak Reverse Working Voltage
I_R	Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
P_{PP}	Peak Pulse Power
C_J	Junction Capacitance
I_F	Forward Current
V_F	Forward Voltage @ I_F



Electricalcharacteristicsperline@25℃ (unlessotherwisespecified)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Peak Reverse Working Voltage	V_{RWM}				5	V
Breakdown Voltage	V_{BR}	I_t = 1mA	5.6	6.7	7.8	V
Reverse Leakage Current	I_R	V_{RWM} = 5V T=25℃			1.0	μA
Clamping Voltage	V_{CL}	I_{PP}=16A		13.5		V
Clamping Voltage	V_C	I_{PP}=1A		7	9	V
Clamping Voltage	V_C	I_{PP}=3A		10	12	V
Junction Capacitance	C_j	V_R=0V f = 1MHz		3.2	6	pF

Absolutemaximumrating@25℃

Rating	Symbol	Value	Units
Peak Pulse Power (t_p=8/20μs)	P_{pp}	40	W
Peak Pulse Current (t_p=8/20μs)	I_{pp}	3	A
Operating Temperature	T_J	-55 to 150	℃
Storage Temperature	T_{STG}	-55 to 150	℃

Typical Characteristics

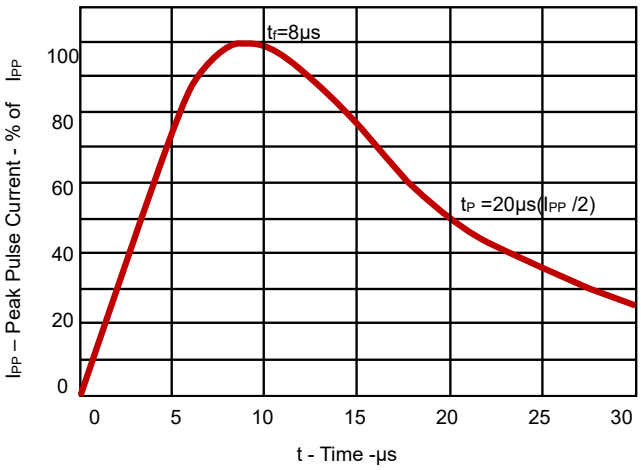


Fig 1.Pulse Waveform

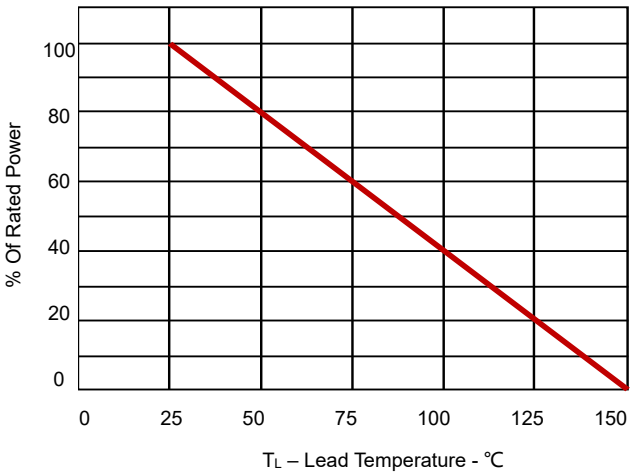


Fig 2.Power Derating Curve

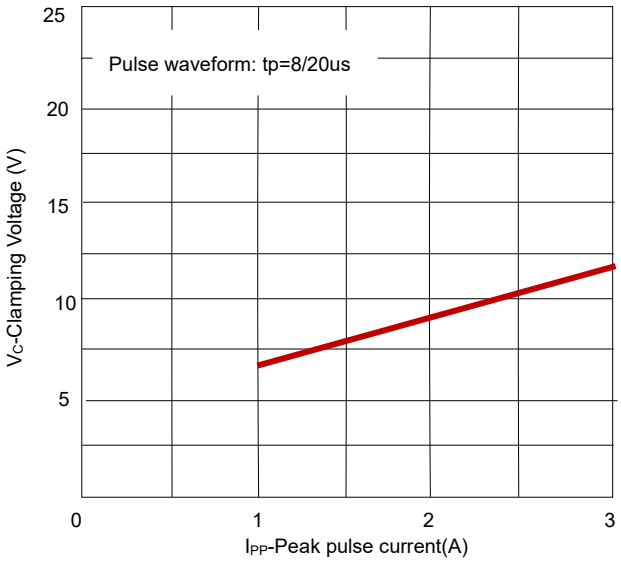


Fig 3. Clamping voltage vs. Peak pulse current

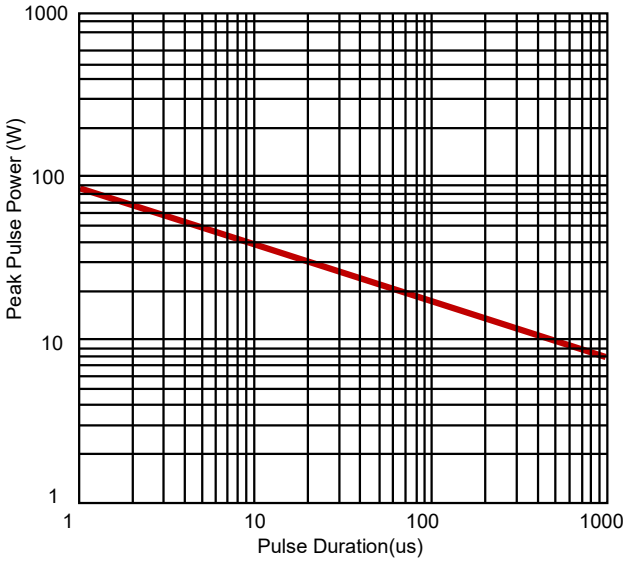


Fig 4. Non Repetitive Peak Pulse Power vs. Pulse time

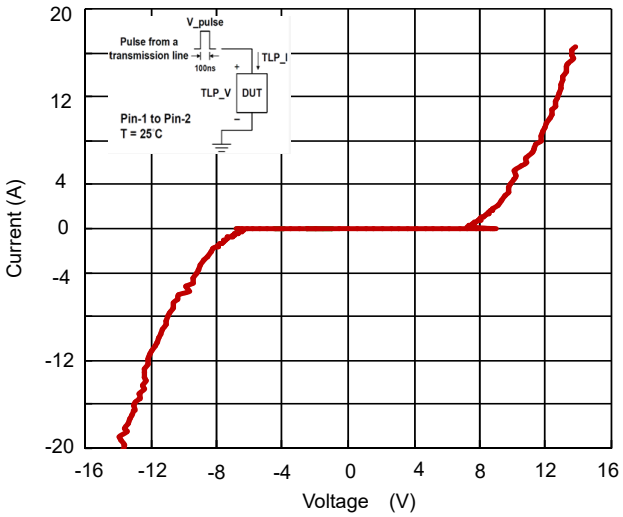


Fig 5. TLP Measurement

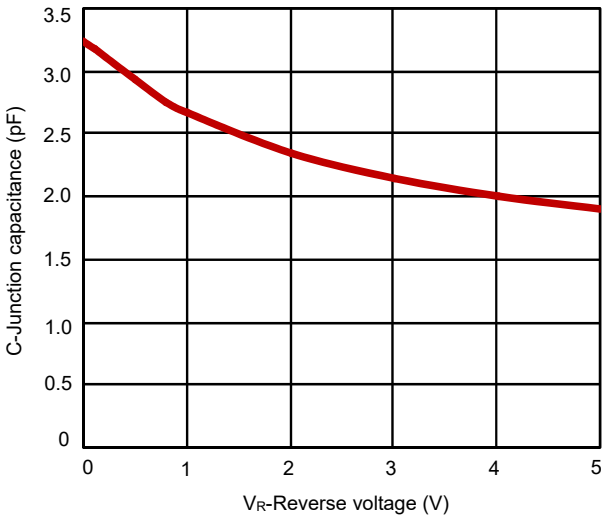
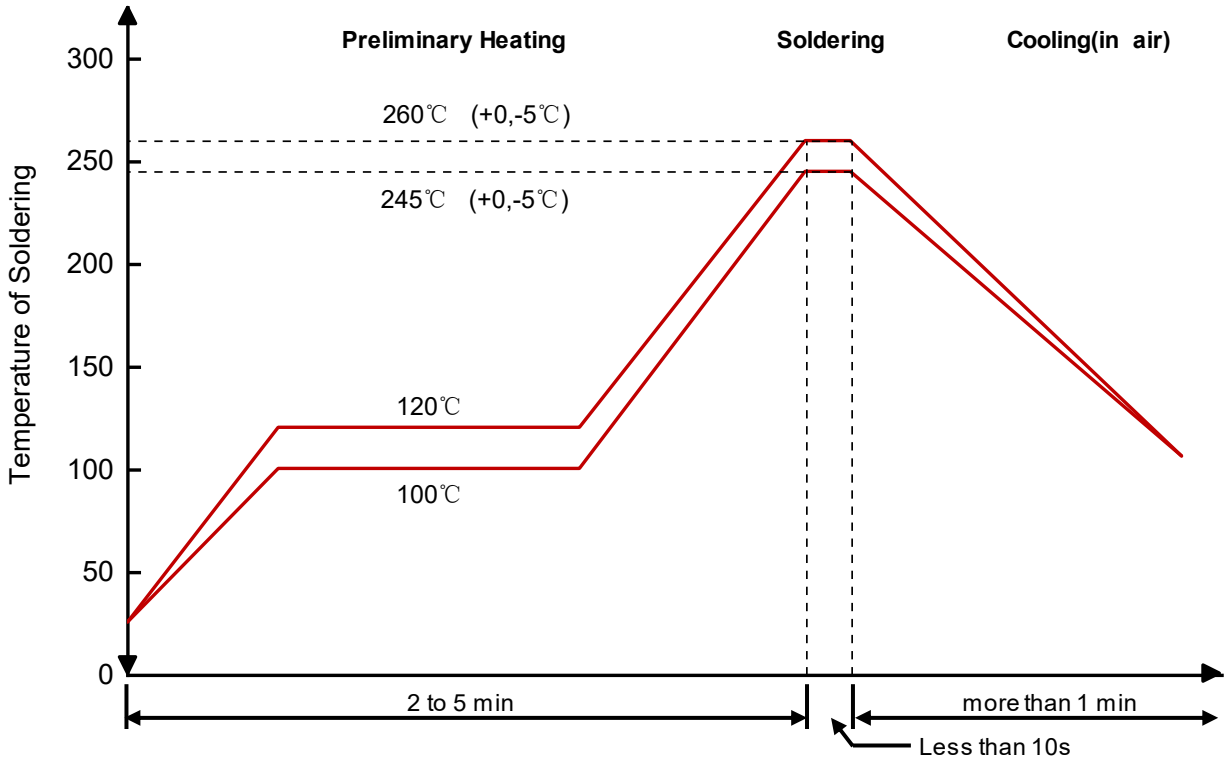


Fig 6. Capacitance vs. Reveres voltage

Solder Reflow Recommendation



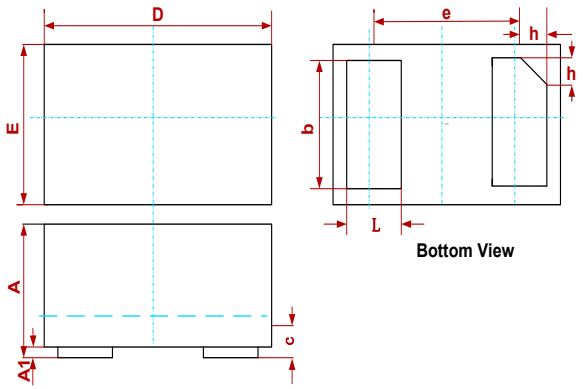
Remark: Pb free for 260℃； Pb for 245℃.

PCB Design

For TVS diodes a low-ohmic and low-inductive path to chassis earth is absolutely mandatory in order to achieve good ESD protection. Novices in the area of ESD protection should take following suggestions to heart:

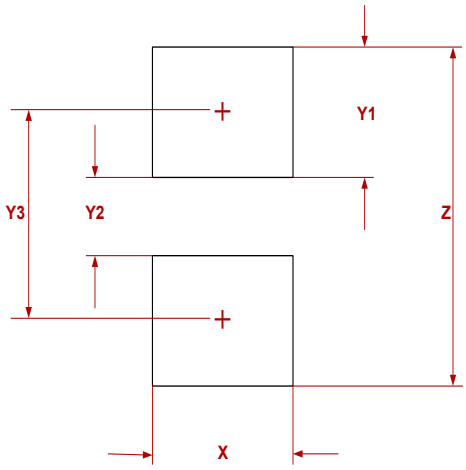
- Do not use stubs, but place the cathode of the TVS diode directly on the signal
- trace. Do not make false economies and save copper for the ground connection.
- Place via holes to ground as close as possible to the anode of the TVS diode.
- Use as many via holes as possible for the ground connection.
- Keep the length of via holes in mind! The longer the more inductance they will have.

PACKAGE MECHANICAL DATA



SYM	DIMENSIONS		
	MILLIMETERS		
	MIN	NOM	MAX
A	0.230		0.330
A1	0.000	0.020	0.050
b	0.215	0.245	0.275
c	0.120	0.150	0.180
D	0.550	0.600	0.650
e	0.355 BSC		
E	0.250	0.300	0.350
L	0.160	0.190	0.220
h	0.079 BSC		

Suggested Pad Layout



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
X	0.30	0.012
Y1	0.25	0.010
Y2	0.15	0.006
Y3	0.40	0.016
Z	0.65	0.026

REEL SPECIFICATION

P/N	PKG	QTY
MSKESD5V0V1BCSF	0201	15000

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