

MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ C7

650V CoolMOS™ C7 Power Transistor
IPZ65R019C7

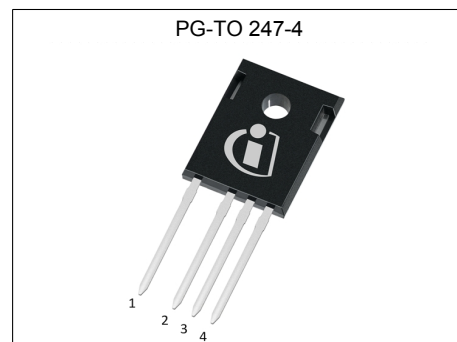
Data Sheet

Rev. 2.0
Final

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.



Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package
- Easy to use/drive due to **driver source pin** for better control of the gate.
- Pb-free plating, halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Benefits

- Enabling higher system efficiency
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures

Applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

Please note: The source and sense source pins are not exchangeable. Their exchange might lead to malfunction.

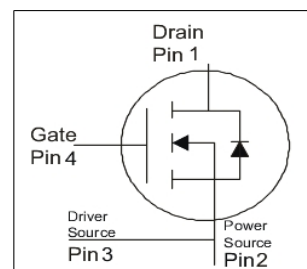


Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	19	mΩ
$Q_{g,typ}$	215	nC
$I_{D,pulse}$	496	A
$E_{oss@400V}$	27	μJ
Body diode di/dt	70	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPZ65R019C7	PG-TO 247-4	65C7019	see Appendix A

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2 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	75 62	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	496	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	583	mJ	$I_D=12.4\text{A}$; $V_{DD}=50\text{V}$
Avalanche energy, repetitive	E_{AR}	-	-	2.92	mJ	$I_D=12.4\text{A}$; $V_{DD}=50\text{V}$
Avalanche current, single pulse	I_{AS}	-	-	12.4	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	446	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	60	Ncm	M3 and M3.5 screws
Continuous diode forward current	I_S	-	-	75	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	496	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	1.5	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$
Maximum diode commutation speed	di/dt	-	-	70	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq I_S$, $T_j=25^\circ\text{C}$
Insulation withstand voltage	V_{ISO}	-	-	n.a.	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$.

³⁾ Identical low side and high side switch with identical R_G .

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.28	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	62	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

4 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V$, $I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=2.92mA$
Zero gate voltage drain current	I_{DSS}	-	-	5	μA	$V_{DS}=650$, $V_{GS}=0V$, $T_j=25^\circ\text{C}$ $V_{DS}=650$, $V_{GS}=0V$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20V$, $V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.017 0.040	0.019 -	Ω	$V_{GS}=10V$, $I_D=58.3A$, $T_j=25^\circ\text{C}$ $V_{GS}=10V$, $I_D=58.3A$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.45	-	Ω	$f=1MHz$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	9900	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Output capacitance	C_{oss}	-	160	-	pF	$V_{GS}=0V$, $V_{DS}=400V$, $f=250kHz$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	338	-	pF	$V_{GS}=0V$, $V_{DS}=0...400V$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	3320	-	pF	$I_D=\text{constant}$, $V_{GS}=0V$, $V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	30	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=58.3A$, $R_G=1.8\Omega$
Rise time	t_r	-	27	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=58.3A$, $R_G=1.8\Omega$
Turn-off delay time	$t_{d(off)}$	-	106	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=58.3A$, $R_G=1.8\Omega$
Fall time	t_f	-	5	-	ns	$V_{DD}=400V$, $V_{GS}=13V$, $I_D=58.3A$, $R_G=1.8\Omega$

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	53	-	nC	$V_{DD}=400V$, $I_D=58.3A$, $V_{GS}=0$ to $10V$
Gate to drain charge	Q_{gd}	-	71	-	nC	$V_{DD}=400V$, $I_D=58.3A$, $V_{GS}=0$ to $10V$
Gate charge total	Q_g	-	215	-	nC	$V_{DD}=400V$, $I_D=58.3A$, $V_{GS}=0$ to $10V$
Gate plateau voltage	$V_{plateau}$	-	5.4	-	V	$V_{DD}=400V$, $I_D=58.3A$, $V_{GS}=0$ to $10V$

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V$, $I_F=58.3A$, $T_j=25^{\circ}C$
Reverse recovery time	t_{rr}	-	760	-	ns	$V_R=400V$, $I_F=75A$, $di_F/dt=70A/\mu s$
Reverse recovery charge	Q_{rr}	-	20	-	μC	$V_R=400V$, $I_F=75A$, $di_F/dt=70A/\mu s$
Peak reverse recovery current	I_{rrm}	-	50	-	A	$V_R=400V$, $I_F=75A$, $di_F/dt=70A/\mu s$

5 Electrical characteristics diagrams

Table 8

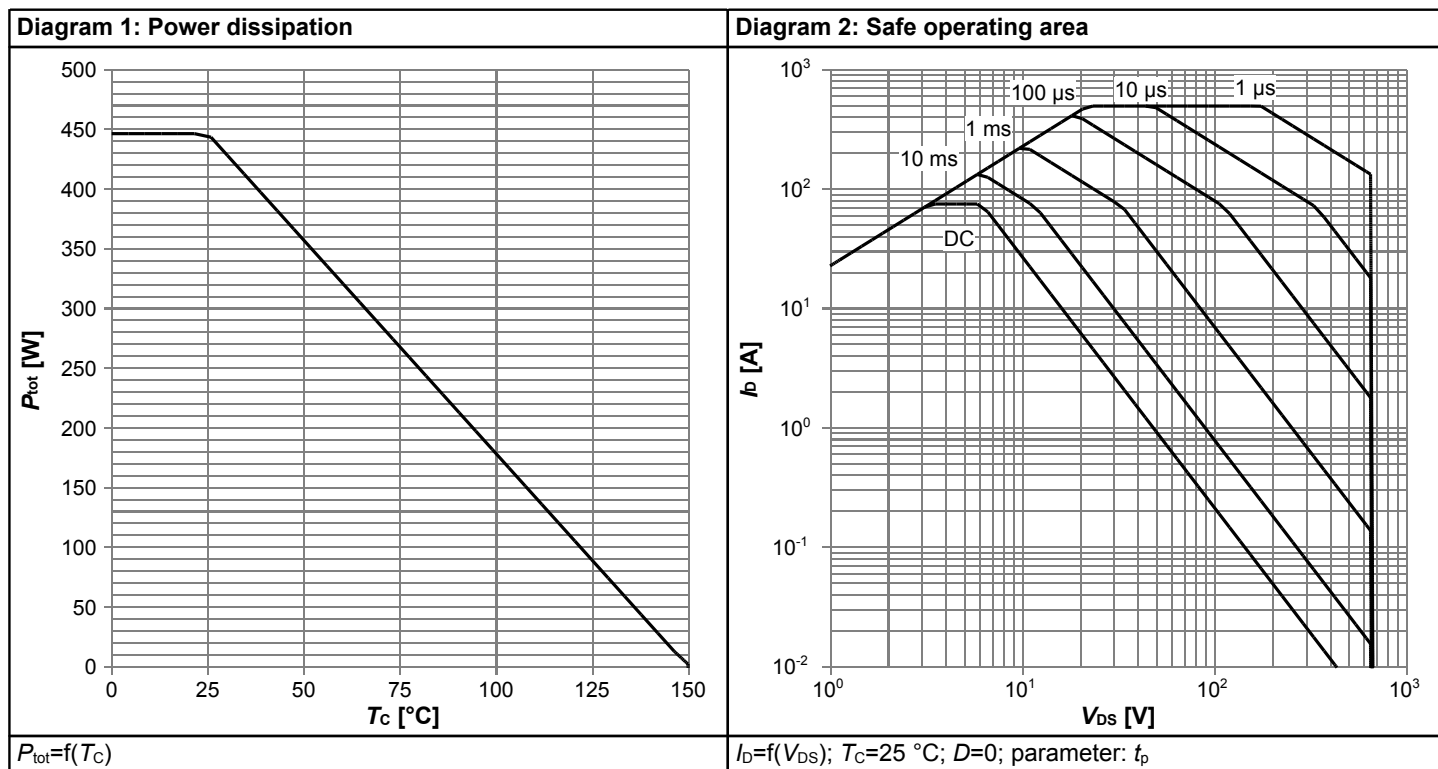


Table 9

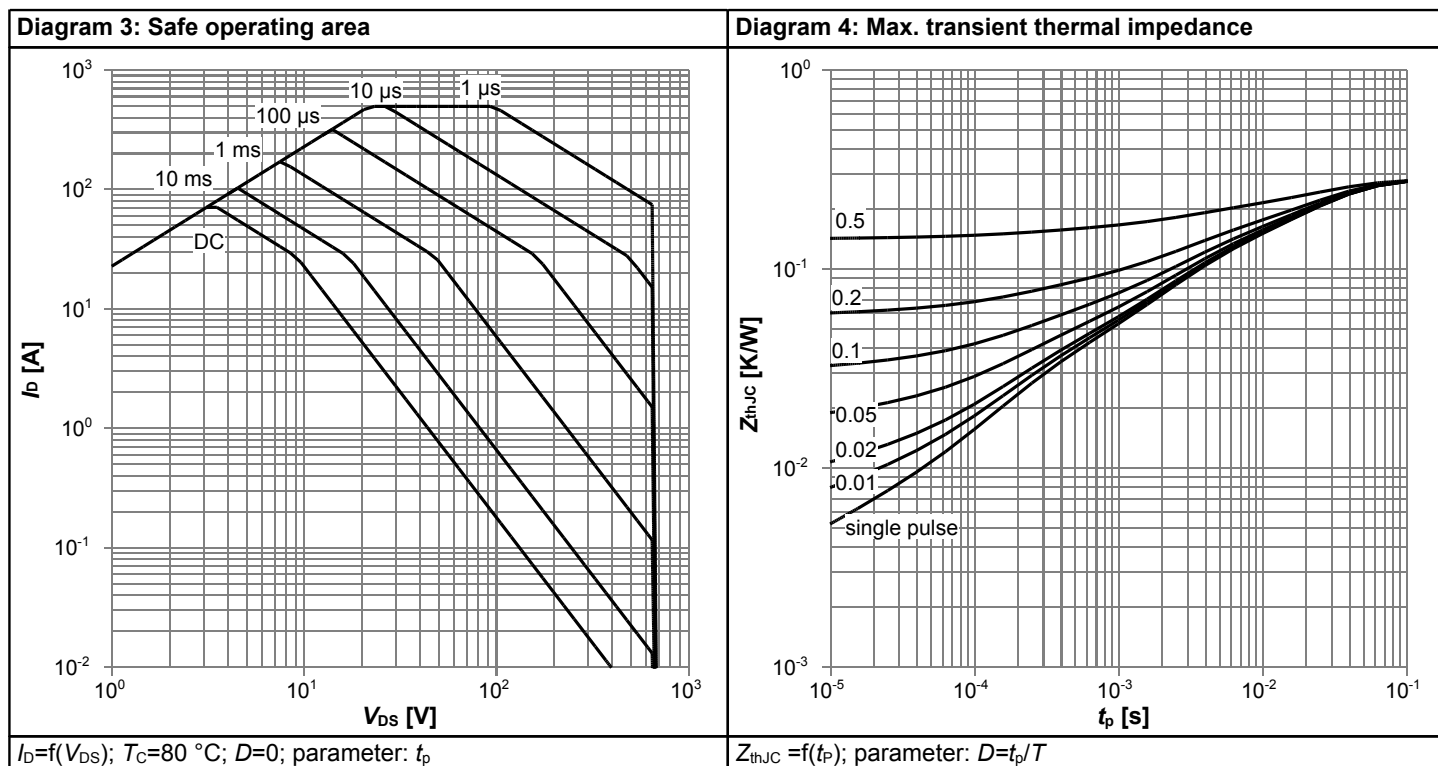


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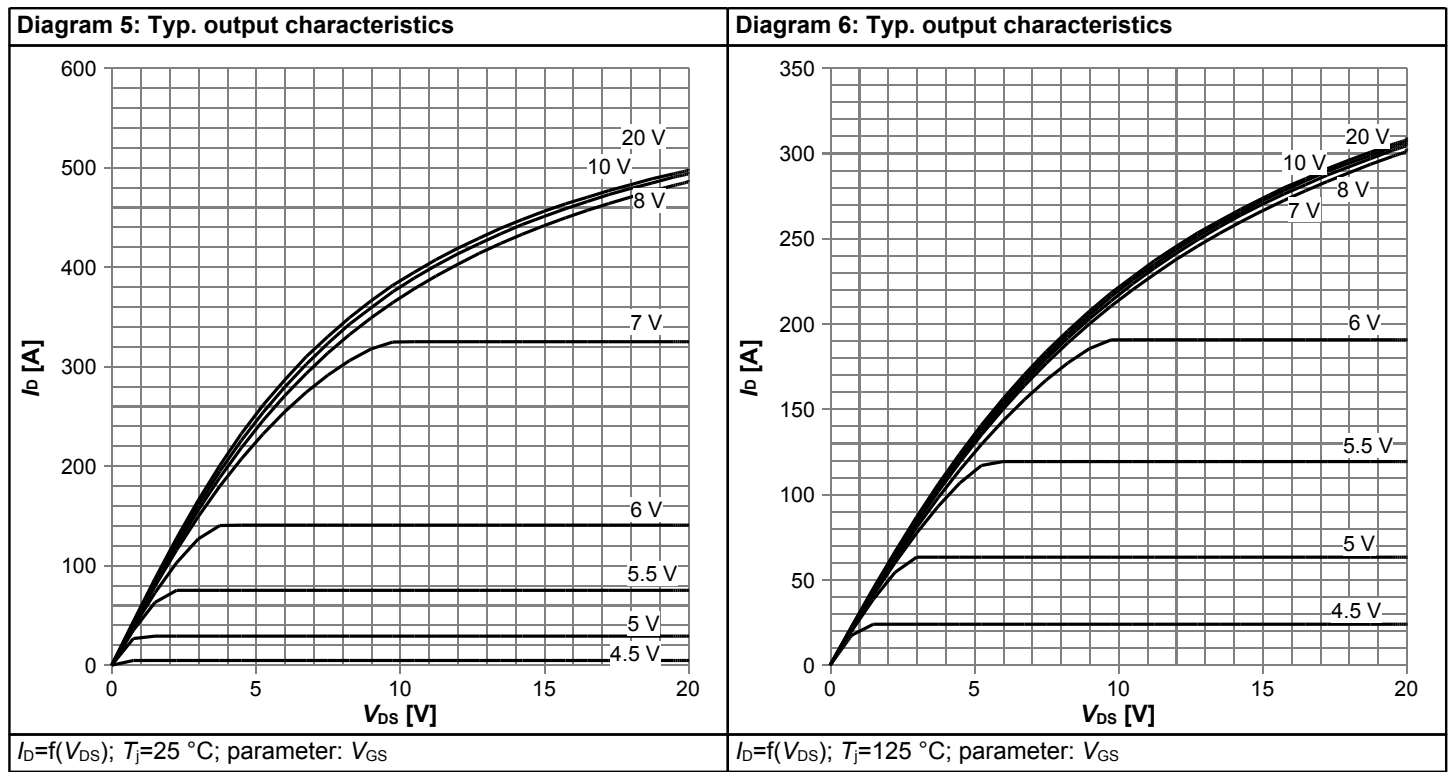


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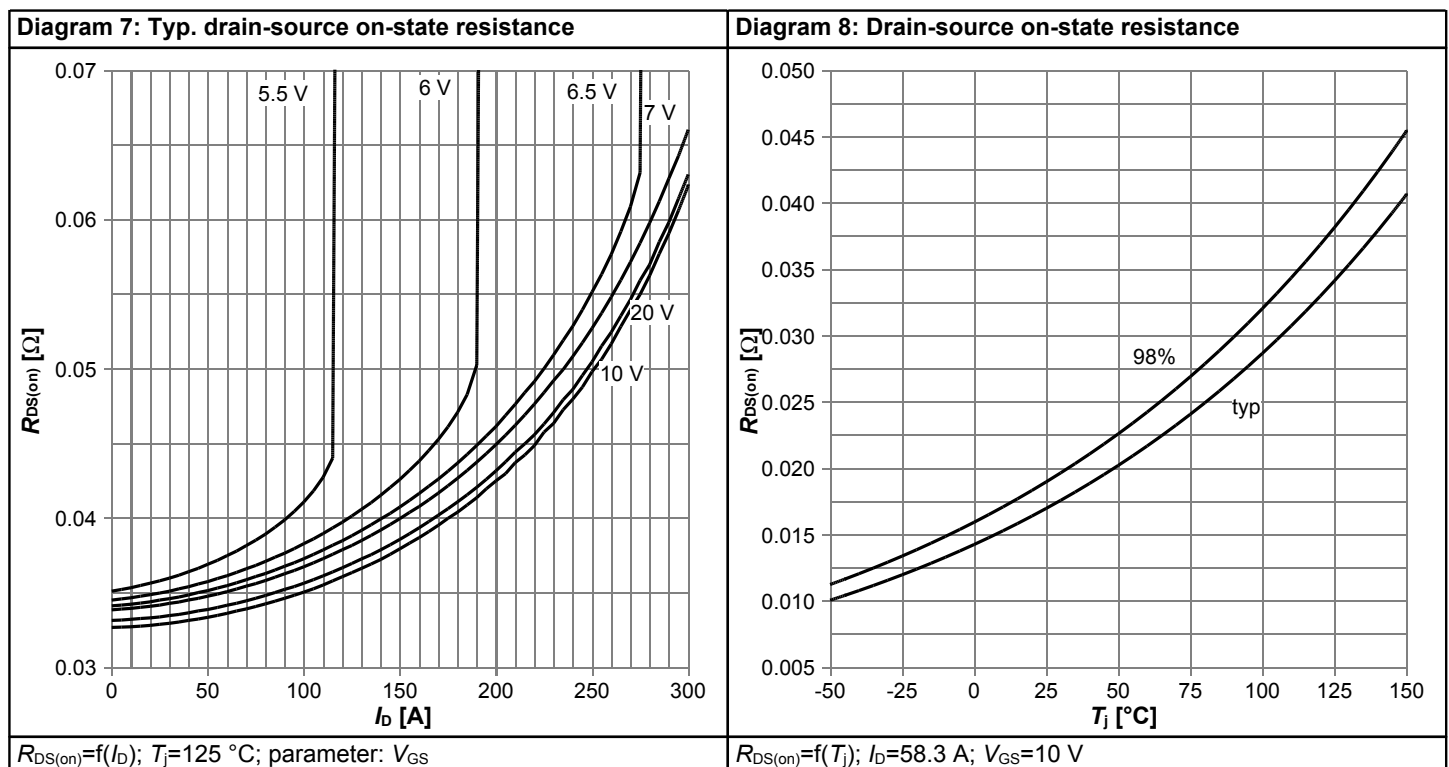


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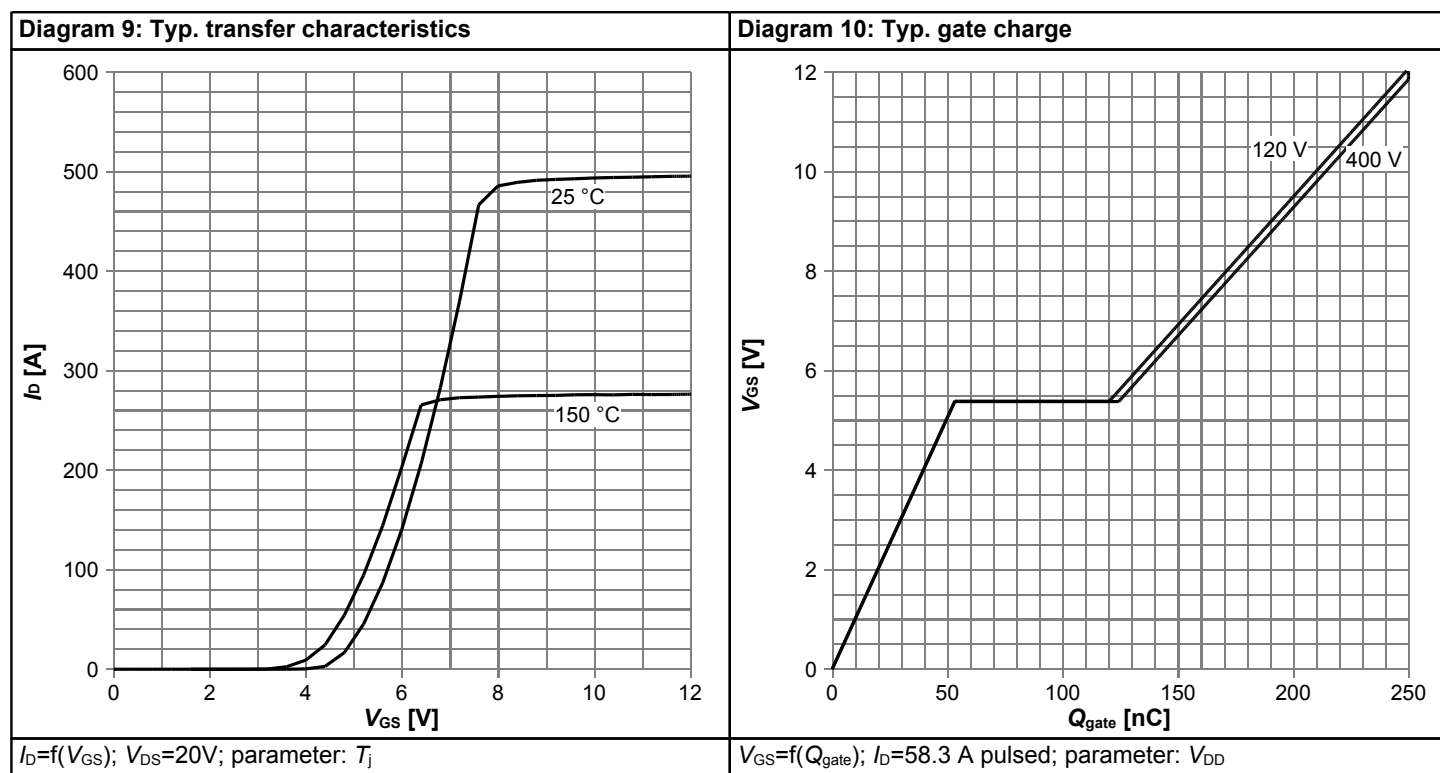


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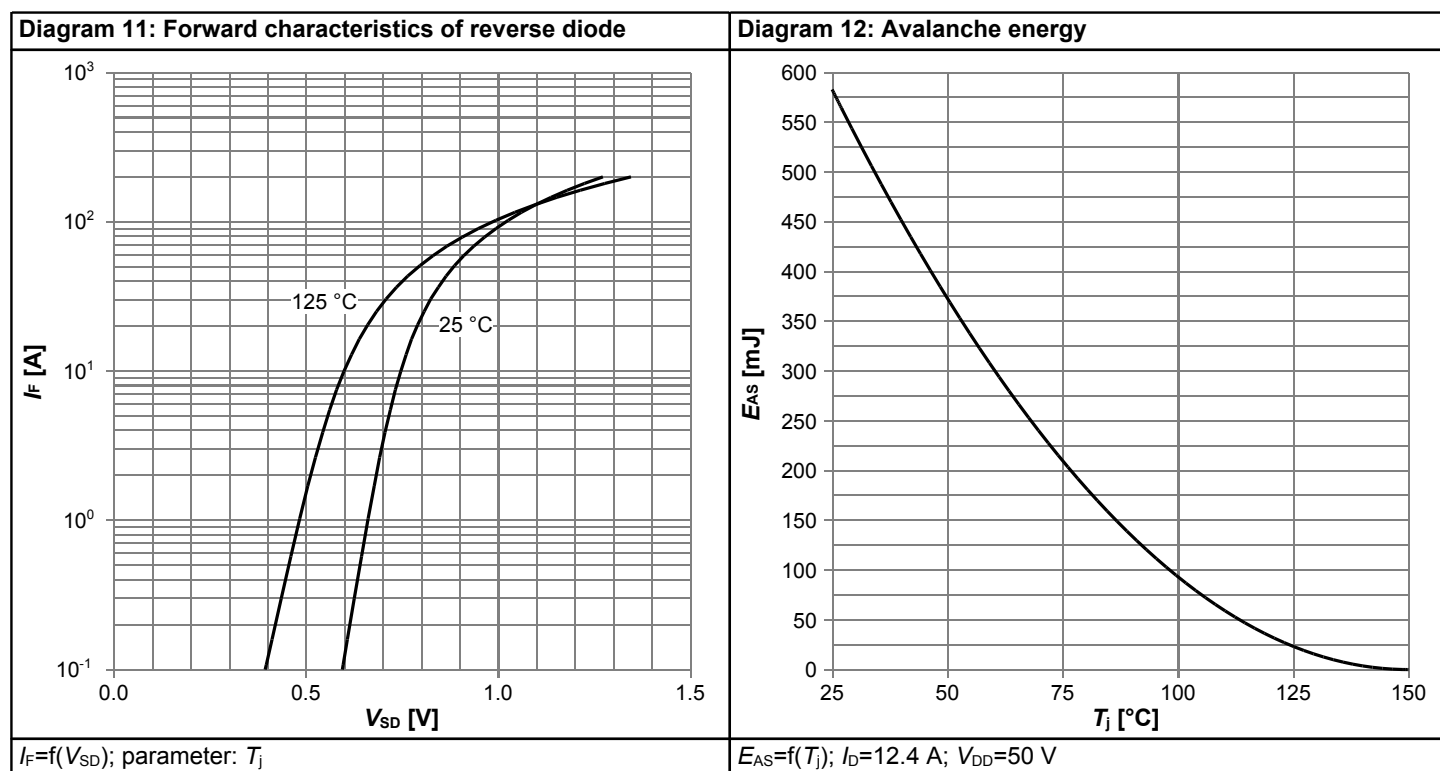


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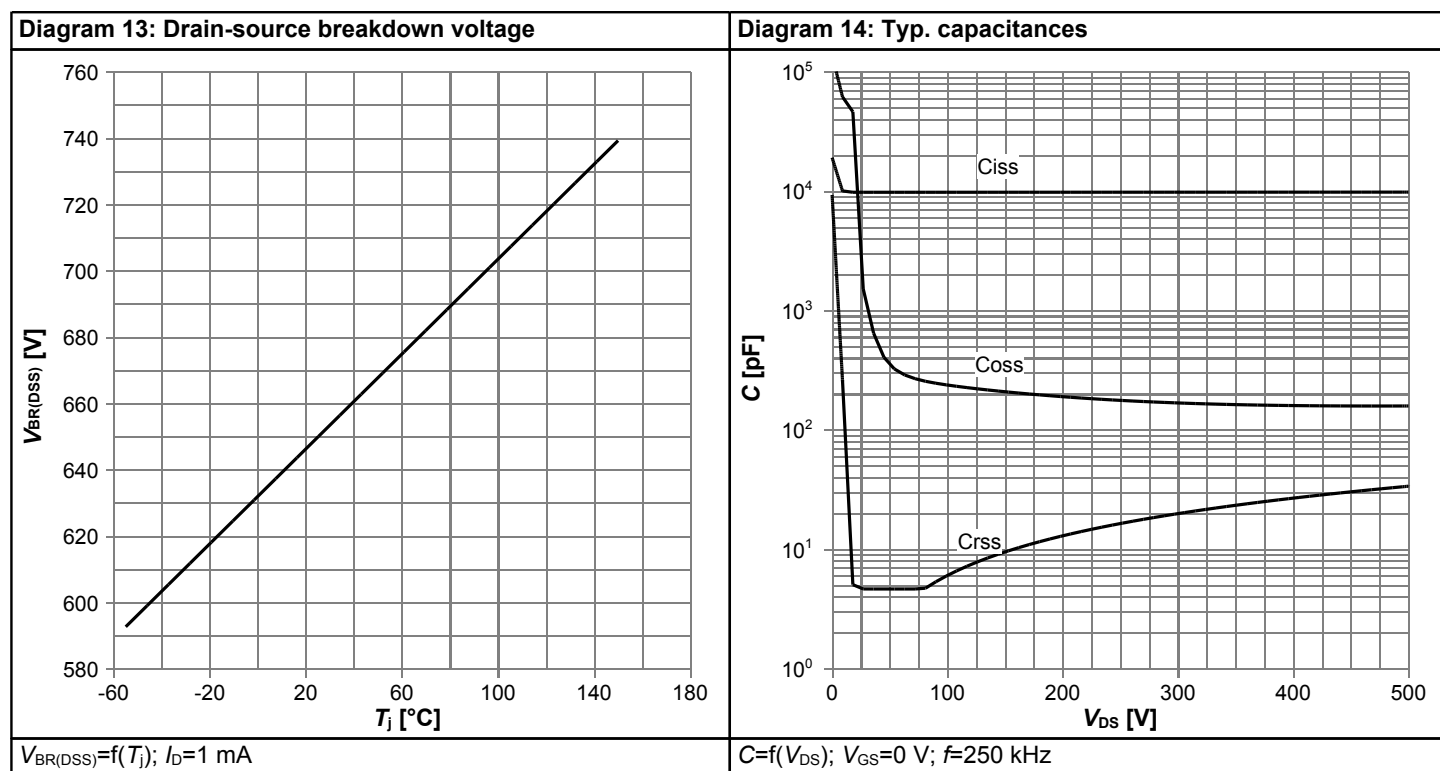
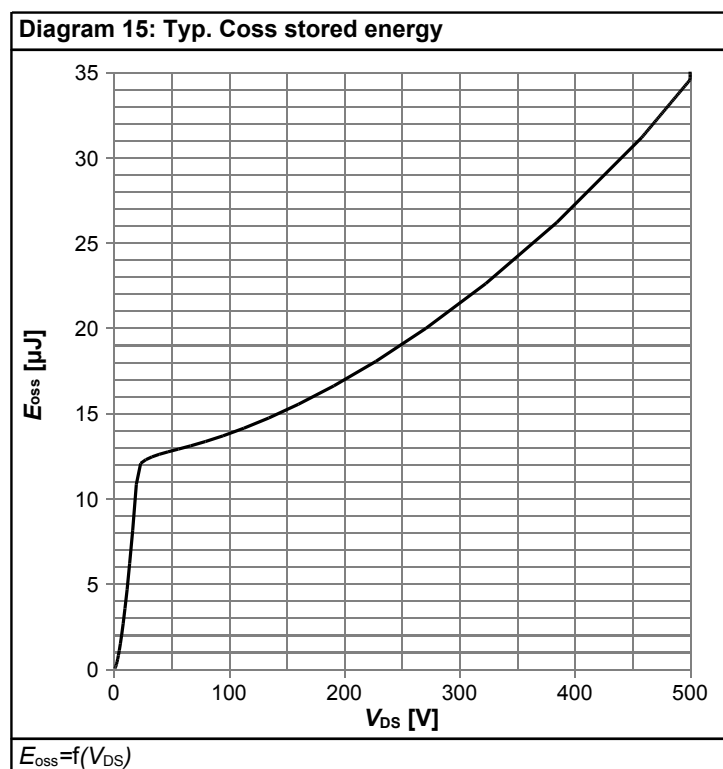


Table 15



6 Test Circuits

Table 16 Diode characteristics

Test circuit for diode characteristics $R_{g1} = R_{g2}$	Diode recovery waveform $t_{rr} = t_F + t_S$ $Q_{rr} = Q_F + Q_S$
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Table 17 switching times (ss)

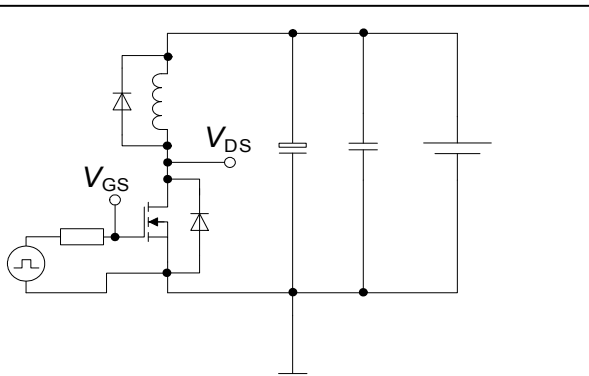
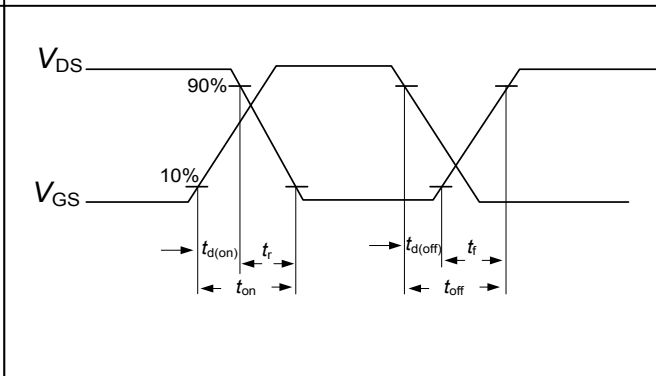
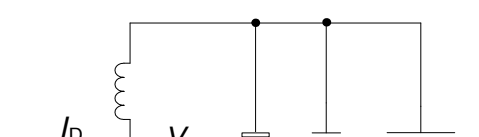
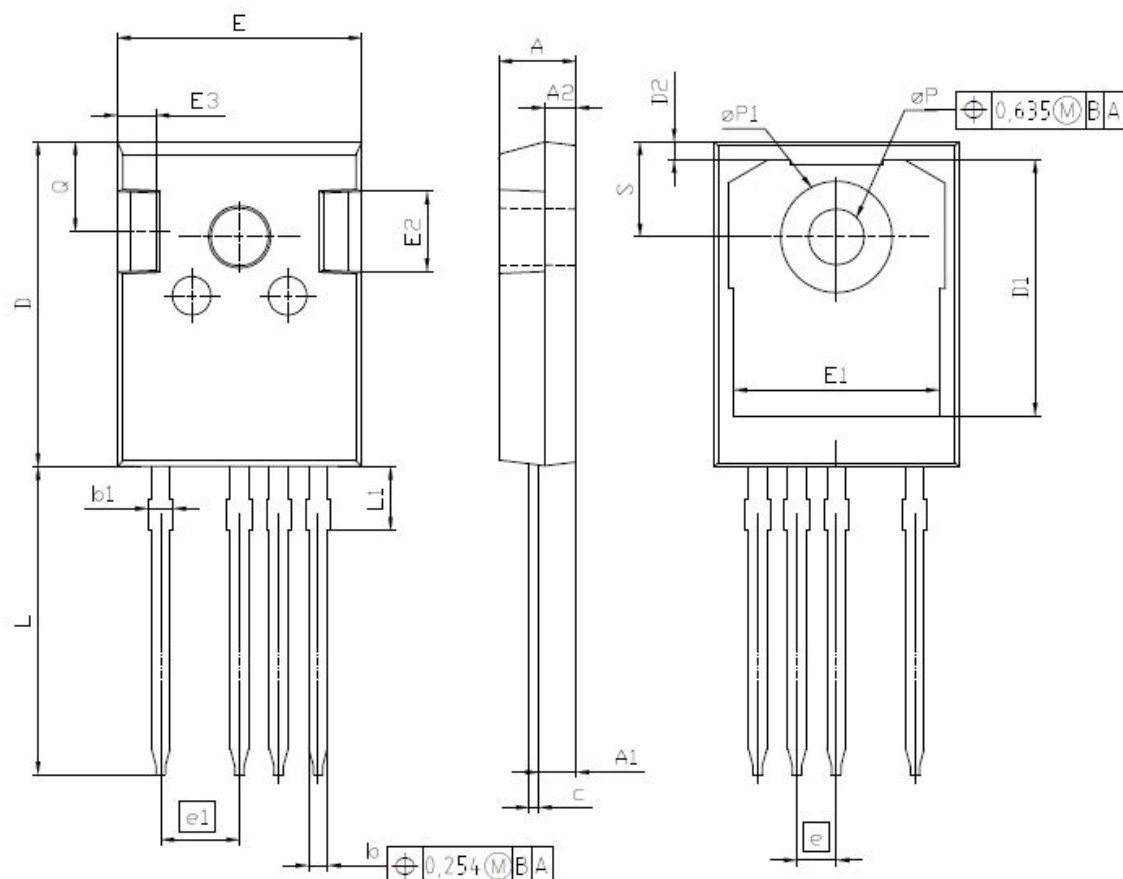
Switching times test circuit for inductive load	Switching times waveform
 The circuit diagram illustrates a MOSFET switching an inductive load. A pulse generator provides a gate voltage V_{GS} through a resistor. The MOSFET's drain is connected to a DC source V_{DS} and an inductive load (inductor and diode). The source is grounded. The inductor is in series with the MOSFET drain, and the diode is in parallel with the load. The MOSFET's gate is driven by a pulse generator. The drain voltage V_{DS} and gate voltage V_{GS} are indicated at measurement points.	 The timing diagram shows the switching waveforms for V_{DS} and V_{GS}. The gate voltage V_{GS} transitions from 10% to 90% and back. The drain voltage V_{DS} transitions from high to low and back. The switching times are defined as follows: $t_{d(on)}$: Delay time from 10% V_{GS} to 90% V_{DS}. t_r: Rise time from 90% V_{DS} to 10% V_{DS}. t_{on}: Total on-time from 10% V_{GS} to 10% V_{DS}. $t_{d(off)}$: Delay time from 90% V_{GS} to 90% V_{DS}. t_f: Fall time from 90% V_{DS} to 10% V_{DS}. t_{off}: Total off-time from 90% V_{GS} to 10% V_{DS}.

Table 18 Unclamped inductive load (ss)

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	0.190	0.205
A1	2.29	2.54	0.090	0.100
A2	1.90	2.16	0.075	0.085
b	1.07	1.33	0.042	0.052
b1	1.10	1.70	0.043	0.067
c	0.50	0.70	0.020	0.028
D	20.80	21.10	0.819	0.831
D1	16.25	17.65	0.640	0.695
D2	0.95	1.35	0.037	0.053
E	15.70	16.13	0.618	0.635
E1	13.10	14.15	0.516	0.557
E2	3.68	5.10	0.145	0.201
E3	1.00	2.60	0.039	0.102
e	2.54 (BSC)		0.100 (BSC)	
e1	5.08		0.200	
N	4		4	
L	19.72	20.32	0.776	0.800
L1	4.02	4.40	0.158	0.173
øP	3.50	3.70	0.138	0.146
øP1	7.00	7.40	0.276	0.291
Q	5.49	6.00	0.216	0.236
S	6.04	6.30	0.238	0.248

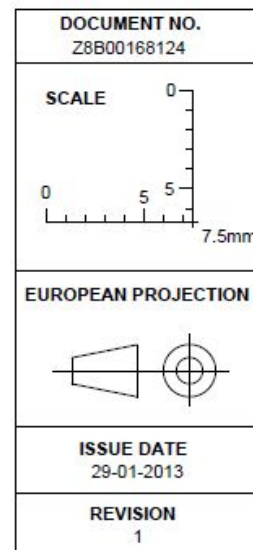


Figure 1 Outline PG-TO 247-4, dimensions in mm/inches

8 Appendix A

Table 19 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPZ65R019C7

Revision: 2013-04-30, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-04-30	Release of final version

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Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

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