N and P Channel Enhancement Mode Power MOSFET

Description

The G085C03D32 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

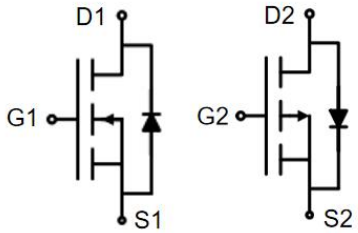
General Features

- NMOS
- V_{DS} 30V
- I_D (at V_{GS} = 10V) 28A
- $R_{DS(ON)}$ (at V_{GS} = 10V) < 11mΩ
- $R_{DS(ON)}$ (at V_{GS} = 4.5V) < 15mΩ
- 100% Avalanche Tested
- RoHS Compliant

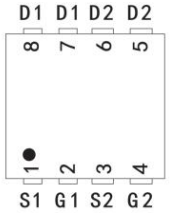
- PMOS
- V_{DS} -30V
- I_D (at V_{GS} = -10V) -12A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 23mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 31mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

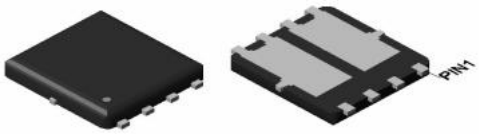
- Power switch
- DC/DC converters



Schematic diagram



pin assignment



DFN3X3-8L Dual

Ordering Information

Device	Package	Marking	Packaging
G085C03D32	DFN3X3-8L Dual	G085C03D	5000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Continuous Drain Current	I_D	28	-12	A
Pulsed Drain Current (note1)	I_{DM}	112	-48	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Power Dissipation	P_D	13	30	W
Single pulse avalanche energy （note2）	E_{AS}	30	36	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	ºC

Thermal Resistance

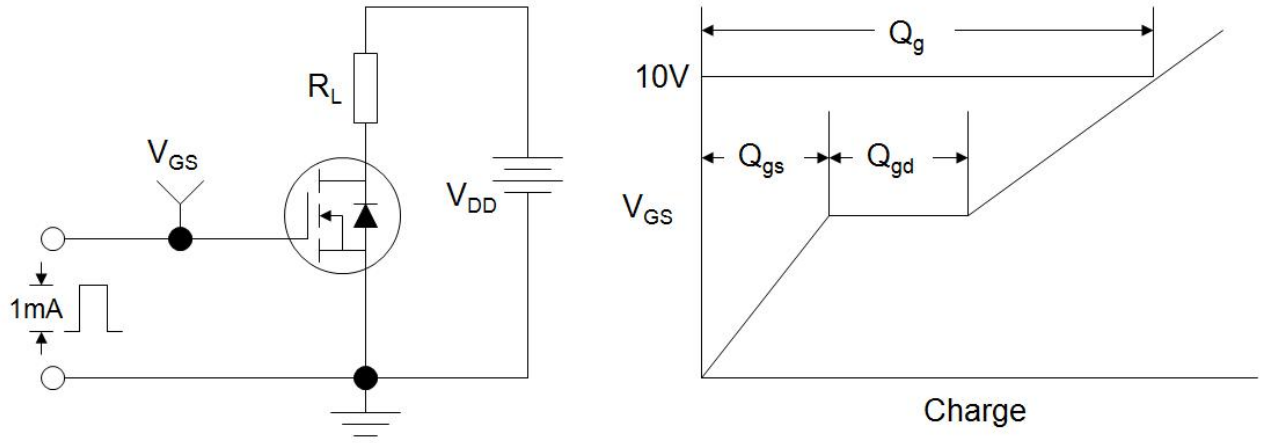
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	55	55	ºC/W
Maximum Junction-to-Case	R_{thJC}	9.6	4.2	ºC/W

NMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = 250μA	30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 30V, V_{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	1.0	1.5	2.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = 10V, I_D = 10A	--	9	11	mΩ
		V_{GS} = 4.5V, I_D = 8A	--	12	15	
Forward Transconductance	g_{FS}	V_{GS} = 5V, I_D = 5A	--	35	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = 15V, f = 1.0MHz	--	1085	--	pF
Output Capacitance	C_{oss}		--	168	--	
Reverse Transfer Capacitance	C_{rss}		--	151	--	
Total Gate Charge	Q_g	V_{DD} = 15V, I_D = 10A, V_{GS} = 10V	--	18	--	nC
Gate-Source Charge	Q_{gs}		--	3	--	
Gate-Drain Charge	Q_{gd}		--	4	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 15V, I_D = 10A, R_G = 3Ω	--	6	--	ns
Turn-on Rise Time	t_r		--	13	--	
Turn-off Delay Time	$t_{d(off)}$		--	20	--	
Turn-off Fall Time	t_f		--	7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	28	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = 10A, V_{GS} = 0V	--	--	1.2	V
Reverse Recovery Charge	Qrr	I_F = 10A, V_{GS} = 0V di/dt=100A/us	--	11	--	nC
Reverse Recovery Time	Trr		--	20	--	ns

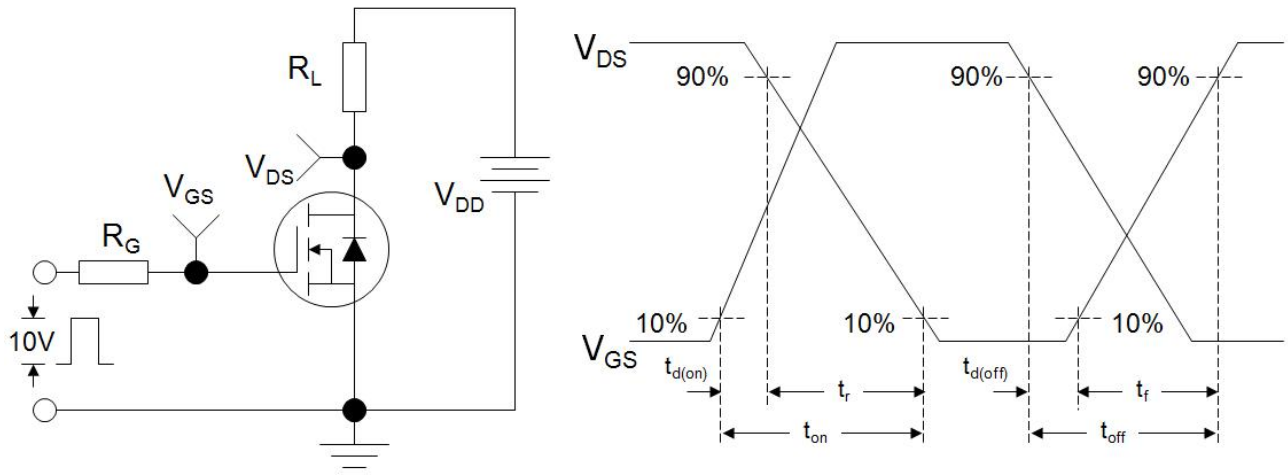
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=30V,VGS=10V,L=0.5mH,Rg=25Ω
3. Identical low side and high side switch with identical R_G

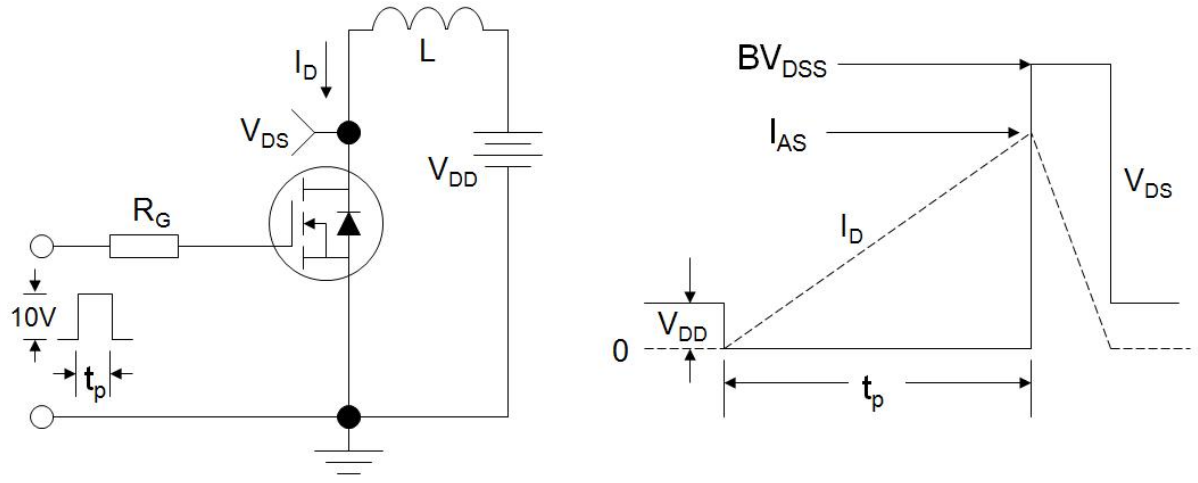
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

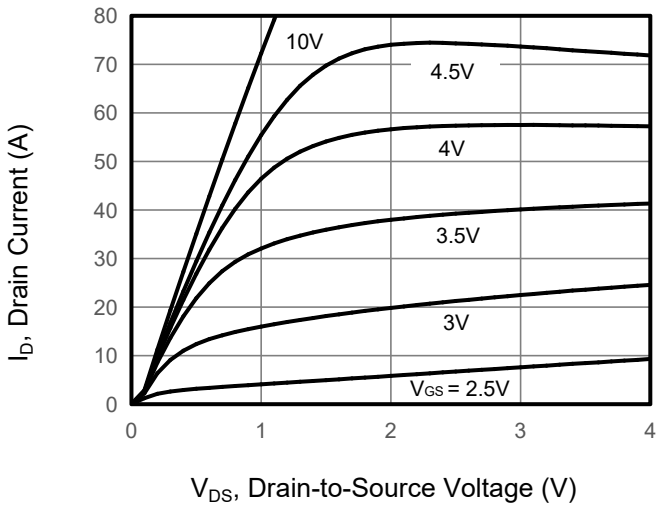


Figure 2. Transfer Characteristics

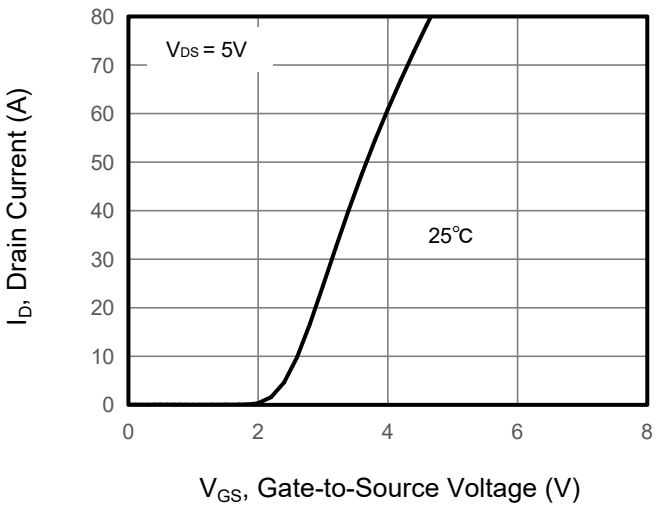


Figure 3. Drain Source On Resistance

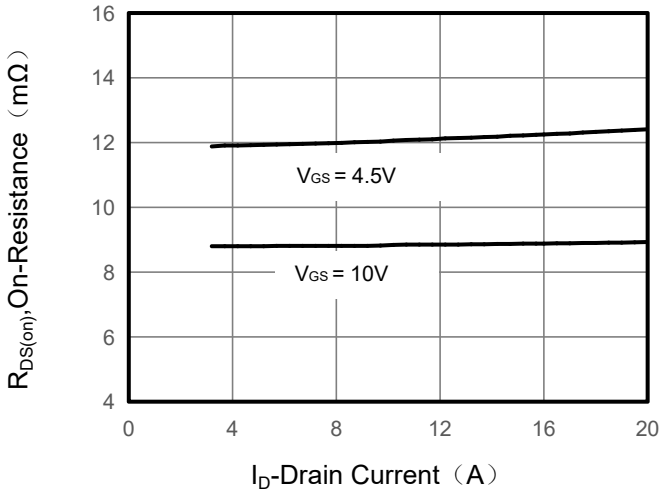


Figure 4. Gate Charge

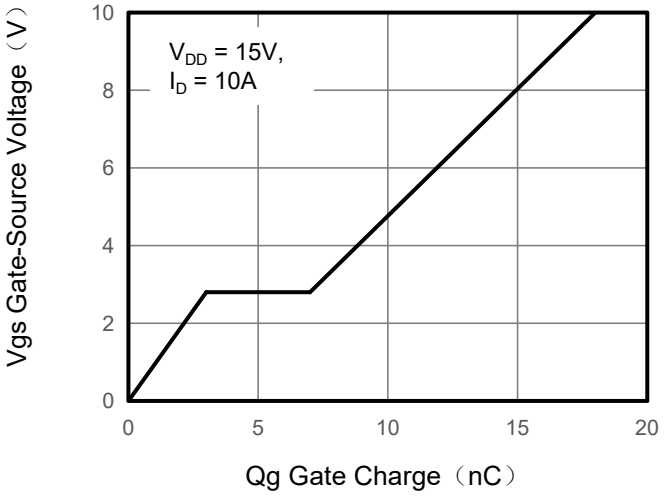


Figure 5. Capacitance

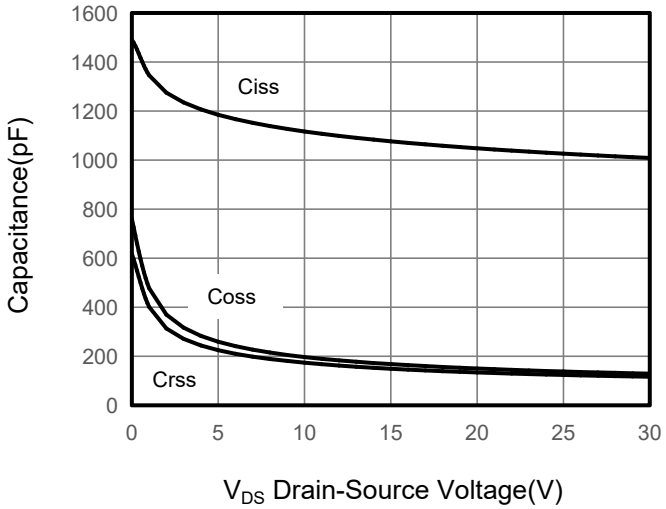
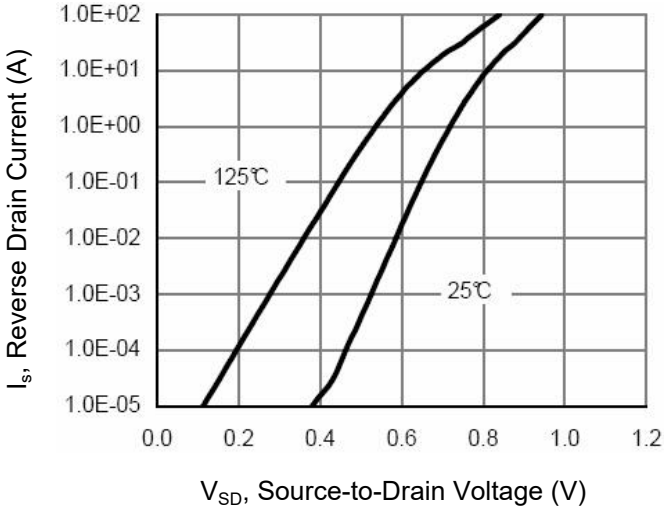


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

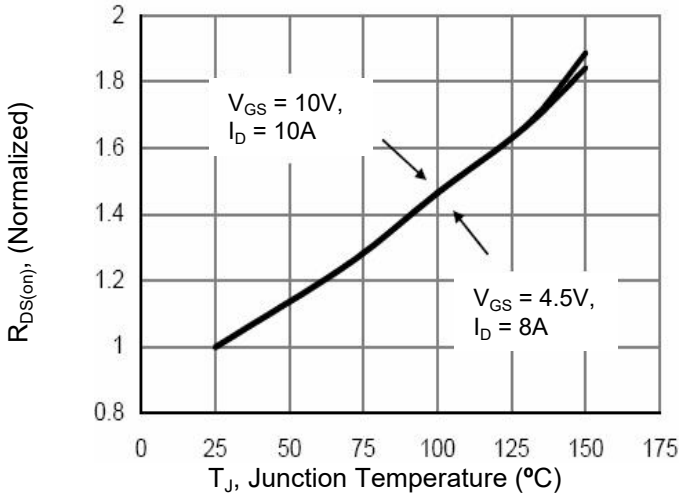


Figure 8. Safe Operation Area

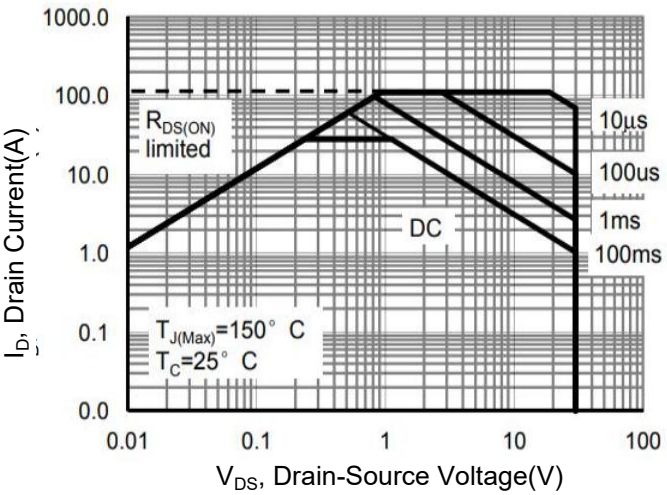
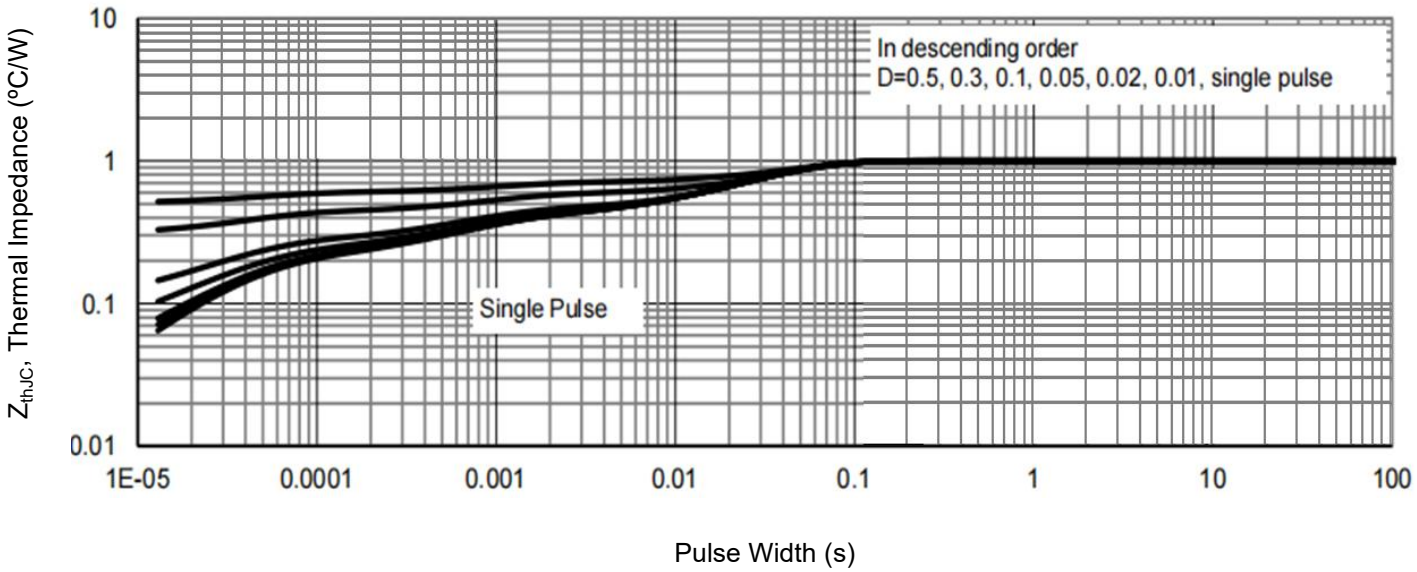


Figure 9. Normalized Maximum Transient Thermal Impedance

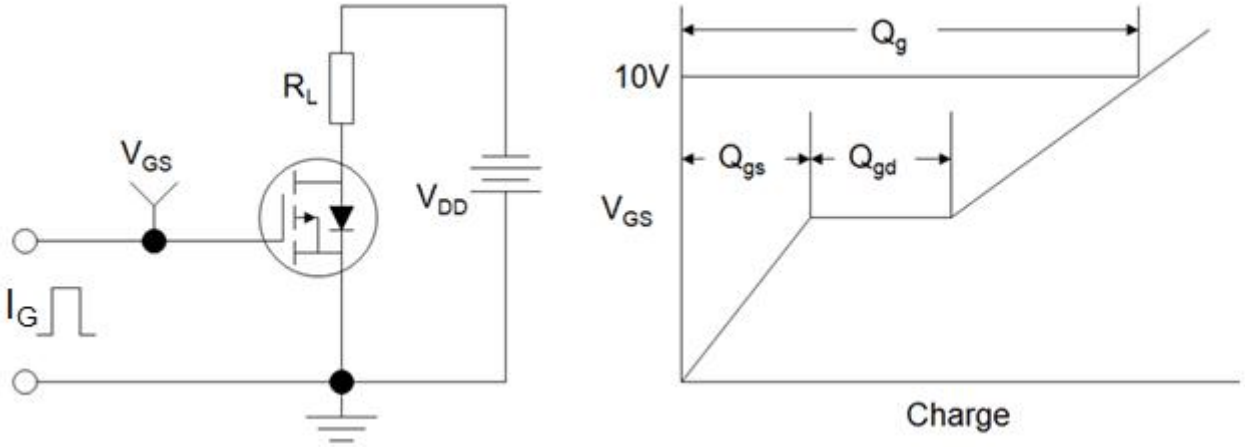


PMOS Specifications T_J = 25ºC, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1.0	-1.5	-2.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -6A	--	19	23	mΩ
		V_{GS} = -4.5V, I_D = -4A	--	26	31	
Forward Transconductance	g_{FS}	V_{DS} = -5V,I_D = -6A	--	27	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz	--	1352	--	pF
Output Capacitance	C_{oss}		--	176	--	
Reverse Transfer Capacitance	C_{rss}		--	169	--	
Total Gate Charge	Q_g	V_{DD} = -15V, I_D = -6A, V_{GS} = -10V	--	25	--	nC
Gate-Source Charge	Q_{gs}		--	3	--	
Gate-Drain Charge	Q_{gd}		--	6	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -6A, R_G = 3Ω	--	9	--	ns
Turn-on Rise Time	t_r		--	8	--	
Turn-off Delay Time	$t_{d(off)}$		--	26	--	
Turn-off Fall Time	t_f		--	8	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-12	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -6A, V_{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	I_F = -6A, V_{GS} = 0V di/dt=-500A/us	--	25	--	nC
Reverse Recovery Time	T_{rr}		--	12	--	ns

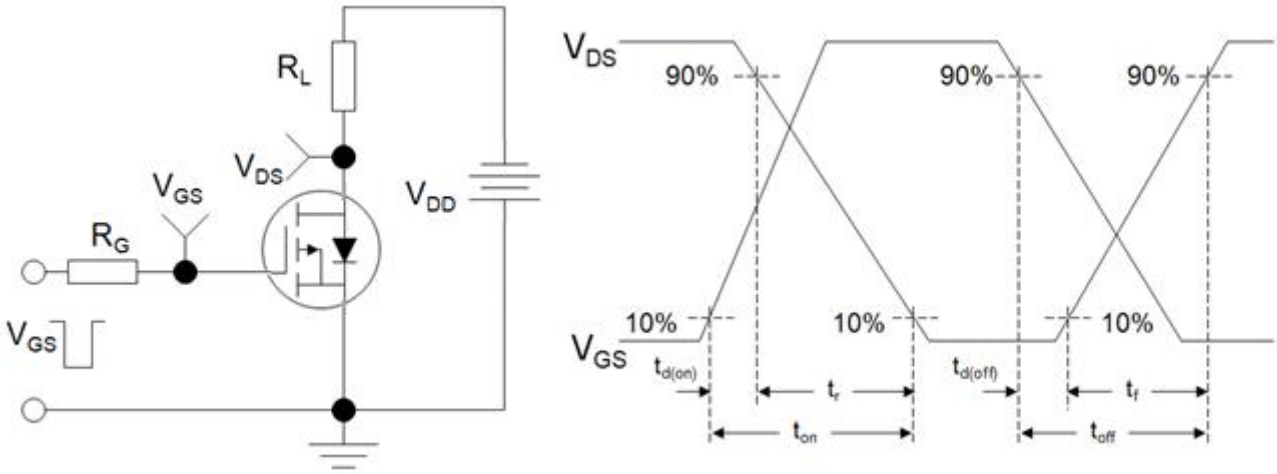
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=-30V,VGS=-10V,L=0.5mH,Rg=25Ω
3. Identical low side and high side switch with identical R_G

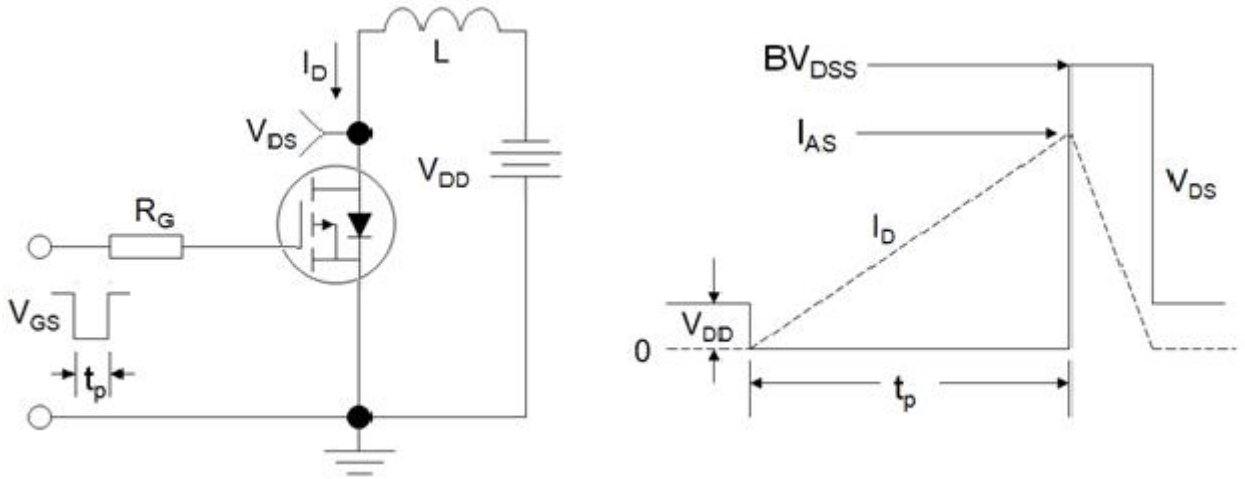
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

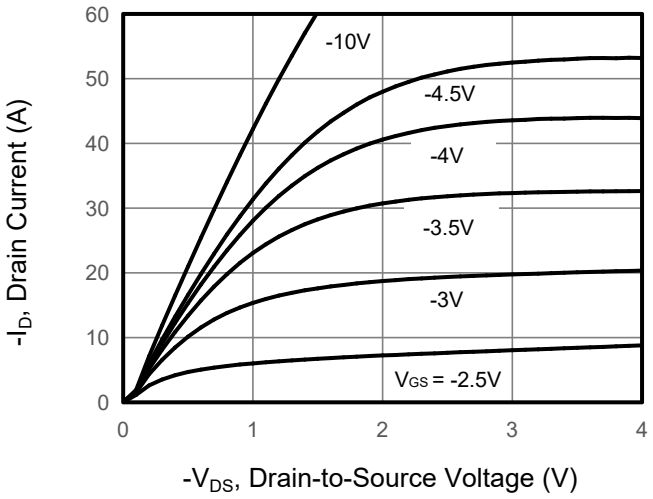


Figure 2. Transfer Characteristics

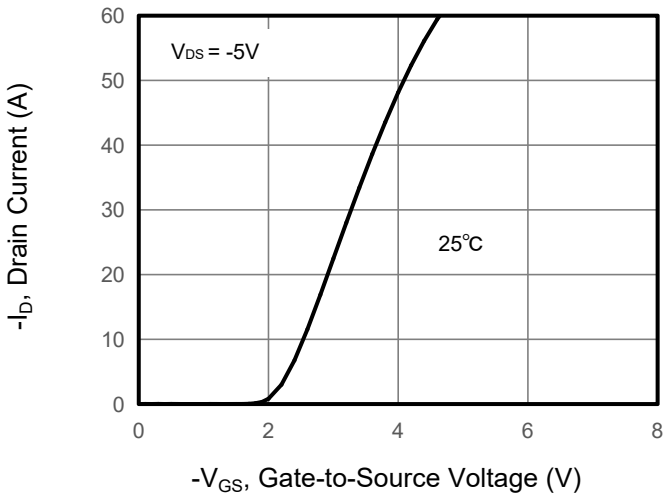


Figure 3.Drain Source On Resistance

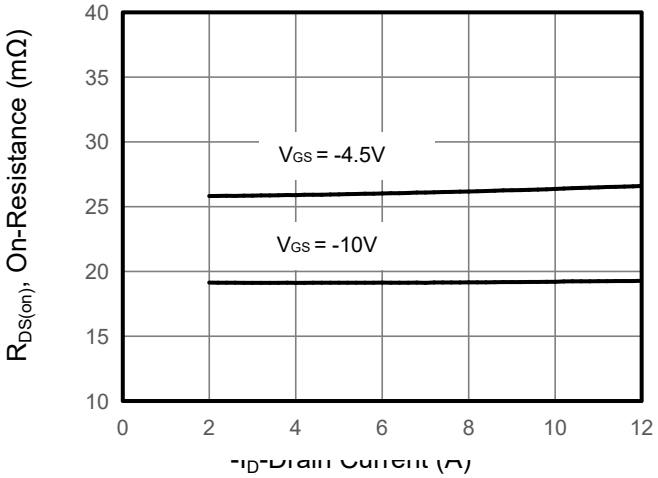


Figure 4. Gate Charge

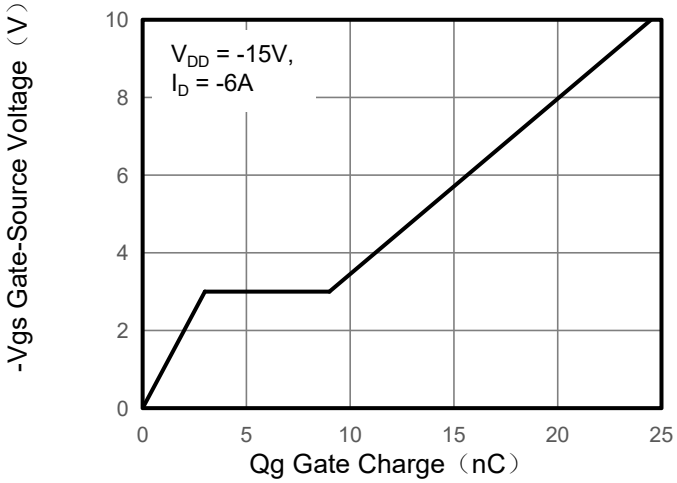


Figure 5. Capacitance

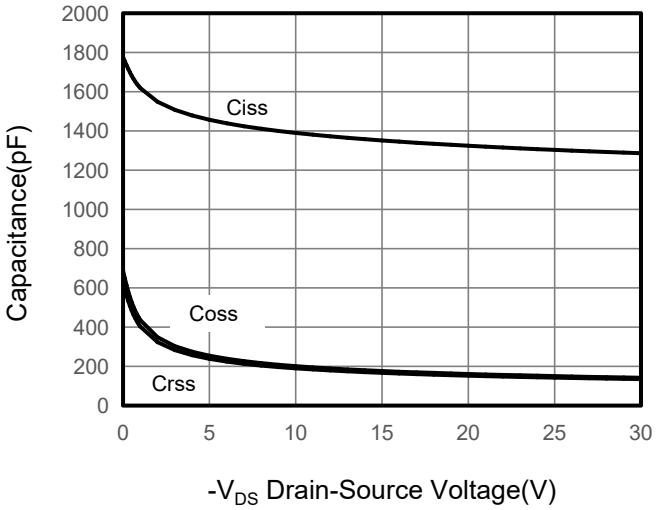
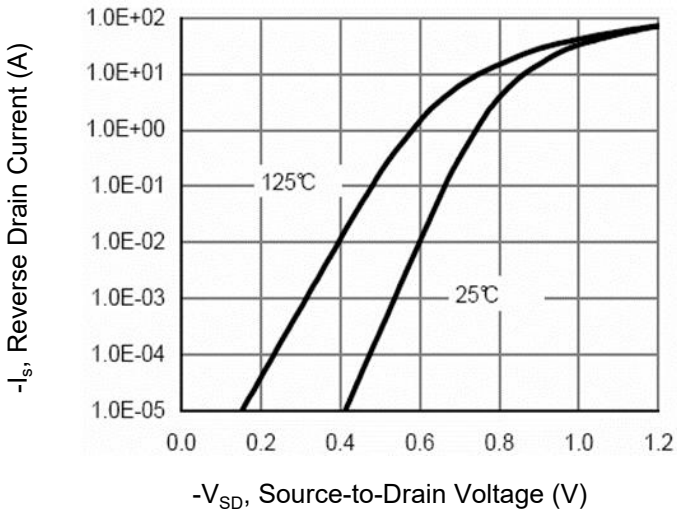


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

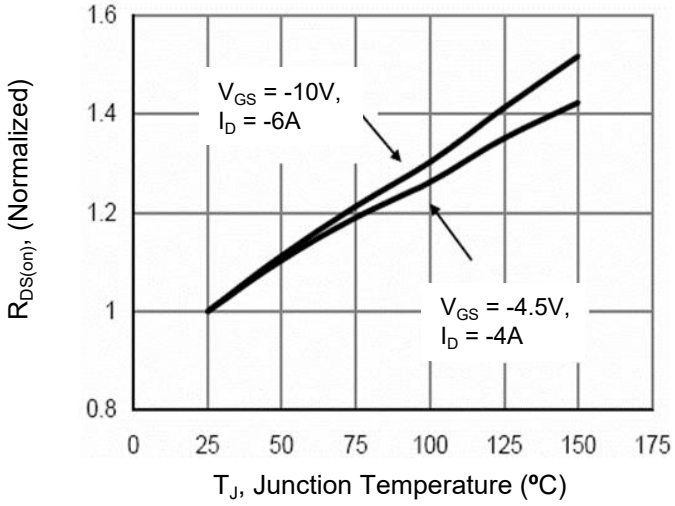


Figure 10. Safe Operation Area

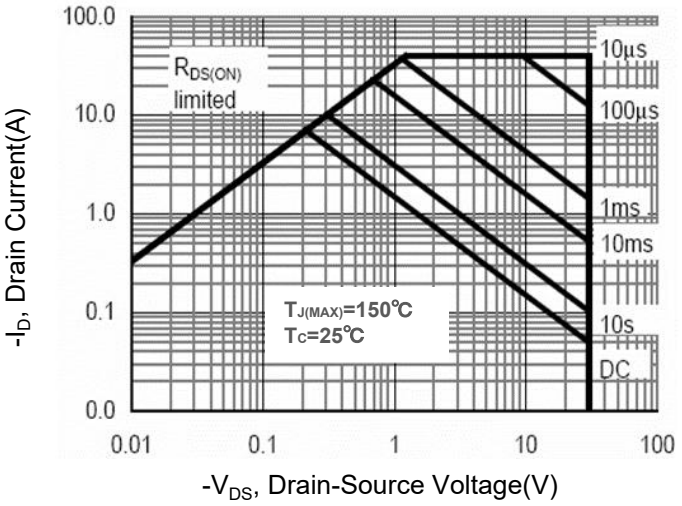
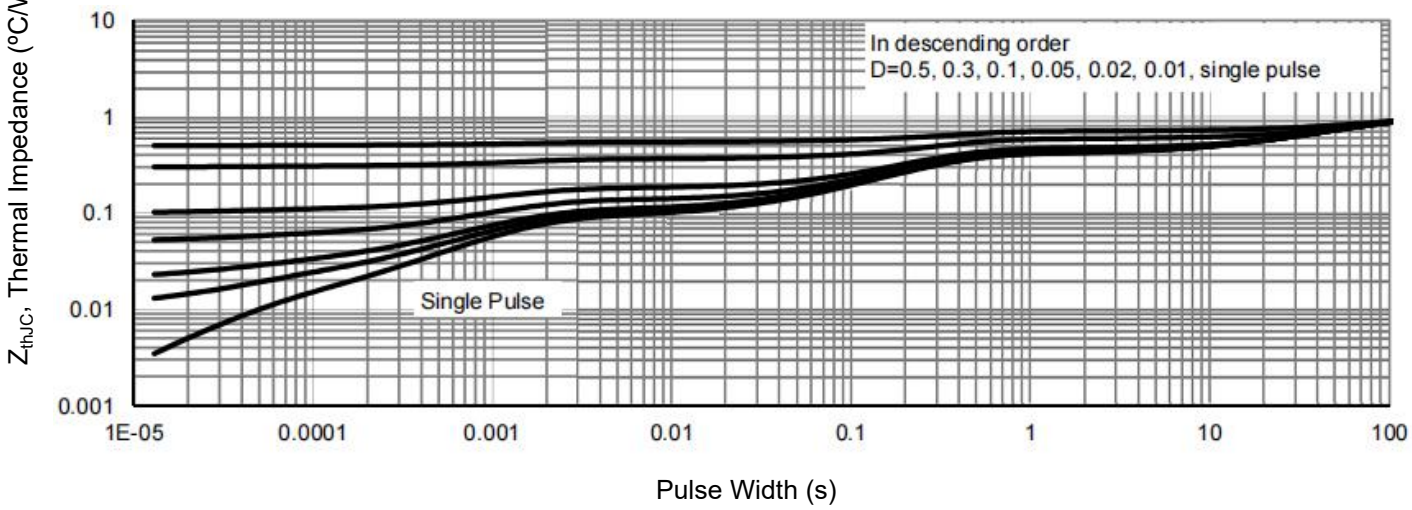
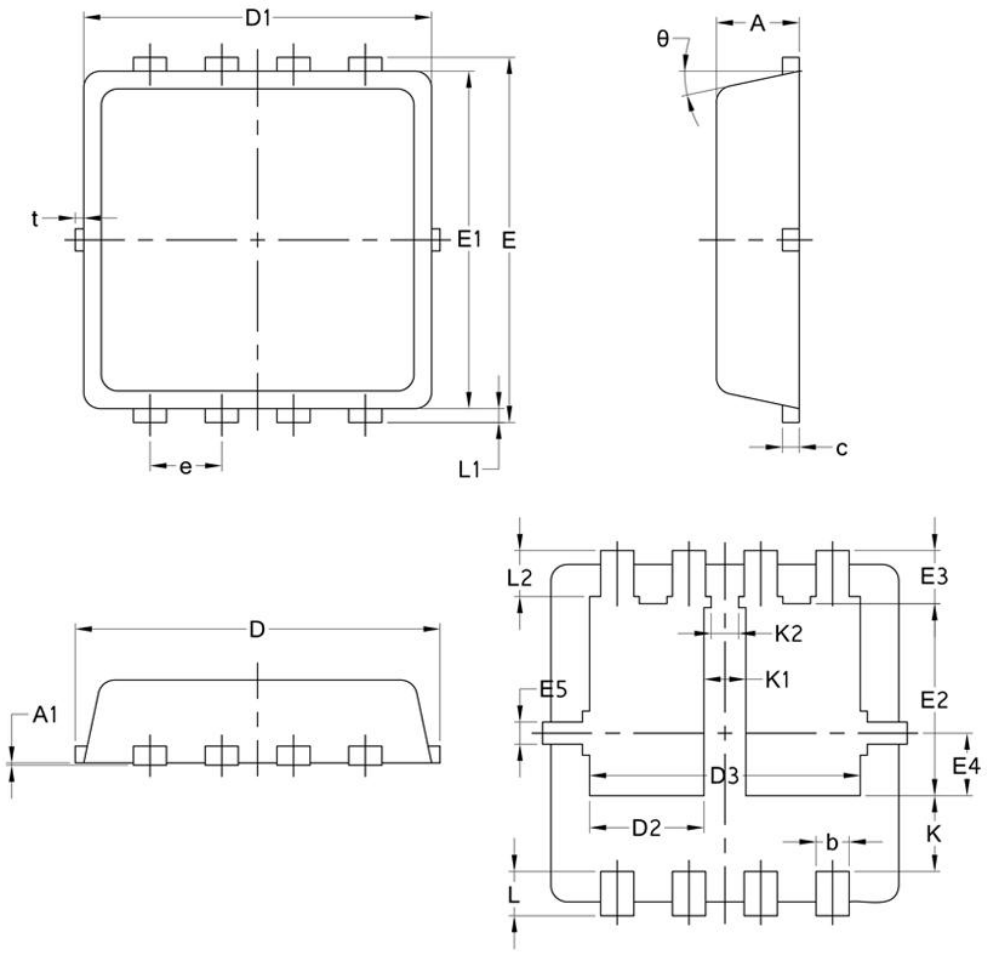


Figure 9. Normalized Maximum Transient Thermal Impedance



DFN3*3-8L Dual Package Information



SYMBOL	COMMON						
	MM						
	MIN	NOM	MAX				
A	0.70	0.75	0.85	E2	1.60	1.74	1.90
A1	/	/	0.05	E3	0.28	0.48	0.65
b	0.25	0.30	0.39	E4	0.37	0.57	0.77
c	0.14	0.152	0.20	E5	0.10	0.20	0.30
D	3.20	3.30	3.45	e	0.60	0.65	0.70
D1	3.05	3.15	3.25	K	0.50	0.69	0.80
D2	0.84	1.04	1.24	K1	0.30	0.38	0.53
D3	2.30	2.45	2.60	K2	0.15	0.25	0.35
E	3.20	3.30	3.40	L	0.30	0.40	0.50
E1	2.95	3.05	3.15	L1	0.06	0.125	0.20
θ	10°	12°	14°	L2	0.27	0.42	0.57
				t	0	0.075	0.13