

Description:

This N-Channel MOSFET uses advanced trench technology and design to provide excellent $R_{DS(on)}$ with low gate charge. It can be used in a wide variety of applications.

Features:

- 1) $V_{DS}=60V, I_D=5.5A, R_{DS(ON)}<45m\Omega @ V_{GS}=10V$
- 2) Low gate charge.
- 3) Green device available.
- 4) Advanced high cell density trench technology for ultra low $R_{DS(ON)}$.
- 5) Excellent package for good heat dissipation.

Package Marking and Ordering Information:

Part NO.	Marking	Package	Packing
DO5N06AA	5N06A	SOT-23-3	3000 pcs/Reel

Absolute Maximum Ratings: ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Units
V_{DS}	Drain-Source Voltage	60	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D	Drain Current -Continuous ¹ ($T_A=25^\circ C$)	5.5	A
	Drain Current -Continuous ¹ ($T_A=70^\circ C$)	3.5	
I_{DM}	Drain Current – Pulsed ²	15	
P_D	Power Dissipation ⁴ ($T_A=25^\circ C$)	1.8	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics:

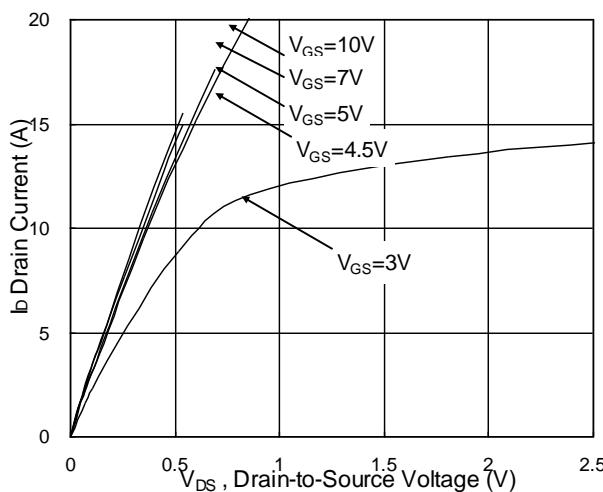
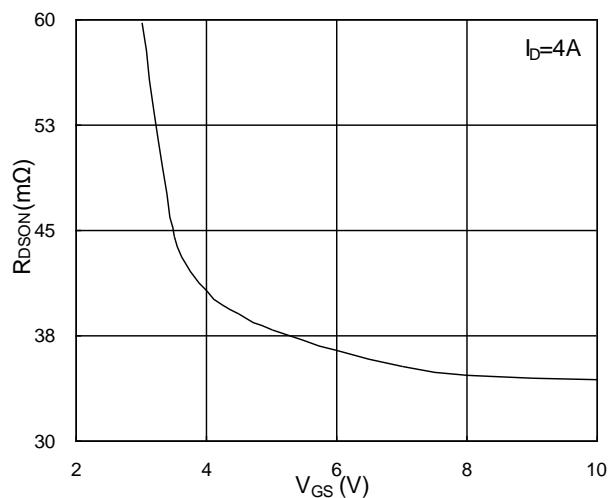
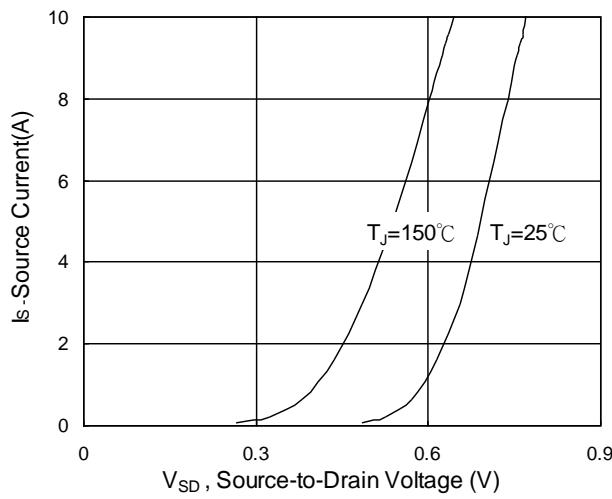
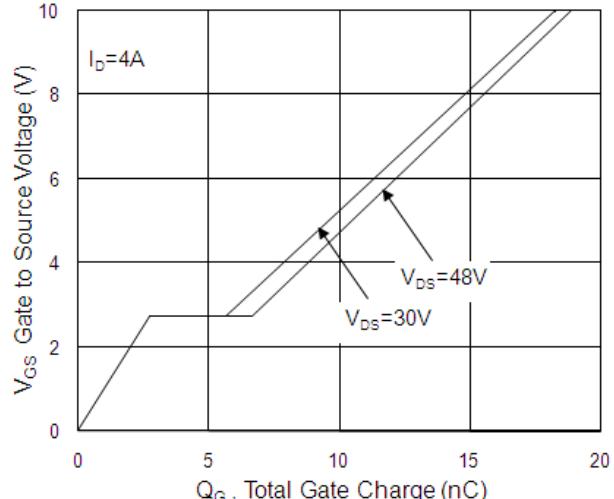
Symbol	Parameter	Max	Units
R_{eJC}	Thermal Resistance,Junction to Case ¹	25	°C/W
R_{eJA}	Thermal Resistance,Junction to Ambient ¹	69	

Electrical Characteristics: ($T_C=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250 \mu\text{A}$	60	---	---	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=48\text{V}, V_{GS}=0\text{V}, T_J=25^\circ\text{C}$	---	---	1	uA
		$V_{DS}=48\text{V}, V_{GS}=0\text{V}, T_J=55^\circ\text{C}$	---	---	5	uA
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$	---	---	± 100	nA
On Characteristics						
$V_{GS(\text{th})}$	GATE-Source Threshold Voltage	$V_{GS}=V_{DS}, I_D=250 \mu\text{A}$	1	---	2.5	V
$R_{DS(\text{ON})}$	Static Drain-Source On Resistance ²	$V_{GS}=10\text{V}, I_D=4\text{A}$	---	35	45	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=3\text{A}$	---	45	60	$\text{m}\Omega$
G_{FS}	Forward Transconductance	$V_{DS}=5\text{V}, I_D=4\text{A}$	---	28.3	---	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS}=15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	---	1000	---	pF
C_{oss}	Output Capacitance		---	60	---	
C_{rss}	Reverse Transfer Capacitance		---	45	---	
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=30\text{V}, I_D=4\text{A}$ $R_G=3.3 \Omega, V_{GS}=10\text{V}$	---	3	---	ns
t_r	Rise Time		---	34	---	ns
$t_{d(off)}$	Turn-Off Delay Time		---	23	---	ns
t_f	Fall Time		---	6	---	ns
Q_g	Total Gate Charge	$V_{GS}=10\text{V}, V_{DS}=48\text{V}, I_D=4\text{A}$	---	19	---	nC
Q_{gs}	Gate-Source Charge		---	2.6	---	nC
Q_{gd}	Gate-Drain "Miller" Charge		---	4.1	---	nC
R_G	Gate Resistance	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	---	2.5	---	Ω
Drain-Source Diode Characteristics						
V_{SD}	Source-Drain Diode Forward Voltage ²	$V_{GS}=0\text{V}, I_S=1\text{A}, T_J=25^\circ\text{C}$	---	---	1.2	V
I_s	Continuous Source Current ^{1,5}	$V_G=V_D=0\text{V}, \text{Force Current}$	---	---	5.5	A
I_{SM}	Pulsed Source Current ^{2,5}		---	---	15	A
Tr_r	Body Diode Reverse Recovery Time	$I_F=4\text{A}, dI/dt=100\text{A}/\mu\text{s}, T_J=25^\circ\text{C}$	---	12.1	---	Ns
Q_{rr}	Body Diode Reverse Recovery Charge		---	6.7	---	Nc

Notes:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%
- 3.The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=21A$
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics: (T_C=25°C unless otherwise noted)

Fig.1 Typical Output Characteristics

Fig.2 On-Resistance vs. Gate-Source

Fig.3 Forward Characteristics Of Reverse

Fig.4 Gate-Charge Characteristics

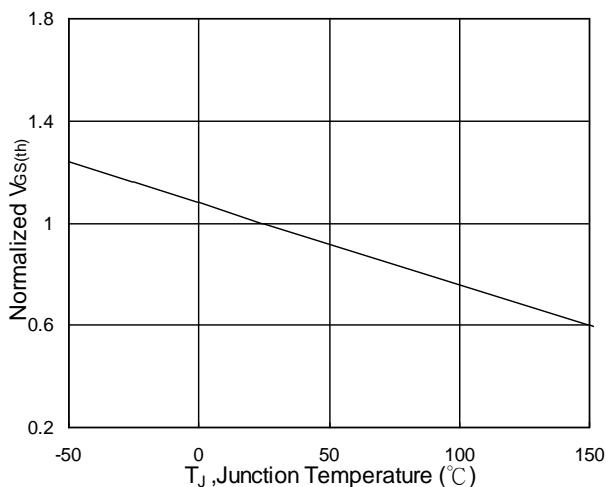
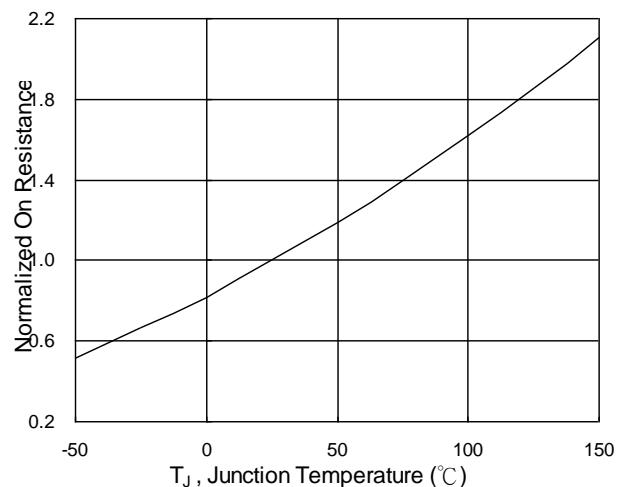
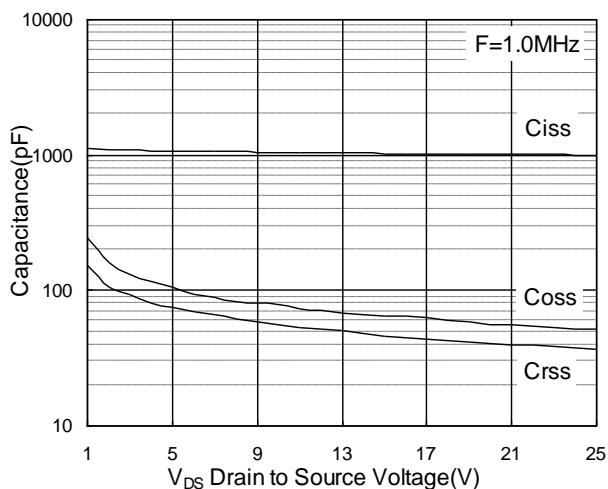
Fig.5 Normalized $V_{GS(th)}$ vs. T_J Fig.6 Normalized $R_{DS(on)}$ vs. T_J 

Fig.7 Capacitance

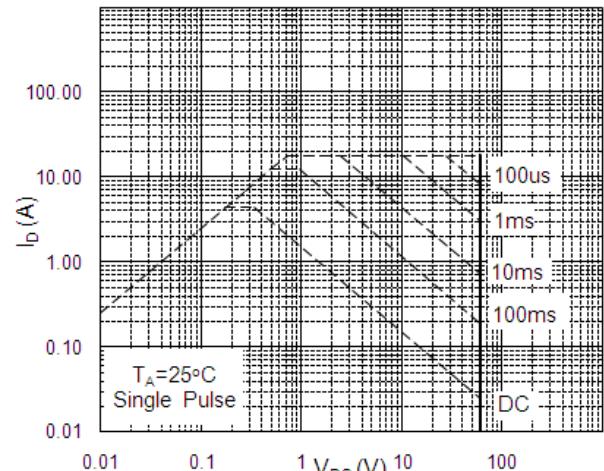


Fig.8 Safe Operating Area

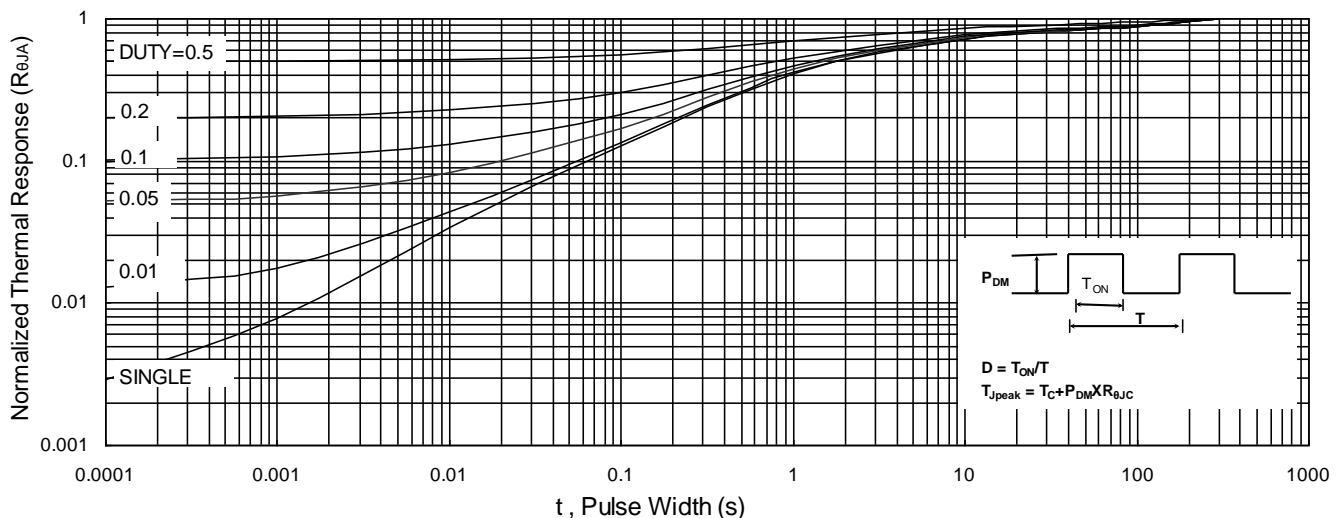
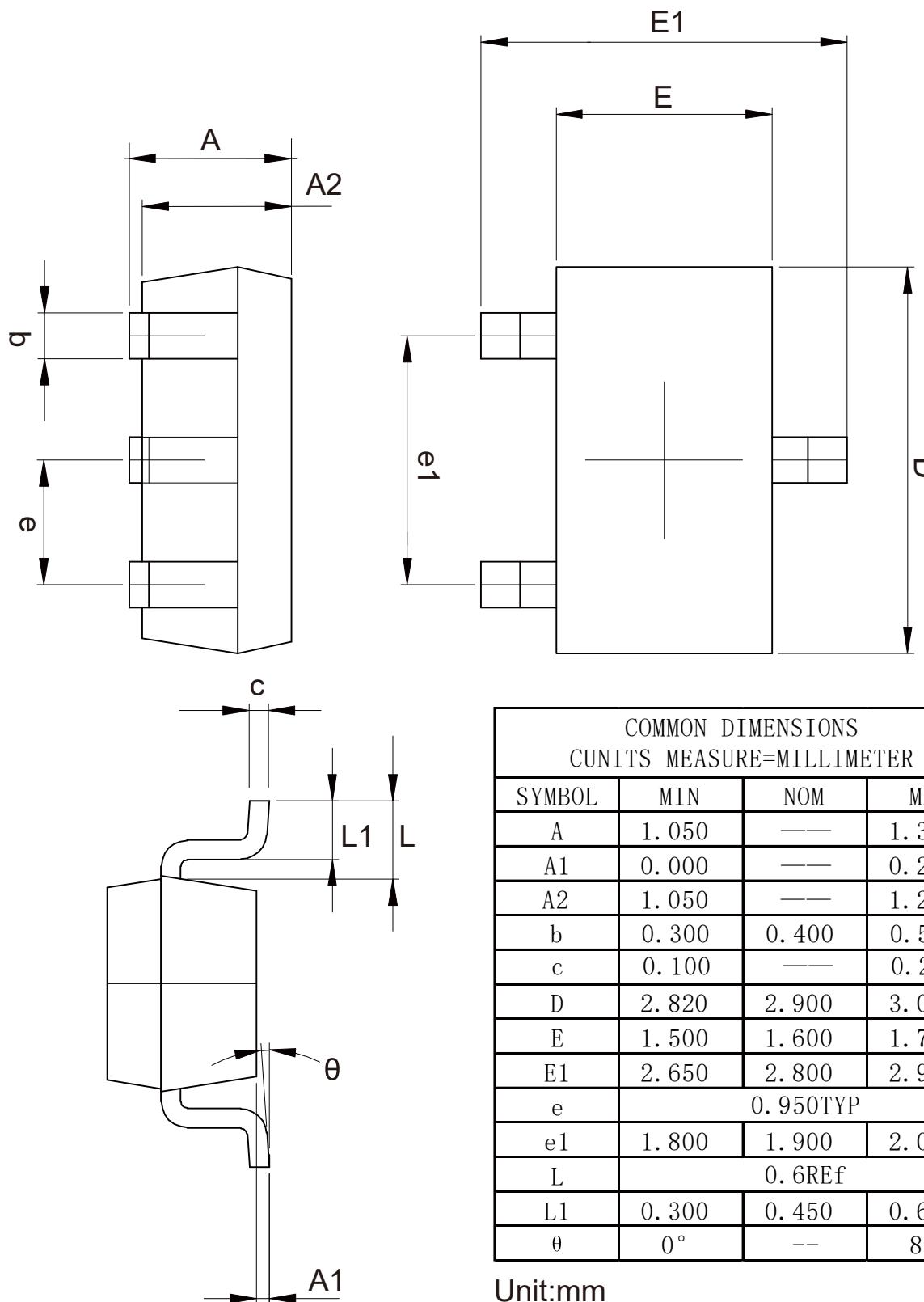
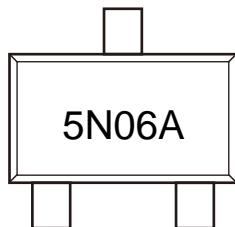


Fig.9 Normalized Maximum Transient Thermal Impedance

SOT-23-3Package Outline Data


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