Himax Imaging, Ltd.

DATA SHEET

(DOC No. HM0360-DS)

HM0360

1/6″ 640 x 480 ▪ VGA 60FPS CMOS Image Sensor

Preliminary version 04 May, 2020

Himax Imaging, Ltd.

HM0360 Ultra Low Power AoS™

1/6″ 640 x 480 ▪ VGA 60FPS CMOS Image Sensor

Himax Imaging, Ltd.
http://www.himax.com.tw

May, 2020

Features

- Ultra Low Power, high sensitivity, low noise VGA sensor
- Operates 7.8mA VGA 60 FPS down to 240µA in monitor mode
- Automatic wake and sleep operation with programmable event interrupt to wake host processor
- On chip high precision oscillator, auto exposure / gain, ambient light sensor and zone detection
- Metered exposure provides well exposed first frame and after extended sleep **(blanking)** period
- External frame synch and stereo camera support
- Flexible binning, subsampling and region of interest
- Embedded line provides metadata frame, AE statistics, zone trigger and other interrupt event information
- On-chip high precision oscillator and LDO
- 1-lane MIPI CSI2 and 8-bit parallel/serial data format that supports 1-bit, 4-bit and 8-bit protocol
- I2C 2-wrie serial interface supporting burst operation for fast register access
- < 13 mm^2 CSP sensor package option
- High CRA for low profile module design

Key Parameters

Sensor parameters	Value
Pixel Array **(Full/ Active)**	656 x 496 / 640 x 480
Pixel Size	3.6µm x 3.6µm / BSI
Image Diagonal	2.88mm **(1/6")**
Color Filter Array	Bayer, Monochrome
Shutter Type	Electronic Rolling Shutter
Frame Rate @ 24MHz	QQVGA 1 FPS to VGA 60 FPS
Readout Modes	Full, VGA, Bin2 / Sub2, Bin4 / Sub4, Fast ROI
S/N Ratio **(Max.)**	45.5 dB
Dynamic Range **(1x)**	TBD dB
Sensitivity	5.5V / Lux-sec @530nm 15V / (µW-sec/cm^2) @850nm
Pixel CRA **(Max.)**	35.74°

Sensor parameters		Value	
Supply Voltage	AVDD	2.8V	
	DVDD	1.2V **(Internal LDO)**	
	IOVDD	1.8V / 2.8V	
Input Reference Clock		6 – 24MHz	
Internal Oscillator		48MHz	
Serial Interface		I2C **(1MHz max. single / burst)**	
MIPI Data Format		8-bit	
Parallel / Serial data format		8-bit, 4-bit+4-bit / 4-bit / 1-bit	
Current Consumption **(8-bit parallel interface, Typical)**		QVGA **(S2)** 2FPS	140 µA
		QVGA 60FPS	3.2 mA
		VGA 60FPS	7.8 mA

Order Information

Part no.	Color option	Operating / Storage temperature	Package
HM0360-AWA	RGB	- 20 ºC to 85 ºC / - 30 ºC to 85 ºC	CSP
HM0360-MWA	Mono	- 20 ºC to 85 ºC / - 30 ºC to 85 ºC	CSP

Revision History

May, 2020

Version	Date	Description of changes
01	2019/04/30	New setup.
02	2019/08/21	Page 2 1. Modify 'Key Parameters' Page 10 2. Modify 'Table 1.1: CSP pin description'. Page 13 3. Modify CH '3.3 Sub-sampling and binning readout'. Page 17 4. Modify 'Table 4.2: Motion Detection (MD) block'. 5. Modify 'Figure 4.4: Example for VGA effective ROI area and map'. Page 23 6. Modify CH '5.1.1 External LDO mode (CSP)'. Page 24 7. Modify CH '5.2.1 Internal LDO mode (CSP)'. Page 28 8. Modify Figure '6.4 Clock dividers'. Page 29 9. Modify Table '6.3 IO control options'. 10. Modify Table '6.4 Output pin status'. Page 51 11. Modify CH '10.22 IO and clock control registers [0x3094 – 0x3128]'. Page 59 12. Modify 'Table 11.3: DC characteristics'. Page 65 13. Add CH '13. Quantum Efficiency (QE)'.
03	2020/04/15	Page 2 1. Modify 'Features'. 2. Modify 'Key Parameters'. Page 11 3. Modify 'Figure 1.1: CSP pin diagram (Top view)'. Page 13 4. Modify CH '2. Sensor Overview'. Page 14 5. Modify CH '3.1 Sensor array'. 6. Modify 'Figure 3.2: VGA resolution pixel readout'. Page 15 7. Modify CH '3.3 Sub-sampling and binning readout'. Page 16 8. Modify 'Figure 3.6: VGA ROI window readout with parallel interface'. Page 17 9. Modify 'Figure 4.1: ISP and digital function blocks'. Page 18 10. Modify 'Table 4.1: ISP and digital block description'. Page 19 11. Modify CH '4.1 Motion Detection (MD)'. **(Remove 'Figure 4.3: Motion detect configuration')** Page 20 12. Modify CH '4.2 Strobe control'. Page 21 13. Modify CH '4.4 Context switch'.

Revision History

May, 2020

Version	Date	Description of changes
		Page 22 14. Modify 'Table 4.3: Interrupt control'. Page 23 15. Modify CH '4.6 AEGC'. Page 24 16. Modify CH '4.7 One Time Programming (OTP) memory'. 17. Add CH '4.8 Pre-meter'. Page 25 18. Add CH '4.9 Embedded data'. Page 26 19. Add CH '4.10 Tone mapping'. Page 29 20. Modify 'Table 6.1: Operating modes'. Page 30 21. Modify 'Figure 6.1: State diagram (Software I2C trigger)'. 22. Modify 'Figure 6.2: State diagram (Hardware pin trigger)'. Page 32 23. Modify 'Table 6.2: Power up sequence timing'. Page 33 24. Modify 'Figure 6.4: Clock dividers'. Page 37~38 25. Add CH '6.7 Multiple camera application'. Page 39 26. Modify 'Figure 7.1: MIPI interface lane'. Page 44 27. Modify CH '9.2 Analog gain control'. Page 46 28. Modify CH ,10.1 Sensor ID registers [0x0000 – 0x0007]'. Page 48 29. Modify CH ' 10.8 Test pattern control registers [0x0601 – 0x0609]'. 30. Modify CH '10.9 Black level control registers [0x1000 – 0x1009]'. Page 49 31. Modify CH '10.10 Monochrome programming registers [0x100A]'. 32. Add CH '10.12 Tone mapping registers [0x1030 – 0x103F]'. Page 50 33. Modify CH '10.13 Automatic exposure programming registers [0x2000 – 0x2072]'. Page 54~55 34. Modify CH '10.15 Motion detection control registers [0x2080 – 0x20C0]'. Page 56 35. Modify CH '10.20 Operation mode registers [0x3026 – 0x302A]'. Page 58 36. Modify CH '10.22 Strobe control registers [0x3080 – 0x3089]'. Page 59 37. Modify CH '10.23 IO and clock control registers [0x3094 – 0x3128]'. Page 60~62 38. Modify CH '10.25 Context switch A registers [0x3500 – 0x3559]'. Page 63~65 39. Modify CH '10.26 Context switch B registers [0x355A – 0x35B3]'.

Revision History

May, 2020

Version	Date	Description of changes
		Page 67~68 40. Modify CH '11.3 DC characteristics'. Page 71 41. Modify 'Figure 11.2: 8-bit parallel video interface timing diagram'. 42. Modify 'Figure 11.3: 4-bit parallel video interface timing diagram'. Page 72 43. Modify 'Figure 11.4: Serial video interface timing diagram'.
04	2020/05/29	Page 2 1. Modify 'Features'. Page 13 2. Modify CH '2. Sensor Overview'. Page 22 3. Modify 'Table 4.3: Interrupt control'. Page 25 4. Modify 'Table 4.4: Embedded Data Content page'. Page 33 5. Modify 'Figure 6.4: Clock dividers'. Page 47 6. Modify CH '10.4 Clock control registers [0x0300 – 0x0302]'. 7. Modify CH '10.6 Monochrome programming registers [0x0370 – 0x0372]'. Page 50~52 8. Modify CH '10.13 Automatic exposure programming registers [0x2000 – 0x2072]'. Page 53 9. Modify CH '10.14 Interrupt programming registers [0x2061 – 0x2065]'. Page 54~55 10. Modify CH '10.15 Motion detection control registers [0x2080 – 0x20C0]'. Page 56~57 11. Modify CH '10.16 OTP programming registers [0x2500 – 0x25FF]'. Page 61 12. Modify CH '10.23 IO and clock control registers [0x3094 – 0x3128]'. Page 62~64 13. Modify CH '10.25 Context switch A registers [0x3500 – 0x3559]'. Page 65~67 14. Modify CH '10.26 Context switch B registers [0x355A – 0x35B3]'. Page 71 15. Modify 'Table 11.5: MIPI timing characteristics'. Page 73 16. Modify 'Table 11.8: 8-bit parallel video interface timing'. 17. Modify 'Table 11.9: 4-bit parallel video interface timing'. Page 74 18. Modify 'Table 11.10: Serial video interface timing'.

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1. Package Information

1.1 Chip Scale Package (CSP)

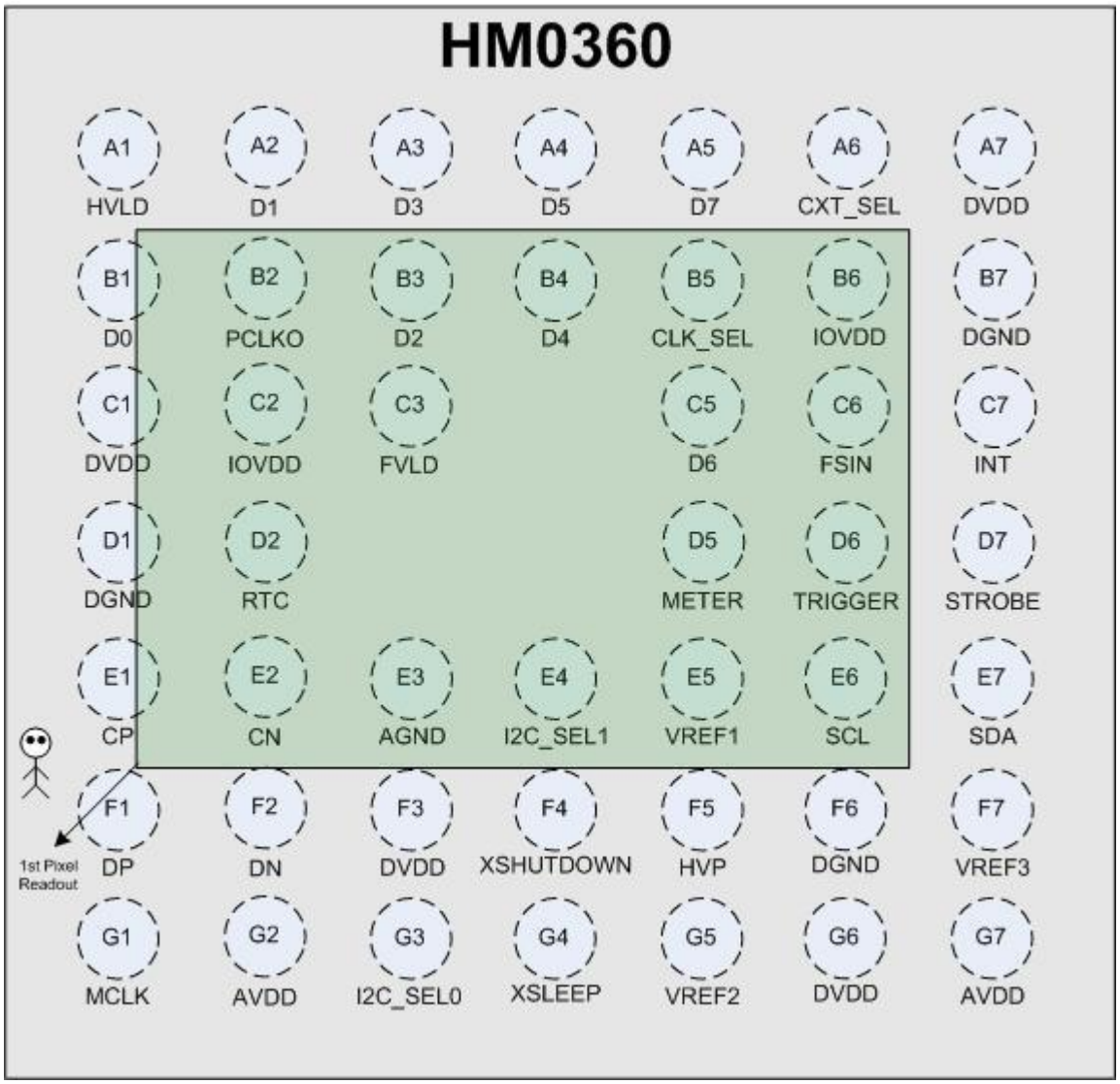


Figure 1.1: CSP pin diagram (Top view)

Pin no.	Pin name	Type	Description
A1	HVLD	Out	Line valid output.
A2	D1	Out	Data 1 output.
A3	D3	Out	Data 3 output.
A4	D5	Out	Data 5 output.
A5	D7	Out	Data 7 output.
A6	CXT_SEL	In	Context switching selection. **(Internal pull low)**
A7	DVDD	Power	Digital power. **(1.2V)**
B1	D0	Out	Data 0 output.
B2	PCLKO	Out	Pixel clock output.
B3	D2	Out	Data 2 output.
B4	D4	Out	Data 4 output.
B5	CLK_SEL	In	Clock source select. **(Internal pull low, Low: Oscillator, High: MCLK, connect to ground for oscillator mode)**
B6	IOVDD	Power	IO power. **(1.8V / 2.8V)**
B7	DGND	Ground	Digital ground.
C1	DVDD	Power	Digital power. **(1.2V)**
C2	IOVDD	Power	IO power. **(1.8V / 2.8V)**
C3	FVLD	Out	Frame valid output.
C5	D6	Out	Data 6 output.
C6	FSIN	In	Frame sync. **(Internal pull low)**
C7	INT	Out	Interrupt output. **(Active high)**
D1	DGND	Ground	Digital ground.
D2	RTC	In	Real time clock source input. **(Must not be left floating, connected to DGND without RTC clock input)**
D5	METER	In	Exposure Meter enable pin. **(Internal pull low / Active high)**
D6	TRIGGER	In	Frame trigger input. **(Internal pull low / Active high)**
D7	STROBE	Out	Strobe output.
E1	CP	Out	MIPI clock positive output.
E2	CN	Out	MIPI clock negative output.
E3	AGND	Ground	Analog ground.
E4	I2C_SEL1	In	I2C device address selection. **(Internal pulling low)**
E5	VREF1	Reference	Voltage reference. **(VRNP)**
E6	SCL	In	I2C serial clock.
E7	SDA	In/Out	Serial data I/O. **(Open drain)**
F1	DP	Out	MIPI data positive output.
F2	DN	Out	MIPI data negative output.
F3	DVDD	Power	Digital power. **(1.2V)**
F4	XSHUTDOWN	In	Reset and power down control pin. **(Active low)**
F5	HVP	Reference	Place an external capacitor if the internal OTP pump is used.
F6	DGND	Ground	Digital ground.
F7	VREF3	Reference	Voltage reference. **(PVDD)**
G1	MCLK	In	Master clock input. **(Connected to DGND when using internal oscillator)**
G2	AVDD	Power	Analog power. **(2.8V)**
G3	I2C_SEL0	In	I2C device address selection. **(Internal pulling low)**
G4	XSLEEP	In	Low power sleep mode. **(Active low)**
G5	VREF2	Reference	Voltage reference. **(VRPP)**
G6	DVDD	Power	Digital power. **(1.2V)**
G7	AVDD	Power	Analog power. **(2.8V)**

Table 1.1: CSP pin description

2. Sensor Overview

The HM0360 is an ultra-low power, Back Side Illuminated **(BSI)** CMOS image sensor designed for energy efficient smart vision applications, such as object-specific classification, tracking and identification. The advanced 3.6µ low noise, deep diode pixel achieves superior image quality performance to enable monitoring, detection and video capture in low light environments while minimizing the use of external, power consuming, LED illuminators.

The HM0360 Always On Sensor architecture delivers a target current consumption of 240µA in AoS monitor mode and 7.8mA in VGA 60 frames per second read out mode. In order to reduce host processor loading, camera latency and system power consumption, the HM0360 features on-chip oscillator with automatic external reference clock detection, automatic frame mode switch, fast sensor initialization, <2ms frame trigger time, context switching and instant frame update. The sensor offers several monitoring options with programmable interrupt thereby allowing the host processor to be placed in low power standby until notified by the sensor.

The HM0360 is available in a compact Chip Scale Package **(CSP)** compatible with standard SMT reflow process. The sensor supports multiple power supply configurations and uses few passive components to enable a highly compact camera module design for next generation energy efficient, smart camera devices.

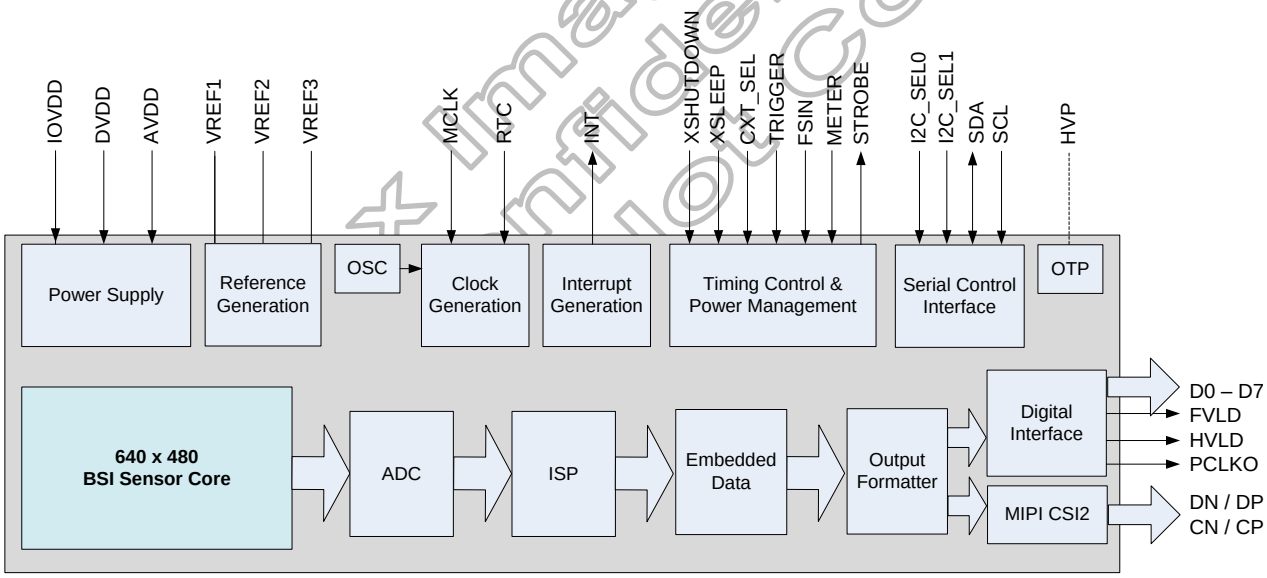


Figure 2.1: HM0360 block diagram

3. Sensor Core and Function Description

3.1 Sensor array

The HM0360 consists of full pixel array of 656 columns and 496 rows. The sensor maximum active resolution is 640 columns and 480 rows which include 16 border pixels.

For the sensors with color filter, the even numbered rows contain the Blue **(B)** and Green **(G_1)** pixel, and the odd numbered rows contain the Red **(R)** and Green **(G_2)** pixels; the even numbered columns contain the Green **(G_2)** and Blue **(B)** pixels, and the odd numbered columns contain the Red **(R)** and Green **(G_1)** pixels. Optically black rows are used by the sensor for black level calibration and masked out from the data output. Programmable horizontal and vertical blanking time adjusts the line length and frame height, respectively.

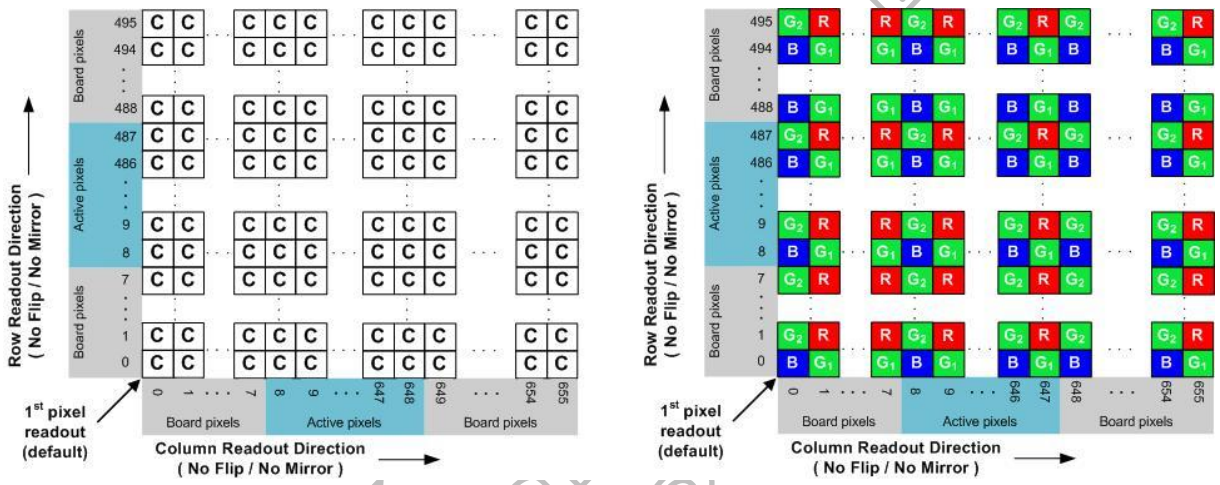


Figure 3.1: Full resolution pixel readout

3.2 VGA window readout

The HM0360 full active pixel array of 656 x 496 can be windowed to 640 x 480 by register **0x3030[0]**.

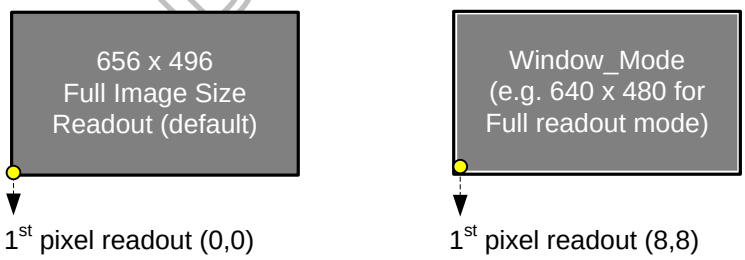


Figure 3.2: VGA resolution pixel readout

3.3 Sub-sampling and binning readout

HM0360 supports Quad and Channel sub-sampling and Quad binning readout for sub2 and sub4 for both Bayer RGB and Monochrome sensor CFA. The sub-sampling readout can be used to reduce sensor resolution while preserving the field of view. The binning readout improves S/N ratio. The sub-sampling and binning modes can be configured in the main and context register banks.

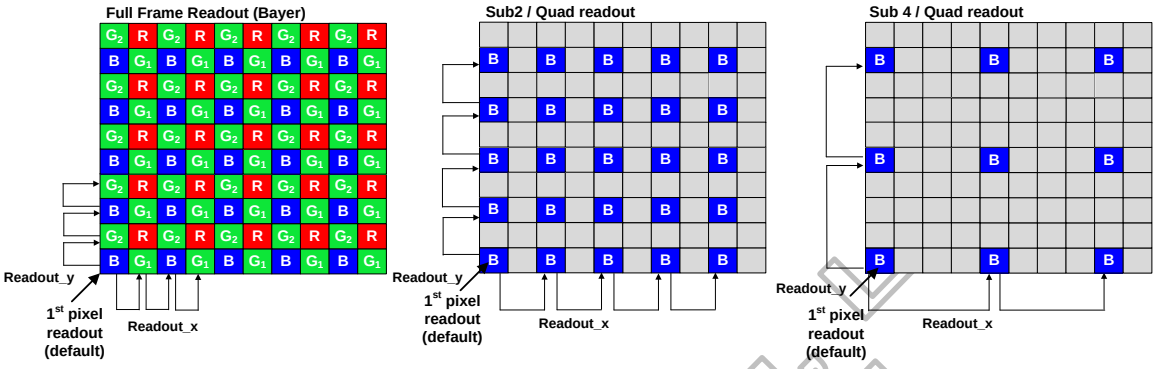


Figure 3.3: Quad mode subsampling (RGB shown)

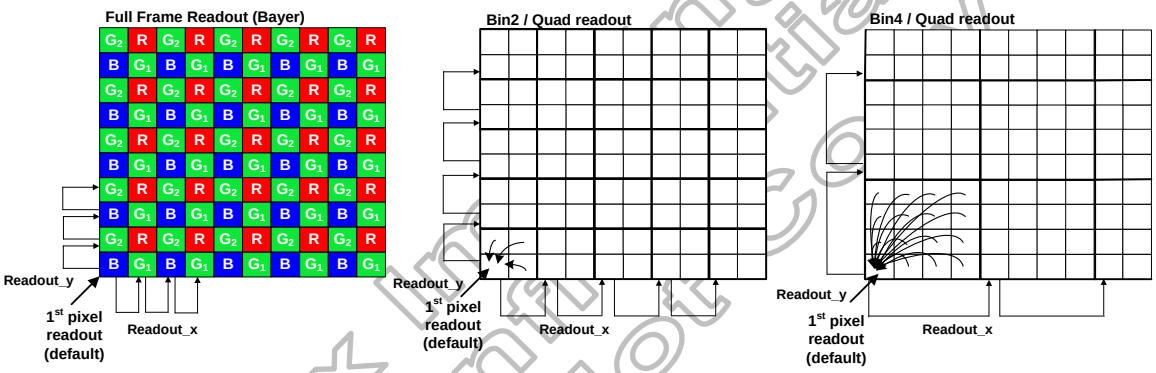


Figure 3.4: Quad mode binning (RGB shown)

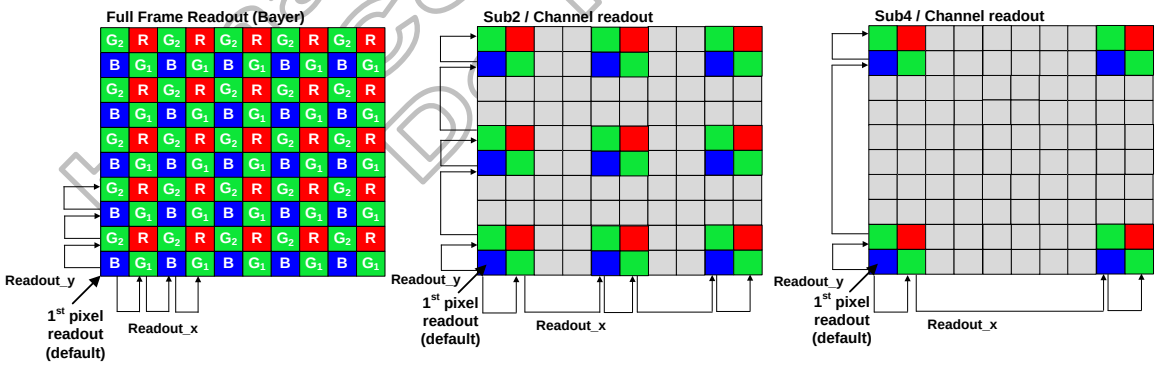


Figure 3.5: Channel mode subsampling (RGB shown)

3.4 Region of Interest (ROI)

The HM0360 supports Region of Interest **(ROI)** window readout mode. The array is partitioned into 10**(H)** x 15**(V)** independently addressable ROI blocks. As shown in the ROI example below, the ROI selection is independent, and the frame timing will need to be programmed and adjusted based on the selected active region as shown the Figure 3.6. The resolution of each ROI block is scaled based on the binning / subsampling mode as described in Table 3.1.

Window readout	Maximum number of ROI	ROI size
VGA **(640 x 480)**	10 x 15	64 x 32
QVGA **(320 x 240)**	10 x 15	32 x 16
QQVGA **(160 x 120)**	10 x 15	16 x 8

Table 3.1: Region of Interest (ROI) block

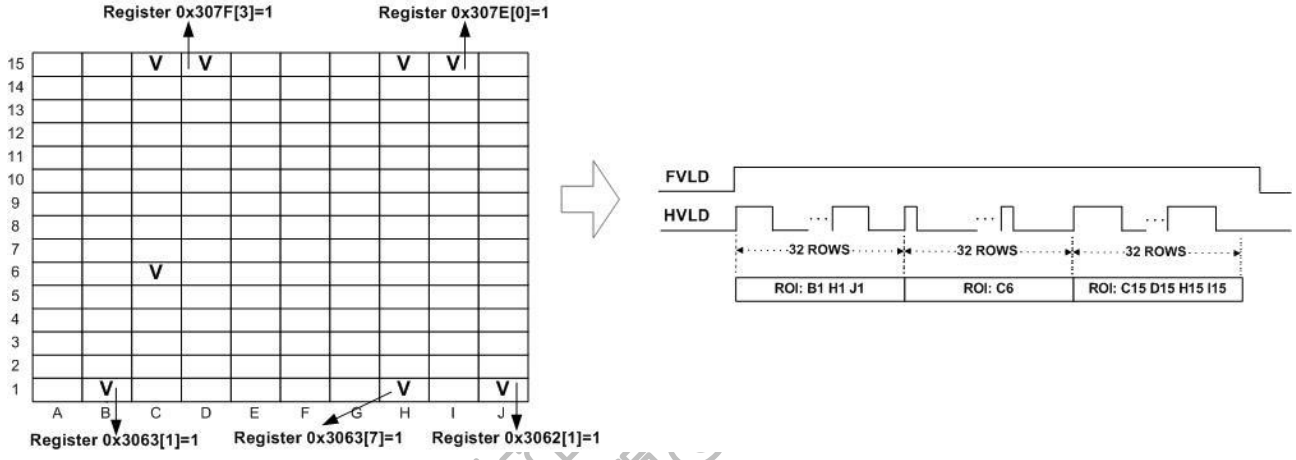


Figure 3.6: VGA ROI window readout with parallel interface

3.5 Horizontal and vertical mirror

The sensor readout can be mirrored in the vertical and horizontal direction where the window center will remain unchanged. The horizontal and vertical mirror readout can be applied in VGA, QVGA **(sub2 or bin2)**, QQVGA **(sub4 or bin4)**, and ROI modes.

In the color sensor version, the color of the first pixel read out will change according to the selected mirror mode as shown in the Figure 3.7.

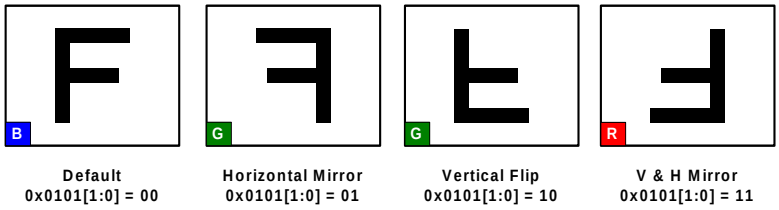


Figure 3.7: Horizontal and vertical mirror readout modes

4. Image Signal Processor Functional Description

The sensor ISP features can be configured by the host through the serial register interface. Please contact Himax Imaging for application notes.

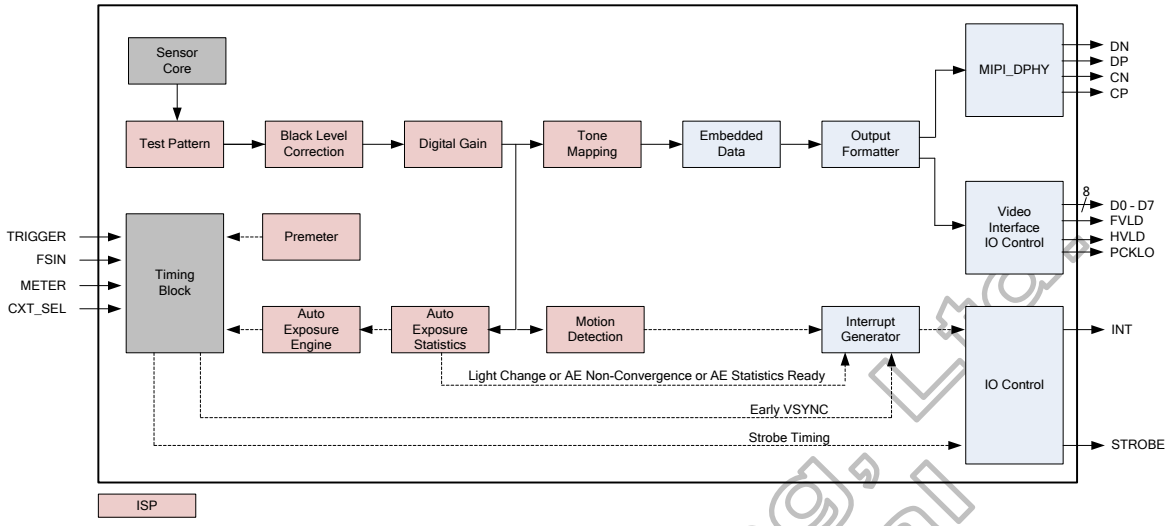


Figure 4.1: ISP and digital function blocks

Block	Digital function	Description	Register range	Register enable bit
ISP	Test Pattern	Five test patterns are supported **(See Figure 4.2)**: a. Color Bar b. FADE To Grey Color Bar c. Walking 1's d. Solid Pattern e. PN9	0x0601~ 0x0609	0x0601[6:4]
	Black Level Correction	Adjusts the black level to the target programmed value based on optical black pixel data	0x1000~ 0x1009	-
	Digital Gain	Global digital gain applied to the video data. Programmed in 2.6 format **(2-bit integer, 6-bit floating)**	0x0202~ 0x020F	0x020E[1:0] 0x020F[7:2]
	Tone mapping	Preserving image detail for monochrome sensor.	0x1030~ 0x103F	-
	Motion Detection	Detect for presence of motion within programmable motion region. The status of the motion detection, including triggered interrupt can be accessed through the registers or embedded data line.	0x2080~ 0x20C0	0x2080[0]
	Automatic Exposure Gain	Control loop which adjusts the sensor exposure, analog and digital gain to the user-defined target luminance value. The AEG can be programmed to avoid 50Hz and 60Hz flicker.	0x2000~ 0x2072	0x2000[0]
	Premeter	Exposure metering approximates scene to quickly set the sensor exposure and gain. The premeter function can be enabled through software **(I2C)** or digital input pin **(METER)**.	0x3026~ 0x302A	0x3026[3:0]
Timing	STROBE	Synchronized with exposure field and can be used to control LED driver. Please see the Strobe control section.	0x3080~ 0x3089	0x3080[0]
	CXT_SEL	The resolution switch in real time through software **(I2C)** or digital input pin **(CTX_SEL)**. Please see the Context switch section.	0x3024~ 0x3025	0x3024[3:0]
	TRIGGER	When selected, frame trigger is controlled by hardware TRIGGER pin. Please see the mode select control in the Operating modes section.	0x0100	0x0100[2:0]
	FSIN	Aligns the frame read field to an external frame synchronization input signal. Please see the FSYNC section.	0x3010 ~ 0x301C	0x3010[1]
	METER	Active high signal to assert Pre-meter function. Please see the Pre-meter section.	0x3026 ~ 0x3027	0x3026[3]
Interrupt Generator	Interrupt Output	Five interrupts are supported a. Early VSYNC b. AE non-converged c. ALC d. MD e. AE statistic ready	0x2061~ 0x2065	a. 0x309C[0] 0x350F[0] 0x3569[0] b. 0x2001[1] 0x3513[1] 0x356D[1] c. 0x2000[7] 0x3512[7] 0x356C[7] d. 0x209E[2:1] e. 0x2001[0] 0x3513[0] 0x356D[0]
OTP	User Info	One time programmable 1 Kbit memory that can be used to store module information.	0x2500~ 0x2507	-
Embedded data	Embedded data	Embedded sensor's information at the last row of current frame	0x0102[0] 0x3511[0] 0x356B[0]	0x0102[0] 0x3511[0] 0x356B[0]

Table 4.1: ISP and digital block description

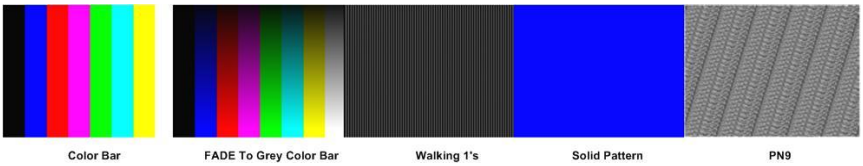


Figure 4.2: Test image patterns

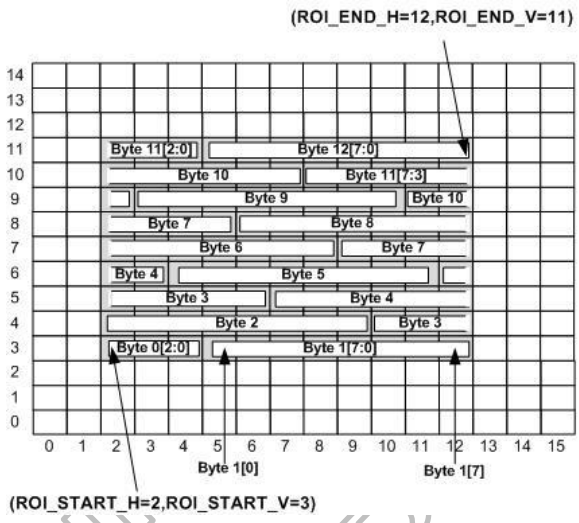
4.1 Motion Detection (MD)

The sensor features on-chip Motion Detection **(MD)** logic. The MD is triggered if a qualified motion event occurs in any one of the selected Motion Detection ROI **(MDROI)**. The maximum MDROI for different resolution is described in Table 4.2. The effective ROI area for motion detect is set by the registers ROI_START_V, ROI_END_V, ROI_START_H and ROI_END_H. Please contact Himax Imaging FAE for additional information to program the MD function.

Window readout	Maximum number of MDROI	ROI size
VGA **(640 x 480)**	16 x 15	40 x 30
QVGA **(320 x 240)**	16 x 15	20 x 15
QQVGA **(160 x 120)**	16 x 14	10 x 8
656 x 496	16 x 16	40 x 30
328 x 248	16 x 16	20 x 15
164 x 124	16 x 15	10 x 8

Table 4.2: Motion Detection (MD) block

There are maximum 256-bit to indicate motion or no-motion for each motion detection block **(Effective ROI area is equal to maximum motion detect block)**. The information can be found in Embedded_line[29] ~ Embedded_line[60] and registers **0x20A1** to **0x20C0**.



Embedded motion map	Register motion map	Corresponding Value
Embedded_ line[29]	Register 0x20A1	Byte 12
Embedded_ line[30]	Register 0x20A2	Byte 11
. . .	. . .	. . .
Embedded_ line[40]	Register 0x20AC	Byte 1
Embedded_ line[41]	Register 0x20AD	Byte 0[2:0]
Embedded_ line[42]	Register 0x20AE	-
. . .	. . .	. . .
Embedded_ line[60]	Register 0x20C0	-

Figure 4.3: Example for VGA effective ROI area and map

4.2 Strobe control

HM0360 supports strobe function synchronized with exposure field and can be used to control synchronized light sources, such as an LED. There are four different modes: Static, Dynamic1, Dynamic2 and Multiple modes as shown in the Figure 4.4.

Strobe function is enabled by setting register **0x3080[0]** to 1 and strobe mode is set by register **0x3080[4:1]**. Strobe front porch is programmed by register **0x3082** and register **0x3083**. Strobe end porch is set by register **0x3084** and register **0x3085**. The step of strobe front porch and strobe end porch are one PCLKO clock time unit. Strobe line is set by register **0x3086** and register **0x3087** with programming resolution of one row. Output programmed number of strobe is set by register **0x3088** and register **0x3089**.

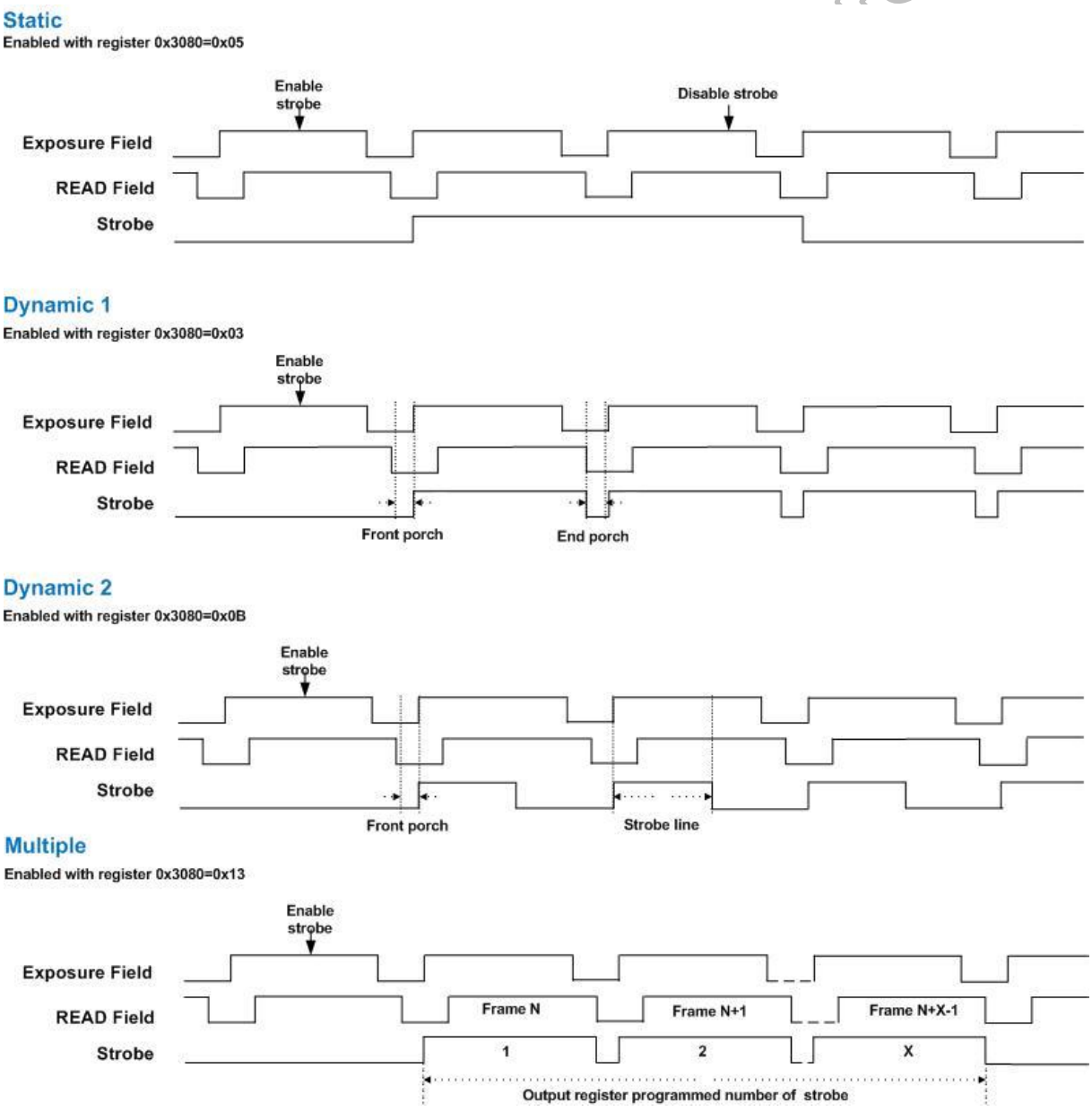


Figure 4.4: Strobe control

4.3 FSYNC

HM0360 can synchronize the sensor read field to the rising edge of an external frame pulse provided at the sensor's FSIN input pin. The FSYNC function is enabled by setting register **0x3010[1]** to 1.

If the period of FSIN pulses is longer than the programmed frame length, the sensor will output one read field at the rising edge of every FSIN pulse. If the period of FSIN pulses are shorter than the internal frame length, the sensor will output the next read field synchronized to the first FSIN following the internal frame length.

The Figure 4.5 is to depict the condition that the period of the FSIN pulses is shorter than the set internal frame length. In this example, the sensor will output one frame data every three FSIN pulses.

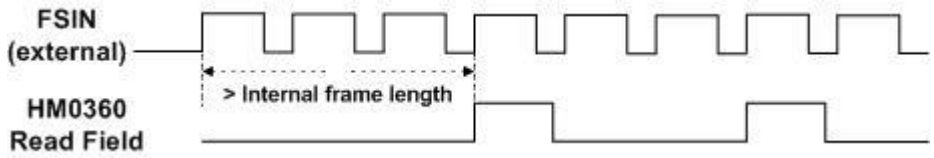


Figure 4.5: FSYNC tracking

4.4 Context switch

HM0360 support two context fields **(Context A, Context B)** that allow programmable parameters, such as frame size, readout mode, PLL, Auto Exposure, Motion Detection, and interrupt configuration to be grouped as one context and selected with an I2C command or hardware input. "Selected with I2C command" is enabled by setting register **0x3024[1]** to 0 and context A is selected by programming register **0x3024[0]** to 0. "Select with hardware input" is enabled by setting register **0x3024[1]** to 1 and context A is selected by applying low voltage level to digital input pin **(CTX_SEL)**. When the new context is selected within the current frame period, the new context will take effect in the following frame.

The context can be manually selected **(Off, Context A, Context B)** or can be set to automatically switch between Context A and Context B. In the automatic switch mode of operation, the number of Context A frames and Context B frames can be programmed by register **0x3025[3:0]** and register **0x3025[7:4]**, respectively.

The Context Switch control register is set by register **0x3024[3:0]**. The Context A registers are set from register **0x3500** to **0x3559**; and the Context B registers are set from **0x355A** to **0x35B3**.

4.5 Interrupt

HM0360 support five interrupt conditions: Early VSYNC; AE non-converged; ALC; MD and AE Statistic ready.

Interrupt	Description	Enable bit
Early VSYNC	An early flag of VSYNC **(provide the delay for host to power up and then receive sensor data successfully)**	0x309C[0] 0x350F[0] 0x3569[0]
AE non-converged	Interrupt happen if AE does not converge	0x2001[1] 0x3513[1] 0x356D[1]
ALC	During AE update disabled a. Interrupt for illumination change. The mean value of frame N is away from AE target **(non-converged)**, interrupt happen if mean value of frame N+1 converge. b. Interrupt happen if mean value does not converge with more than frames programmed by frame counter **(register 0x205B[7:0])**	0x2000[7] 0x3512[7] 0x356C[7]
MD	Motion interrupt enable	0x209E[1]
AE statistic ready	During AE update disabled AE statistic calculated ready, store related information in register and embedded line	0x2001[0] 0x3513[0] 0x356D[0]

Table 4.3: Interrupt control

4.6 AEGC

The AEGC state machine adjusts the integration, analog gain and digital gain against the target brightness value. Three convergence zones with programmable damping factors balance speed and stability.

In the fast zone, large exposure steps are applied to quickly converge to the target brightness value. In the slow zone, small exposure gain steps are applied to smoothly converge to the target brightness value. Inside the target zone, the control loop does not change exposure gain values.

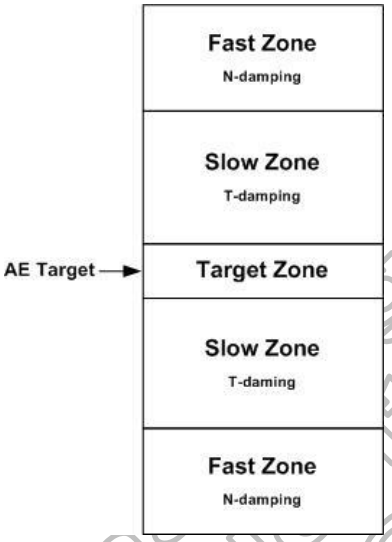


Figure 4.6: AE Zone

HM0360 support 5x5 AE ROI window mode that allow weighting adjustment in each ROI block. The start address of 5x5 AE ROI window is set by register CNT_ORG_H and register CNT_ORG_V. The size of each ROI block is set by register CNT_ST_H and CNT_ST_V.

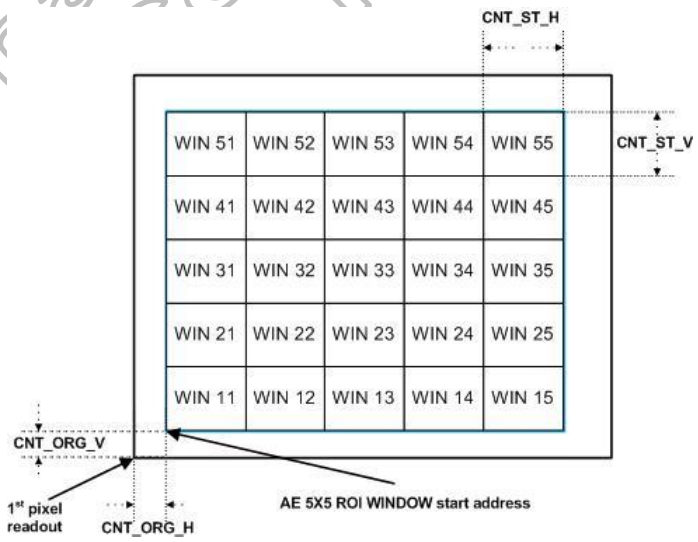


Figure 4.7: AE ROI window

4.7 One Time Programming (OTP) memory

HM0360 offers 1 Kbit of One Time Programming **(OTP)** memory that can be used to store module information. It is recommended to connect a 0.1μF capacitor between HVP pin and ground for write operation. HVP pin can be left open **(floating)** during read operation.

4.8 Pre-meter

To further reduce the camera power consumption and system latency, the HM0360 offers pre-meter function to quickly output well-exposed frames. The pre-meter function is enabled by programming register **0x3026[3:0]** and the operation scenario is depicted in Figure 4.8.

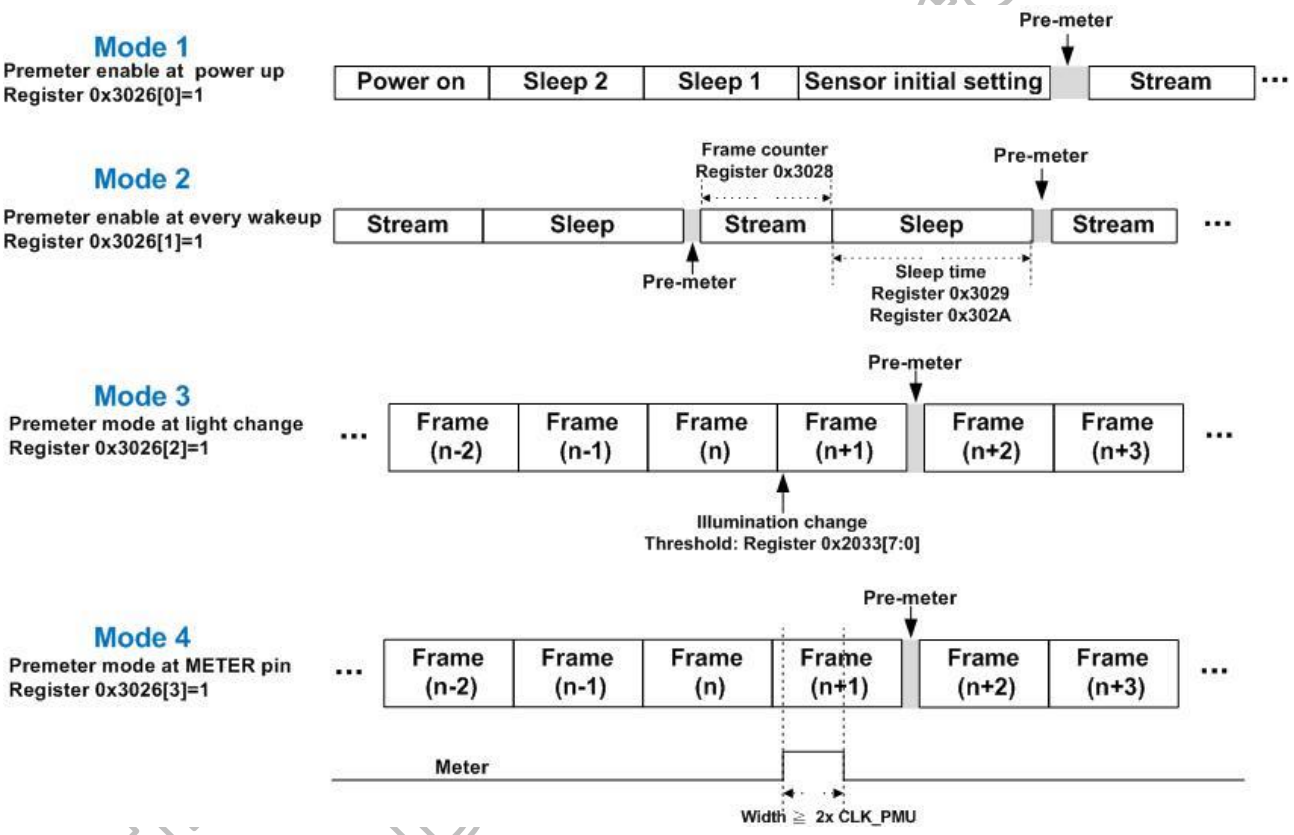


Figure 4.8: Four operation scenarios for pre-meter

4.9 Embedded data

HM0360 supports embedded data which contains predefined sensor register data such as I2C slave address ID, frame count, AE and MD parameters for current frame. The embedded data is available for both MIPI and parallel interface. The embedded sensor register data are appended at the last row of frame by setting EMBEDDED_LINE_EN to 1.

Byte content	Embedded content
0	I2C slave ID
1	FRAME_COUNT_H
2	FRAME_COUNT_L
4	FRAME_LENGTH_LINES_H
5	FRAME_LENGTH_LINES_L
6	LINE_LENGTH_PCK_H
7	LINE_LENGTH_PCK_L
8	INTEGRATION_H
9	INTEGRATION_L
10	ANALOG_GAIN
11	DIGITAL_GAIN_H
12	DIGITAL_GAIN_L
24	Interrupt Indicator [5]: Early VSYNC [4]: RESERVED [3]: MD INT [2]: AE non-converged [1]: AE statistic ready [0]: AE ALC
25	AE MEAN
28	[0]: MD INT Flag **(Origin)** [1]: MD INT Flag **(Latency)**
29~60	MD flag 0~MD flag 31

Table 4.4: Embedded Data Content

4.10 Tone mapping

HM0360 supports tone mapping **(it does not increase dynamic range and only for monochrome sensor)** to preserve image details. Compression curve **(Input 10b, Output 8b)** and examples for three level are provided based on “low”, “medium” and “High” level.

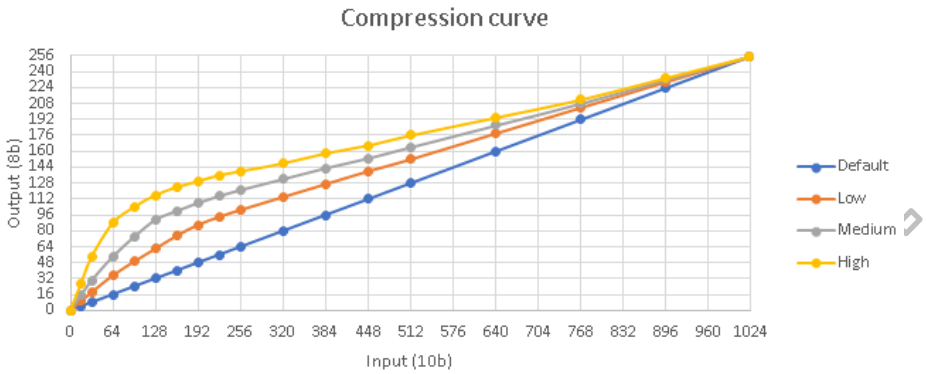


Figure 4.9: Compression curve (input 10b, output 8b)

Register	Default (Hex)	Low (Hex)	Medium (Hex)	High (Hex)
0x1030	0x04	0x09	0x0F	0x1B
0x1031	0x08	0x12	0x1E	0x36
0x1032	0x10	0x23	0x36	0x58
0x1033	0x18	0x31	0x4A	0x68
0x1034	0x20	0x3E	0x5B	0x74
0x1035	0x28	0x4B	0x64	0x7C
0x1036	0x30	0x56	0x6C	0x82
0x1037	0x38	0x5E	0x73	0x88
0x1038	0x40	0x65	0x79	0x8C
0x1039	0x50	0x72	0x84	0x94
0x103A	0x60	0x7F	0x8F	0x9E
0x103B	0x70	0x8C	0x99	0xA6
0x103C	0x80	0x98	0xA4	0xB0
0x103D	0xA0	0xB2	0xBA	0xC2
0x103E	0xC0	0xCC	0xD0	0xD4
0x103F	0xE0	0xE6	0xE8	0xEA

Table 4.5: Tone mapping parameters

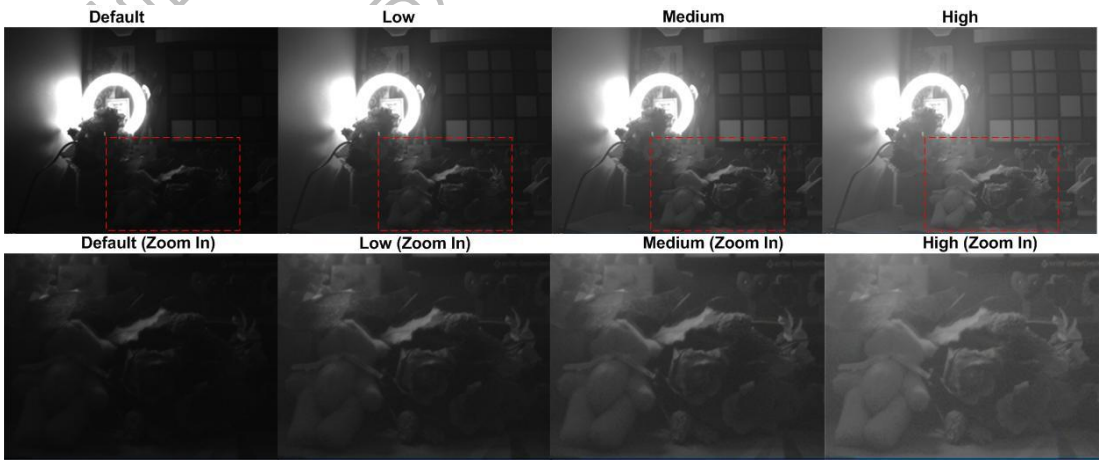
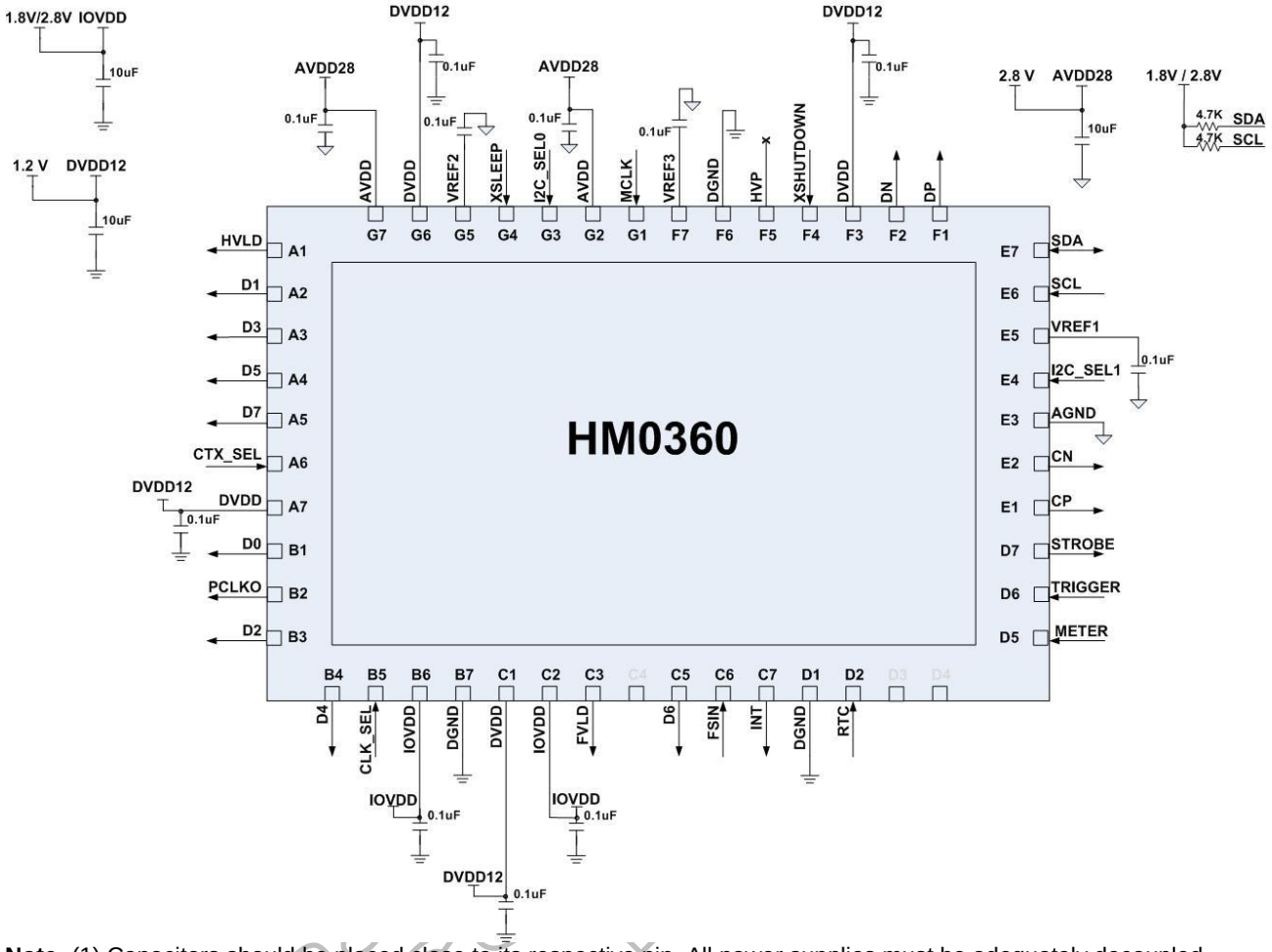


Figure 4.10: Tone mapping examples

5. Typical Application Circuit

5.1 Reference circuit for triple supply

5.1.1 External LDO mode (CSP)

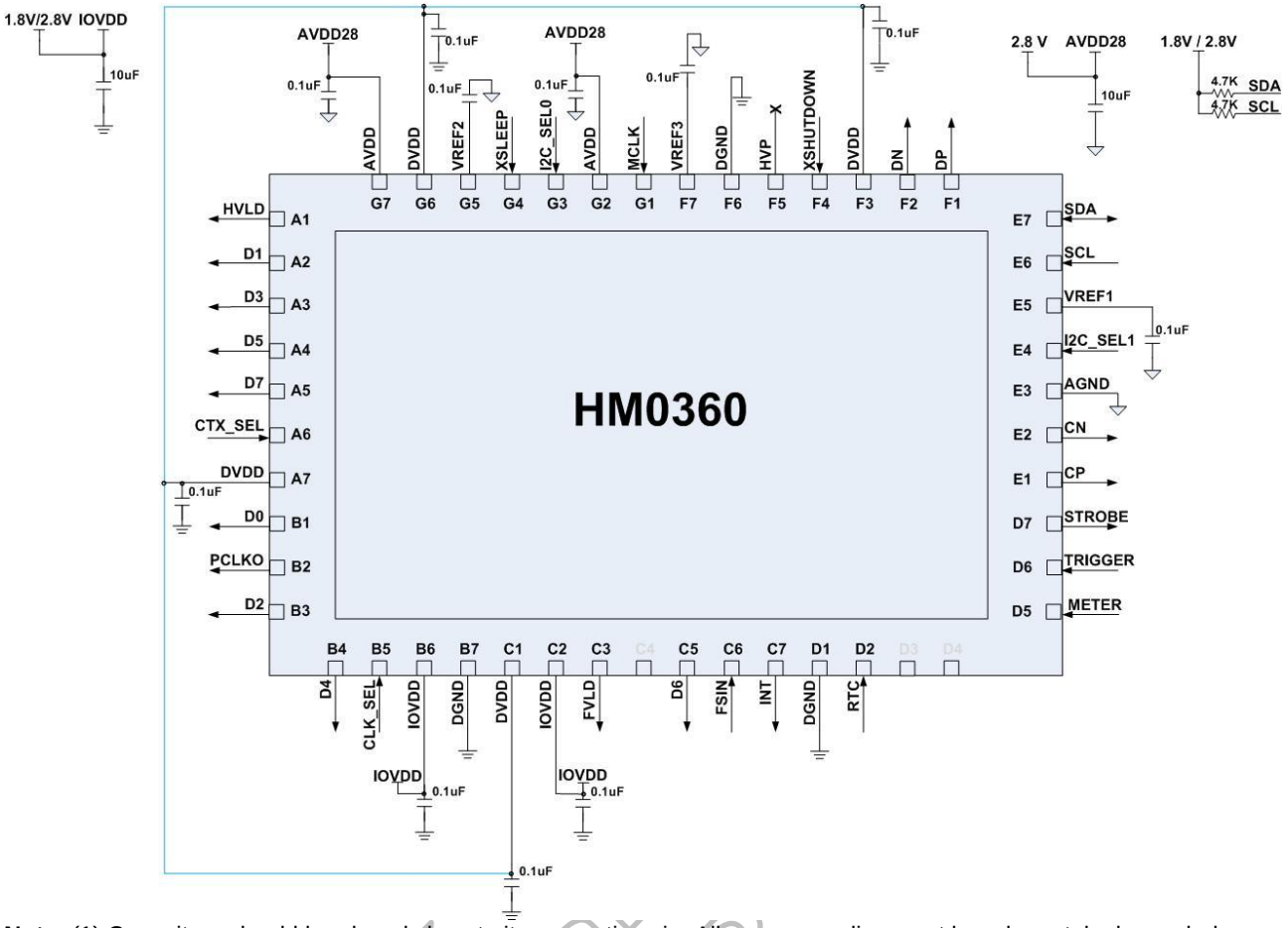


Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) CCI pull-up resistors should have a value based on the CCI specification **(typically 4k7 ohm)**
(3) RTC pin must not be left floating, connected to DGND without RTC clock input.
(4) MCLK connect to DGND when using internal oscillator.

Figure 5.1: Application circuit for CSP (External LDO mode)

5.2 Reference circuit for dual supply

5.2.1 Internal LDO mode (CSP)



Note: (1) Capacitors should be placed close to its respective pin. All power supplies must be adequately decoupled.
(2) CCI pull-up resistors should have a value based on the CCI specification **(typically 4k7 ohm)**.
(3) RTC pin must not be left floating, connected to DGND without RTC clock input.
(4) MCLK connect to DGND when using internal oscillator.

Figure 5.2: Application circuit for CSP (Internal LDO mode)

6. System Level Description

6.1 Operating modes

The HM0360 supports nine modes of operation as shown in Table 6.1.

Mode	Description	Power	Register values	I2C	CLOCK	Digital
Power off	No power supplied to sensor	Off	-	-	-	-
Sleep 2 **(HW)**	Hardware sleep; lowest power consumption mode **(XSLEEP=low)**	On	Retained	Off	Off	Standby mode
Sleep 1 **(SW)**	**MODE_SELECT[2:0]=000** Soft sleep with I2C enabled; Wait for SW I2C trigger or I2C configuration for HW trigger and TRIGGER command	On	Retained	On	On or Off	Standby mode
Streaming 1	**MODE_SELECT[2:0]=001** SW I2C triggered; continuous streaming	On	Retained	On	On	On
Streaming 2	**MODE_SELECT[2:0]=010** SW I2C triggered; auto wake up, output N frame and then sleep. Register **0x3028[7:0]** sets the frame output number. Register **0x3029[7:0]** and **0x302A[7:0]** set sleep time counter	On	Retained	On	On	On
Streaming 3	**MODE_SELECT[2:0]=011** SW I2C triggered; output register programmed number of frames **(0x3028[7:0])**, then enters s/w standby and clears **MODE_SELECT** register bit to 000	On	Retained	On	On	On
Streaming 4	**MODE_SELECT[2:0]=100** Digital input pin **(TRIGGER)** trigger streaming enable	On	Retained	On	On	On
Streaming 5	**MODE_SELECT[2:0]=110** Digital input pin **(TRIGGER)** frame trigger; output register programmed number of frames **(0x3028[7:0])**, then enters S/W standby	On	Retained	On	On	On
Streaming 6	**MODE_SELECT[2:0]=111** Digital input pin **(TRIGGER)** frame trigger; auto wake up, output N frame and then sleep **(cycle, until HW TRIGGER goes to low)**. Register **0x3028[7:0]** is to set frame output number. Register **0x3029[7:0]** and **0x302A[7:0]** set sleep time counter	On	Retained	On	On	On

Table 6.1: Operating modes

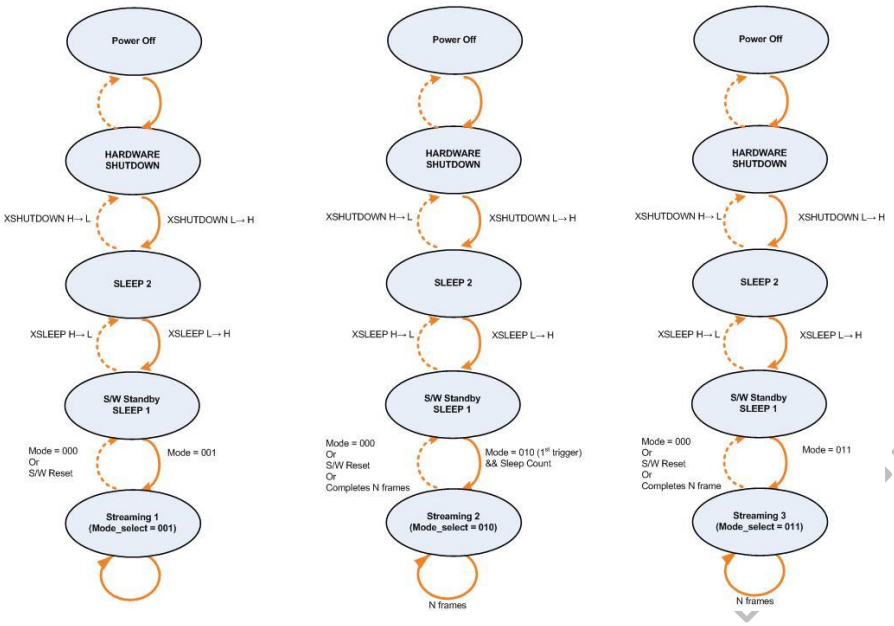


Figure 6.1: State diagram (Software I2C trigger)

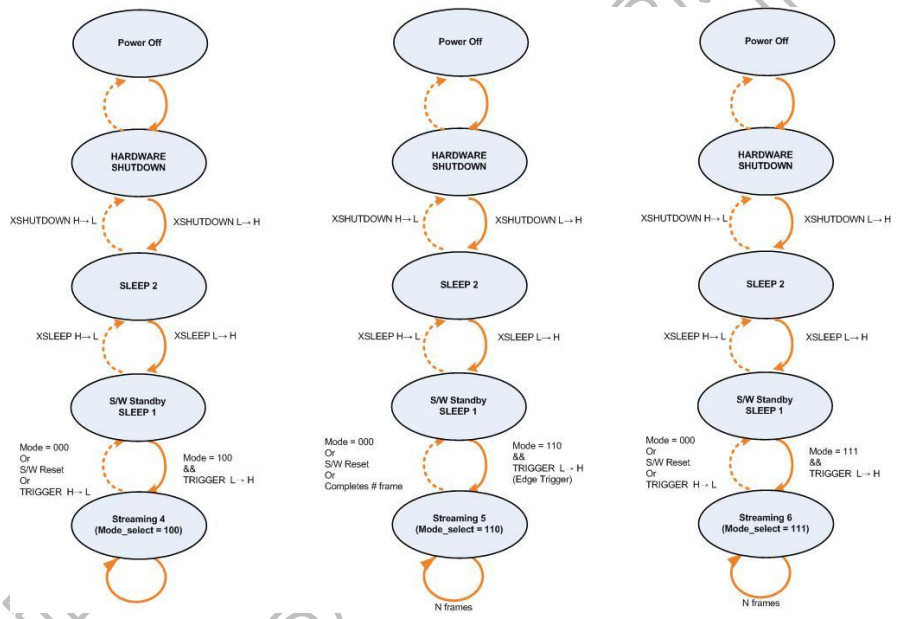


Figure 6.2: State diagram (Hardware pin trigger)

6.2 Reset

HM0360 provides two methods of reset methods: Power On Reset **(POR)** and software reset.

During power up, an internal POR circuit applies a system reset until the XSHUTDOWN pin reaches a monitored voltage threshold. This insures that the supply voltage is stable, and the sensor can be properly initialized.

Software reset is applied by writing register value 0 or 1 to register bit SW_RESET [0] **(0x0103[0])**. When reset is applied, the sensor will return to “Standby Mode” and reset all serial interface registers to its default values.

6.3 Power up sequence

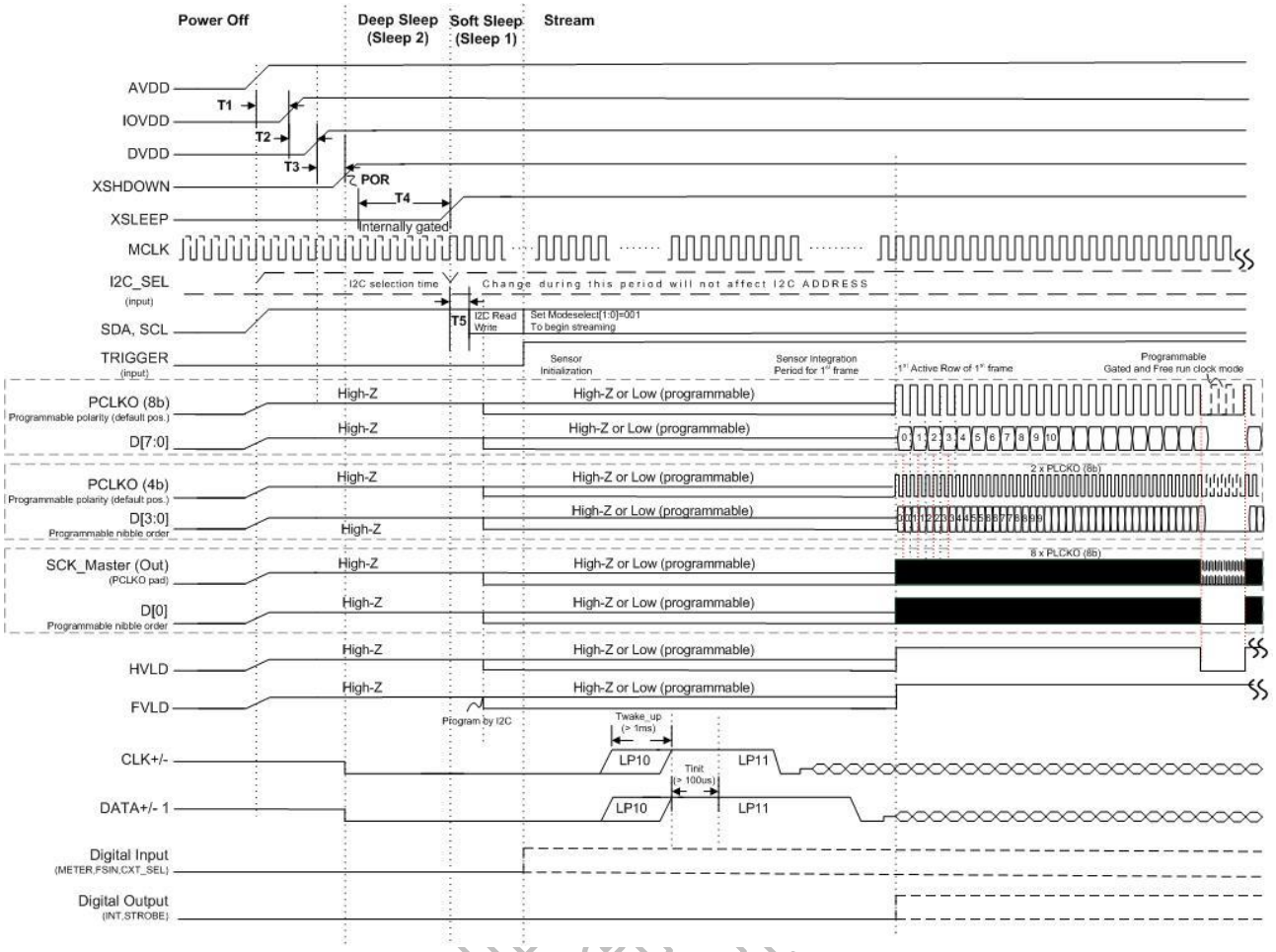


Figure 6.3: Power up sequence

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
AVDD to IOVDD	T1	0	-	∞	s
IOVDD to DVDD	T2	0	-	∞	s
DVDD to XSHDOWN **(External DVDD)**	T3	0	-	∞	s
Power On Reset time	POR	-	-	50	µs
Power On Reset to XSLEEP	T4	200	-	-	µs
XSLEEP to 1st I2C command	T5	10	-	-	µs

Note: (1) The minimum timing of T4 is 0 us when using external reference clock and external LDO mode.

Table 6.2: Power up sequence timing

6.4 Clock setup

Reference clock to the sensor can be provided externally through the MCLK pin or generated by the on-chip self-oscillator. The sensor will select the self-oscillator if applying low voltage level to CLK_SEL pin.

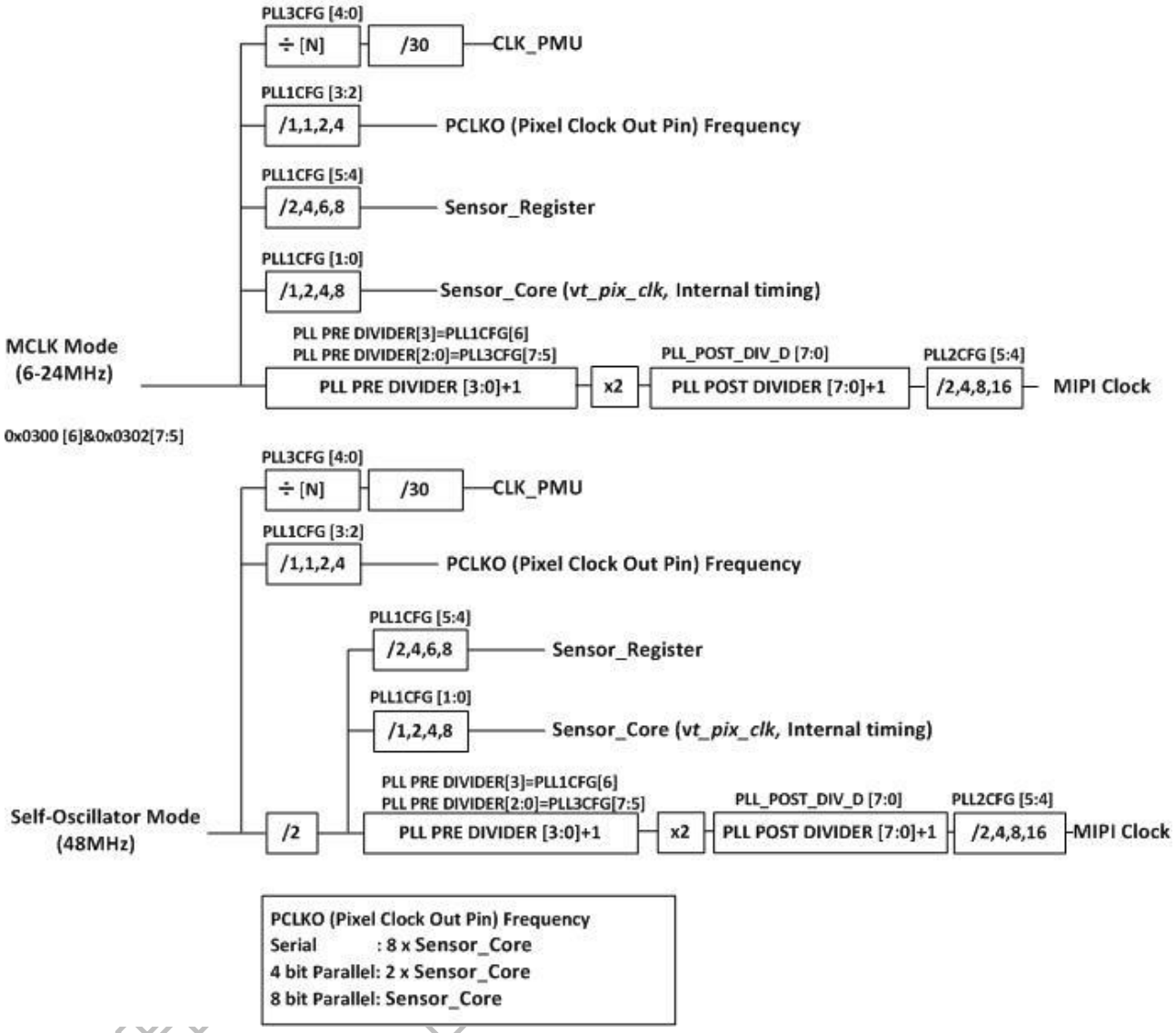


Figure 6.4: Clock dividers

6.5 IO control options

Options for IO pins can be programmed based on the Table 6.3. Please consult Himax Imaging FAE for additional information.

Output pin	Drive strength	Polarity	Interface bit width	Sync advance or retreat	MSB / LSB	PCLKO clock gating
D[7:4]	**0x310F[5:3]**	-	**0x310F[7:6]** 00=8-bit 01=4-bit 10=1-bit	-	**0x3112[3]**(1) 0=MSB 1=LSB	-
D[3:1]	**0x310F[2:0]**	-		-		-
D[0]	**0x310E[6:4]**	-		-		-
HVLD	**0x310E[3:1]**	-	-	**0x3096[7:0]~ 0x3099[7:0]**	-	-
FVLD	**0x310E[3:1]**	-	-	**0x3094[7:0] 0x3095[7:0]**	-	-
PCLKO	**0x3110[2:0]**	**0x3112[2]** 0: Falling edge 1: Rising edge	-	-	-	**0x1014[3]** 0: Non-gated 1: Gated clk
INT STROBE	**0x3111[2:0]**	-	-	-	-	-

Note: (1) 1-bit / 4-bit data mode only.

Table 6.3: IO control options

The status for output pins can be control by register described in Table 6.4.

Register 0x310E[0]	Register 0x3110[7]	Register 0x30A8[0]	Register 0x30A5	Streaming	Standby/VSYNC blanking
1	0	1	0x01	Driving	Hi-Z
0	1	1	0x01	Driving	Driving
-	-	0	0x00	Hi-Z	Hi-Z

Table 6.4: Output pin status

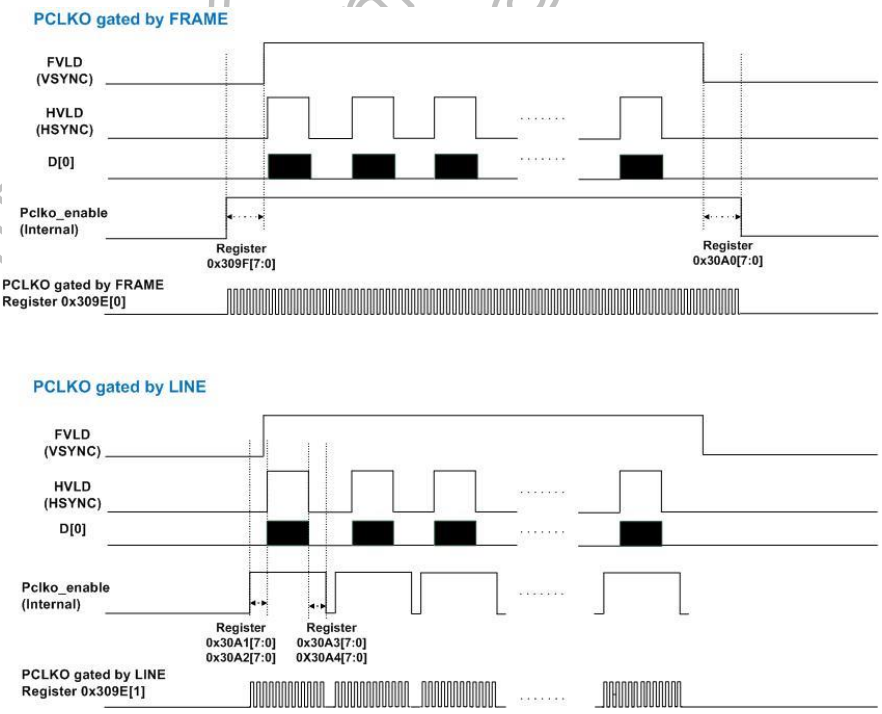


Figure 6.5: Gated serial data clock option

6.6 Data format control

Output data bit	Mode of operation	0x310F[6] 4bit_enable	0x310F[7] 1bit_enable	0x1014[3] gated_enable	0x309E[1:0] gate by frame/line	0x3112[3] msb_enable
8	Non-gated	0	0	0	0	0
8	Gated by frame	0	0	1	1	0
4	Non-gated; LSB	1	0	0	0	0
	Non-gated; MSB	1	0	0	0	1
	Gated by frame; LSB	1	0	1	1	0
	Gated by line; MSB	1	0	1	2	1
1	Non-gated; LSB	0	1	0	0	0
	Non-gated; MSB	0	1	0	0	1
	Gated by frame; LSB	0	1	1	1	0
	Gated by line; MSB	0	1	1	2	1

Table 6.5: Data format control setting summary

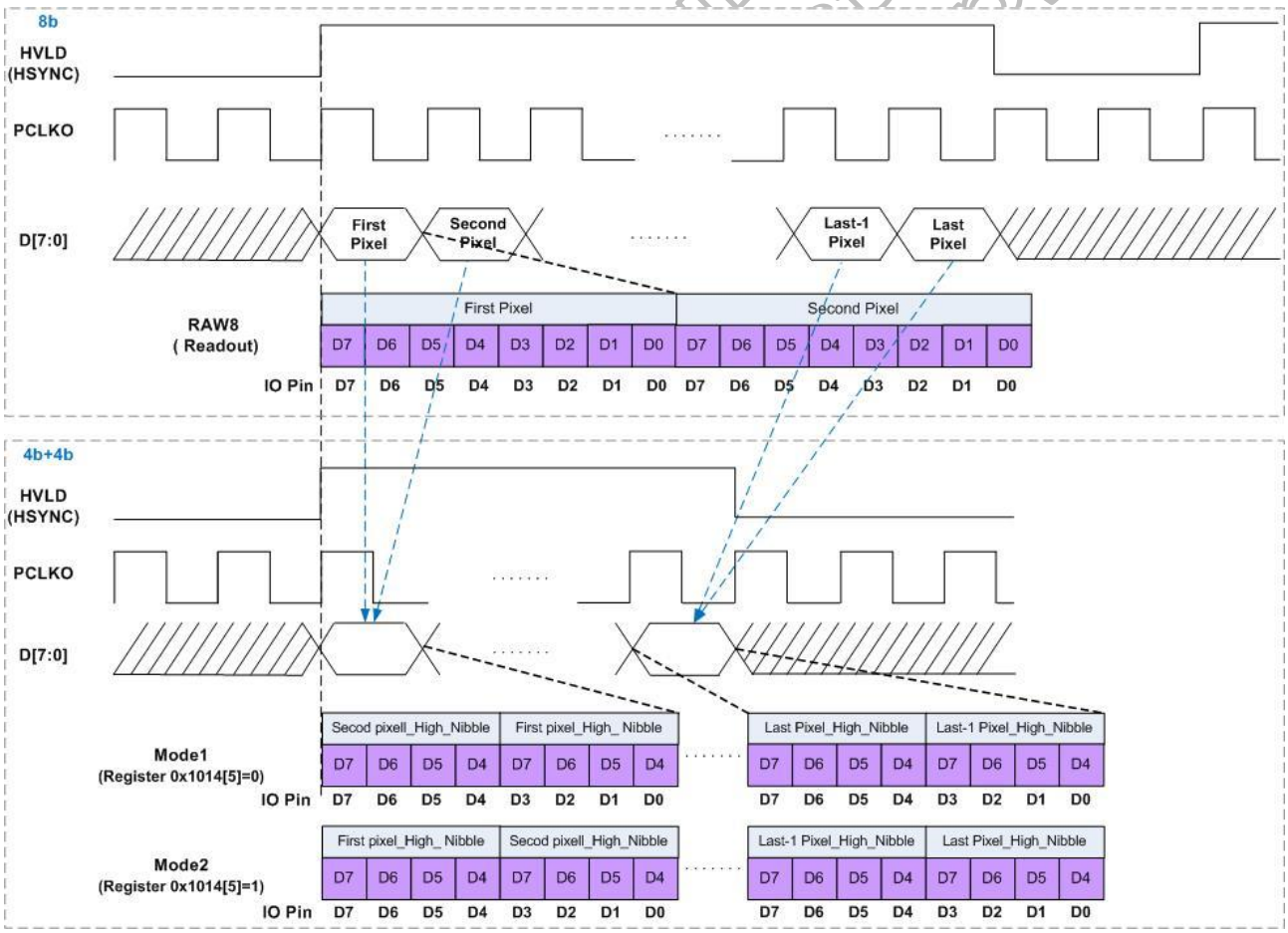


Figure 6.6: Output format on 8-bit data IO interface

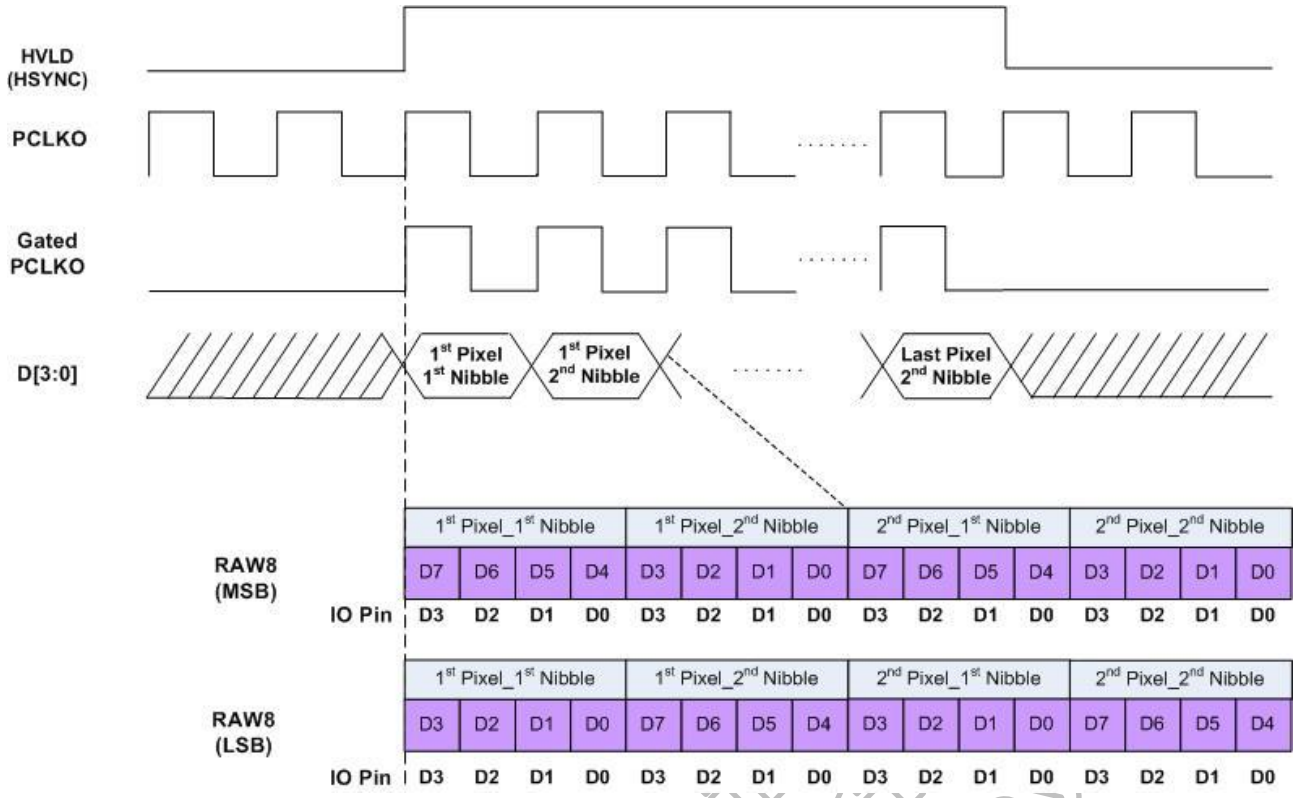


Figure 6.7: Output format on 4-bit data IO interface

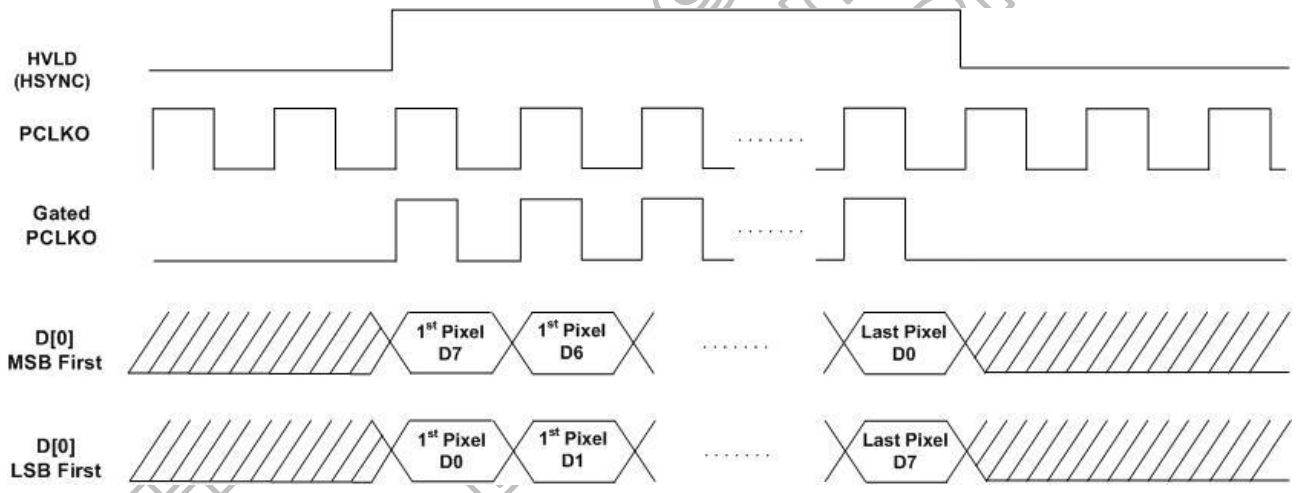


Figure 6.8: Output format on serial data IO interface

6.7 Multiple camera application

HM0360 supports two modes for multiple HM0360 sensors to output image in sequence.

6.7.1 Mode 1

Mode 1 is enabled by programming register **0x30A9** to 0x01. An example of block diagram and the operation scenario for mode 1 **(daisy chain)** are depicted in Figure 6.9 and Figure 6.10 respectively. The constraint for mode 1 is that hardware trigger should be pulled low in the duration between VSYNC1 rising edge and VSYNC2 falling edge.

- Sensor 1 streams on after applying high voltage level to hardware trigger.
- Sensor 2 outputs one frame after receiving statistic ready interrupt of INT1 through FSIN2 pin.
- Sensor 1 outputs one frame after receiving statistic ready interrupt of INT2 through FSIN1 pin.

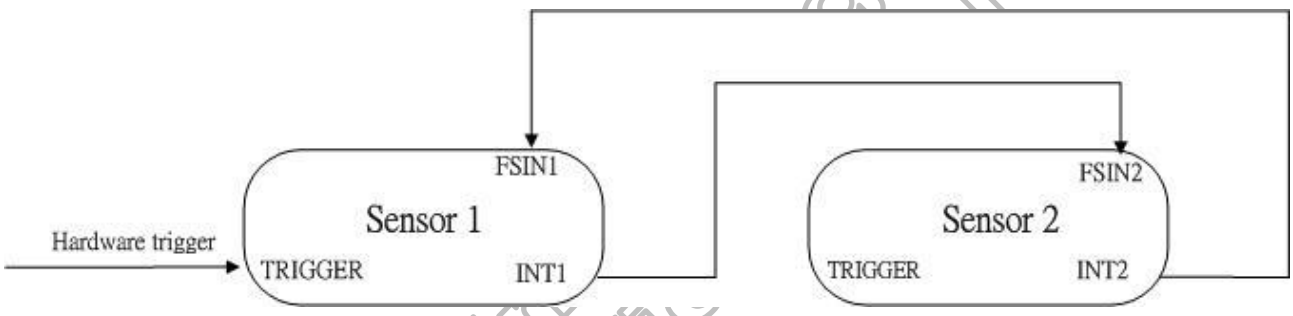


Figure 6.9: Block diagram for mode 1

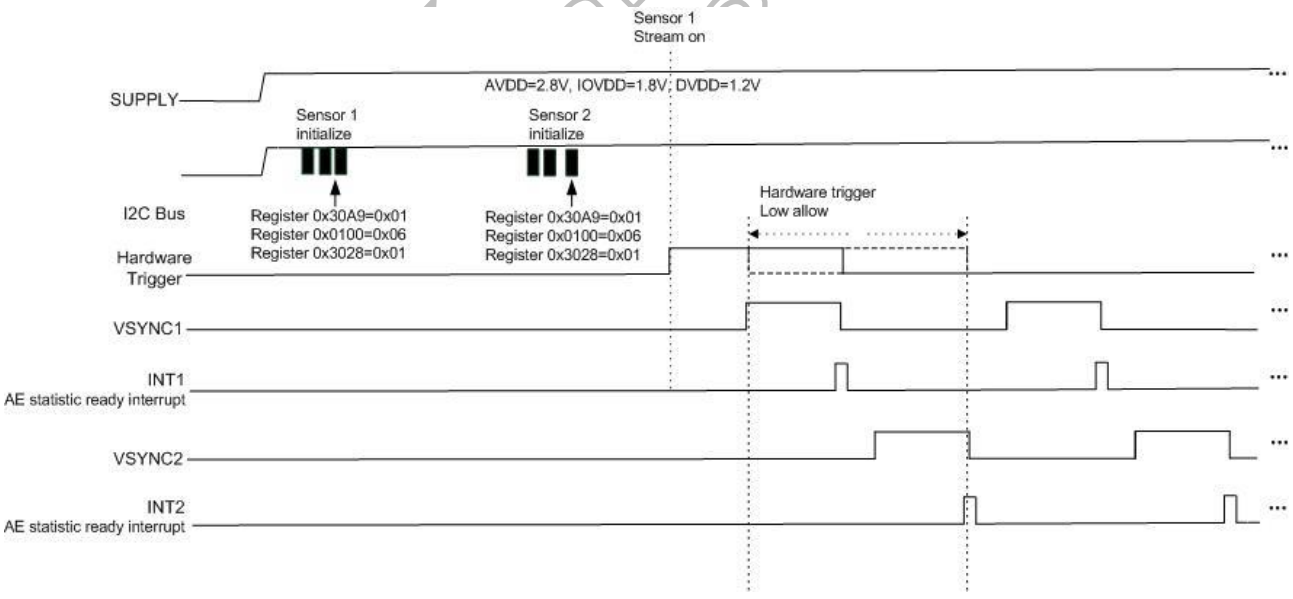


Figure 6.10: Operation scenario for mode 1

6.7.2 Mode 2

HM0360 supports a digital function to adjust the latency between hardware trigger and 1st VSYNC rising edge. This function is enabled by programming register **0x30A9** to 0x02. The latency is controlled by register **0x30AA** and register **0x30AB** with programmable resolution of 1 row. This function can also be used for multiple HM0360 sensors to output images sequentially based on a common master clock input. An example of block diagram and the operation scenario for mode 2 are depicted in Figure 6.11 and Figure 6.12 respectively

- Frame length A= Frame length B =Frame height 1+ Frame height 2+ T_C+T_D
  - T_A= maximum integration time + 32 rows
  - Min.T_C and T_D : 8 rows

- Adjust T_B to output VSYNC2 frame height during the VSYNC1 blanking area.
  - T_B= T_A +Frame height 1+T_D

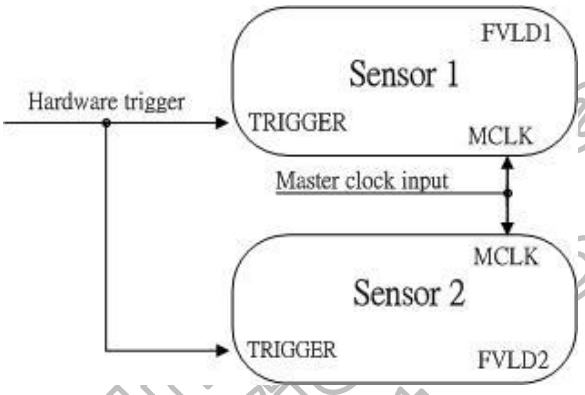


Figure 6.11: Block diagram for mode 2

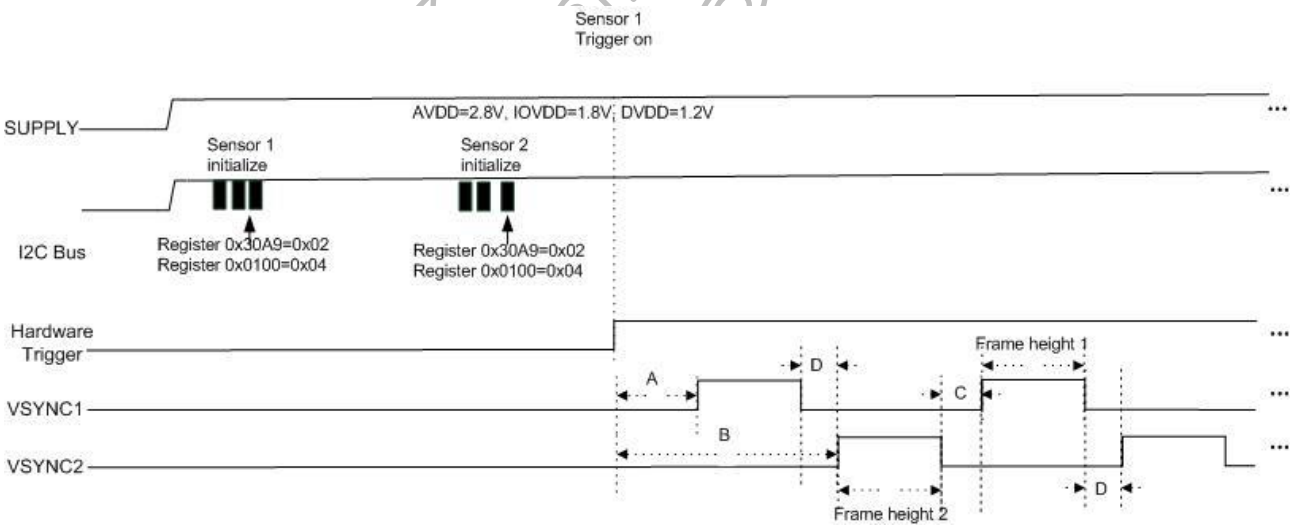


Figure 6.12: Operation scenario for mode 2

7. MIPI serial data interface

The HM0360 supports 1-lane MIPI CSI2 interface **(forward link in High Speed and Low Power mode)** following MIPI Alliance D-PHY specification v1.20 and CSI-2 standard v1.00.

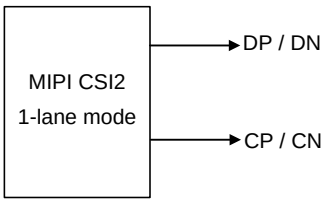


Figure 7.1: MIPI interface lane

7.1 Frame format

The format of the frame follows Figure 7.2. The Line Start **(LS)** and Line End **(LE)** marker are tunable.

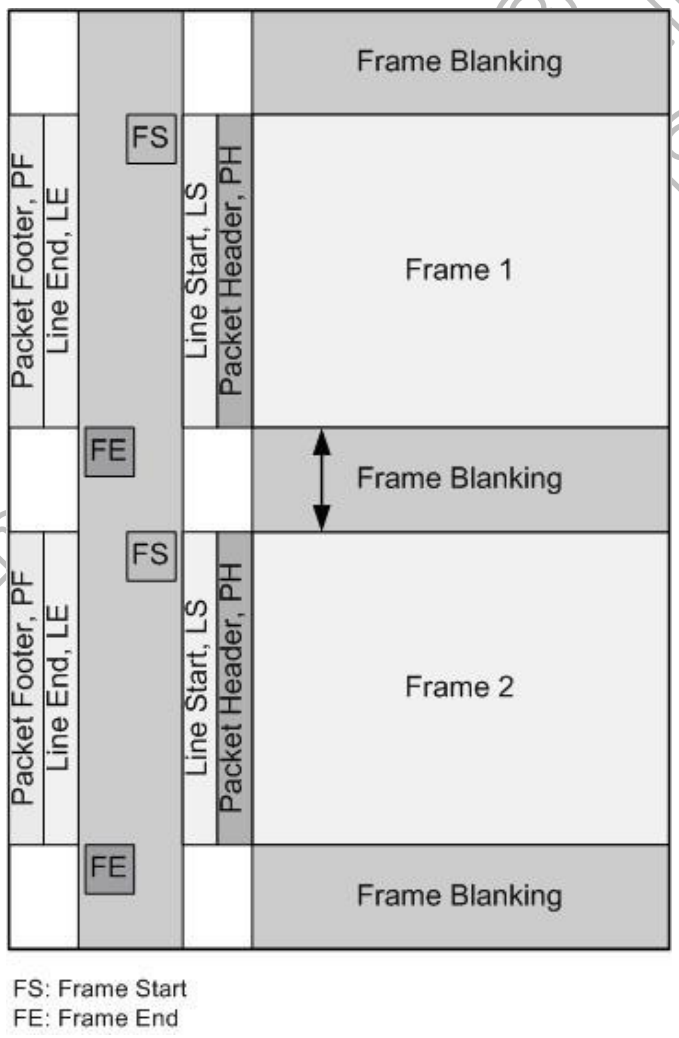


Figure 7.2: Frame format

7.2 MIPI clock mode

The HM0360 supports continuous and gated clock mode as shown in Figure 7.3.

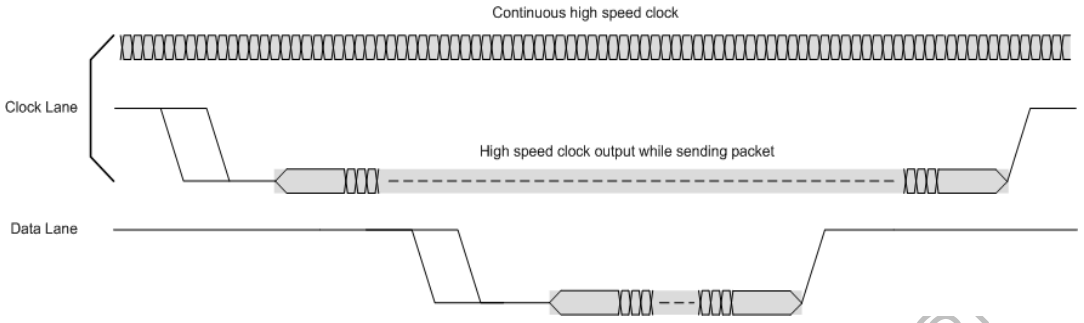


Figure 7.3: MIPI clock lane options

8. Serial Interface Description

The 2-Wire serial interface provides read/write access to the sensor registers

- 2-Wire serial interface consists of SDA **(Bidirectional serial data)** and SCL **(Serial clock)** pins.
- HM0360 uses 16-bit register address and 8-bit register data.
- The sensor uses double-buffered registers to ensure that register changes that affect sensor operation takes place at the beginning of the next valid video frame.
- Supports single and burst read / write up to 1MHz
- The host generates SCL clock signal to the sensor and uses the signal to synchronize all data transfer.

8.1 I2C slave address ID

- Slave address is configured by I2C_SEL0 and I2C_SEL1 pin following the Table 8.1.
- The address of the sensor can be changed by register **0x3401[6:0]** when register **0x3400[0]** set to 1.

I2C_SEL1 pin	I2C_SEL0 pin	Address
Pull Down	Pull Down	0x24 **(7-bit)**
Pull Down	Pull High	0x25 **(7-bit)**
Pull High	Pull Down	0x34 **(7-bit)**
Pull High	Pull High	0x35 **(7-bit)**

Table 8.1: Device address configuration

8.2 Start / Stop conditions

The Start and Stop conditions on the serial bus is issued by the Host.

SDA Transition	SCL	Condition
High to Low	High	Start
Low to High	High	Stop

Table 8.2: Serial interface Start / Stop transition

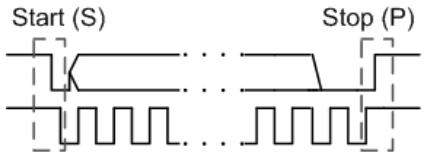


Figure 8.1: 2-Wire serial interface Start / Stop condition

8.3 Data valid

One SCL pulse is generated for each data bit transferred. The host should ensure that the SDA signal must be stable when SCL in High. The SDA signal can transition when SCL is Low.

8.4 Data format

Data is transferred one byte at a time. The most significant bit should always be transferred first. Each byte is followed by an Acknowledge **(ACK)** or a No-Acknowledge bit **(No ACK)**.

8.5 Acknowledge / No-Acknowledge

Each 8-bit is followed by an Acknowledge **(ACK)** or No-Acknowledge **(No ACK)** bit.

- Acknowledge: The Host will release the SDA line. The sensor will drive the SDA line low.
- No-Acknowledge: The Host will release the SDA line. The sensor will not drive the SDA pin **(Pulled high)**. The No ACK bit is used to terminate a read sequence.

8.6 Write sequence

The write sequence is initiated by the Host with Start **(S)** condition, followed by 8-bit device slave ID **(write ID)**

- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(high byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or No ACK signal.
- The write operation is completed when the Host asserts a stop condition

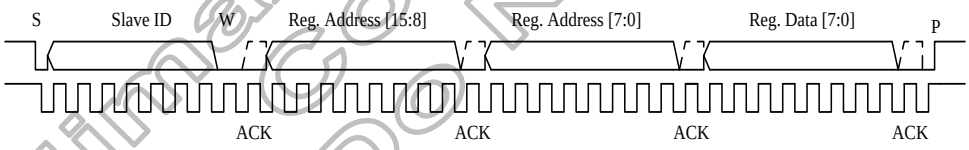


Figure 8.2: 2-Wire serial interface 16-bit address write

8.7 Read sequence

The read sequence is initiated by Host with Start **(S)** condition, followed by the 8-bit device slave ID **(write ID)**.

- If the slave ID is recognized by the sensor, the ACK bit will be sent to the Host.
- Once the Host receives an ACK from the sensor, it can begin to transmit the register address **(high byte first, then low byte)**, then the register data. After each byte, the sensor will issue an ACK or No ACK bit.
- The write operation is completed when the Host asserts a Stop condition.
- The Host must issue another Start condition, followed by the 8-bit device slave ID **(Read ID)**.
- If the register ID is recognized by the sensor, the ACK bit will be sent to the Host.
- The sensor will respond with the Register Data Out.
- The Host will issue an ACK, and then asserts the Stop condition.

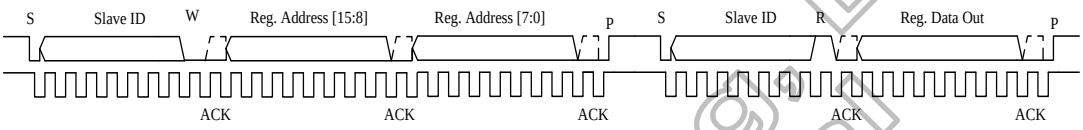


Figure 8.3: 2-Wire serial interface 16-bit address read

9. Sensor Core Control

9.1 Frame retiming

Serial registers that are synchronized to sensor timing utilize double-buffer register to ensure that changes take effect at the start of the frame boundary. In the Register Table section of this document, the registers that require retiming, such as gain and integration **(exposure)**, are indicated by the designator **CMU (Command Update)**.

Changes to retimed registers take effect at the boundary of either the first **(N+1)** or second subsequent frame **(N+2)**. Register **0x3032[0]** = 1 selects N+1 update.

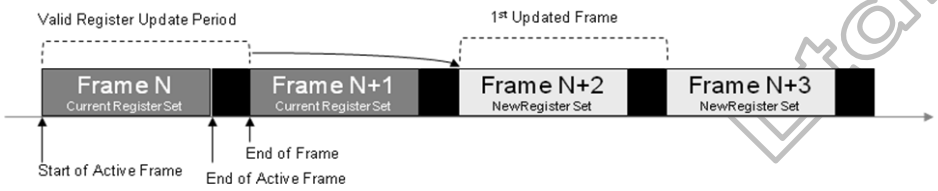


Figure 9.1: (N+2) command update (CMU) timing

9.2 Analog gain control

Analog gain follows the equation 2^N where N is set by ANALOG_ GAIN **0x0205[6:4]**. The valid programmable values for the analog gain register are defined in Table 9.1.

Code (Hex)	Gain (x)	Gain (dB)
0 x 00	1	0
0 x 10	2	6
0 x 20	4	12
0 x 30	8	18
0 x 40	16	24

Table 9.1: Global analog gain settings

9.3 Exposure control

The HM0360 supports coarse integration control with a programmable resolution of 1 row. The exposure time of the sensor is calculated using the following equation:

A. Integration time (seconds) = coarse_integration x line_length_pck / (vt_pix_clk (MHz) x 10^6)
B. Coarse_integration_time ≤ (frame_length_lines – 4)

9.3.1 50Hz / 60Hz flicker avoidance

To avoid flicker, the sensor exposure time should be set in intervals of 1/100 seconds or 1/120 seconds for 50Hz or 60Hz flicker avoidance, respectively.

A. Integration Step Size (60Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 120
B. Integration Step Size (50Hz Avoidance) = vt_pix_clk (MHz) x 1 x 10^6 / line_length_pck / 100

9.4 Frame rate control

The frame rate of the sensor is calculated based on the Video Timing Clock and uses the following equations:

A. 65535 ≥ line_length_pck ≥ min_line_length_pck
B. 65535 ≥ frame_length_lines ≥ min_frame_length_lines
C. frame rate = vt_pix_clk (MHz) ^{x} 1 x 10^6/ (frame_length_lines x line_length_pck)

10. Register Table

10.1 Sensor ID registers [0x0000 – 0x0007]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0000	[7:0]	MODEL_ID_H	RO	16-bit sensor part number	-	0x03
0x0001	[7:0]	MODEL_ID_L	RO	**(HM0360)**	-	0x60
0x0002	[7:0]	SILICON_REV	RO	Silicon Revision Number	-	-
0x0005	[7:0]	FRAME_COUNT_H	RO	16-bit Frame counter	-	0xFF
0x0006	[7:0]	FRAME_COUNT_L	RO		-	0xFF
0x0007	[1:0]	PIXEL_ORDER	RO	[1:0] Color Sensor Pixel Order 0: GR 1: RG 2: BG 3: GB	-	0x02

10.2 Sensor mode control registers [0x0100 – 0x0104]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0100	[2:0]	MODE_SELECT	RW	[2:0]: Sensor mode selection **SW I2C trigger** streaming: 000: Sleep1 001: Continuous streaming 010: Automatic wake up sleep cycles 011: Snapshot with N frames output **HW pin trigger** streaming: 100: continuous Streaming 110: Snapshot with N frames output 111: Automatic wake up sleep cycles	-	0x00
0x0101	[1:0]	IMAGE_ORIENTATION	RW	Image Orientation [1]: Vertical flip enable [0]: Horizontal mirror enable	Y	0x00
0x0102	[0]	EMBEDDED_LINE_EN	RW	[0]: Embedded line enable	-	0x00
0x0103	[0]	SW_RESET	WO	[0]: Software reset	-	0xFF
0x0104	[0]	COMMAND_UPDATE	WO	[0]: Command update	-	0x00

10.3 Sensor exposure gain control registers [0x0202 – 0x020F]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0202	[7:0]	INTEGRATION_H	RW	Coarse integration time in lines	Y	0x00
0x0203	[7:0]	INTEGRATION_L	RW	**(16-bit UINT)**	Y	0x08
0x0205	[6:4]	ANALOG_GAIN	RW	Analog Global Gain code **(3-bit UINT)**	Y	0x00
0x020E	[1:0]	DIGITAL_GAIN_H	RW	Digital Global Gain code	Y	0x01
0x020F	[7:2]	DIGITAL_GAIN_L	RW	**(8-bit UINT)**	Y	0x00

10.4 Clock control registers [0x0300 – 0x0302]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0300	[7:0]	PLL1CFG	RW	[7]: Reserved [6]: PLL PRE DIVIDER [3] [5:4]: CLK_I2C divider 00: /2 01: /4 10: /6 11: /8 [3:2]: PCLKO divider 00: /1 01: /1 10: /2 11: /4 [1:0]: CLK_TB divider 00: /1 01: /2 10: /4 11: /8	Y	0x04
0x0301	[7:0]	PLL2CFG	RW	[7:6]: Reserved [5:4]: mipi_cll = pll output 00: /2 01: /4 10: /8 11: /16 [3]: Reserved [2:0]: Reserved	-	0x0A
0x0302	[7:0]	PLL3CFG	RW	[7:5]: PLL PRE DIVIDER [2:0] [4:0]: Divider for 24MHz to 1MHz	-	0x78

10.5 Frame timing control registers [0x0340 – 0x0343]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0340	[7:0]	FRAME_LENGTH_LINES_H	RW	frame_length_lines **(16-bit UINT)**	Y	0x02
0x0341	[7:0]	FRAME_LENGTH_LINES_L	RW		Y	0x14
0x0342	[7:0]	LINE_LENGTH_PCK_H	RW	line_length_pck **(16-bit UINT)**	Y	0x03
0x0343	[7:0]	LINE_LENGTH_PCK_L	RW		Y	0x00

10.6 Monochrome programming registers [0x0370 – 0x0372]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0370	[0]	MONO_MODE	RW	[0]: Mono Mode Indicator	-	0x00
0x0371	[0]	MONO_MODE_ISP	RW	[0]: Mono Mode for ISP block	-	0x01
0x0372	[0]	MONO_MODE_SEL	RW	[0]: Select Mono_mode indicator from OTP	-	0x01

10.7 Sub-sampling / Binning control registers [0x0380 – 0x0382]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0380	[1:0]	H_SUB	RW	[1:0]: Horizontal Operation 00: Full frame 01: Sub2 10: Sub4	-	0x00
0x0381	[1:0]	V_SUB	RW	[1:0]: Vertical Operation 00: Full frame 01: Sub2 10: Sub4	-	0x00
0x0382	[1:0]	BINNING_MODE	RW	Binning Operation [1]: Horizontal Binning [0]: Vertical Binning	-	0x00

10.8 Test pattern control registers [0x0601 – 0x0609]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x0601	[6:4] [0]	TEST_PATTERN_MODE	RW	[6:4]: Mode selection 0: Color Bar 1: FADE To Grey Color Bar 2: Walking 1's 3: Solid Pattern 4: PN9 [0]: Test pattern enable	-	0x00
0x0602	[2:0]	TEST_DATA_BLUE_H	RW	TEST_DATA_BLUE_H	-	0x00
0x0603	[7:0]	TEST_DATA_BLUE_L	RW	TEST_DATA_BLUE_L	-	0x00
0x0604	[2:0]	TEST_DATA_GB_H	RW	TEST_DATA_GB_H	-	0x00
0x0605	[7:0]	TEST_DATA_GB_L	RW	TEST_DATA_GB_L	-	0x00
0x0606	[2:0]	TEST_DATA_GR_H	RW	TEST_DATA_GR_H	-	0x00
0x0607	[7:0]	TEST_DATA_GR_L	RW	TEST_DATA_GR_L	-	0x00
0x0608	[2:0]	TEST_DATA_RED_H	RW	TEST_DATA_RED_H	-	0x00
0x0609	[7:0]	TEST_DATA_RED_L	RW	TEST_DATA_RED_L	-	0x00

10.9 Black level control registers [0x1000 – 0x1009]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x1000	[0]	RESERVED	RW	RESERVED. Set to 1	-	0x01
0x1003	[7:0]	RESERVED	RW	RESERVED. Set to the same level as BLC target	-	0x20
0x1004	[7:0]	BLC_TGT	RW	Black level target 0-255	-	0x20
0x1007	[0]	RESERVED	RW	RESERVED. Set to 1	-	0x01
0x1008	[7:0]	RESERVED	RW	RESERVED. Set to the same level as BLC target	-	0x20
0x1009	[7:0]	BLC2_TGT	RW	BLC2 target. Set to the same level as BLC target	-	0x20

10.10 Monochrome programming registers [0x100A]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x100A	[1:0]	MONO_CTRL	RW	Mono control [1]: MONO_mode [0]: RESERVED, Set to 1	-	0x00

10.11 VSYNC / HSYNC / pixel shift registers [0x1014]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x1014	[5:0]	OPFM_CTRL	RW	Output format control [5]: 2-pixel mode option [4]: Parallel 8bits, 2-pixel mode [3]: PCLKO_gating_enable 0: PCLKO free-running 1: PCLKO gated by PCLKO_enable signal from timing control [2]: RESERVED [1]: HSYNC_shift_enable [0]: VSYNC_shift_enable	-	0x0F

10.12 Tone mapping registers [0x1030 – 0x103F]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x1030	[7:0]	CMPRS_01	RW	Compression_01	-	0x10
0x1031	[7:0]	CMPRS_02	RW	Compression_02	-	0x19
0x1032	[7:0]	CMPRS_03	RW	Compression_03	-	0x28
0x1033	[7:0]	CMPRS_04	RW	Compression_04	-	0x35
0x1034	[7:0]	CMPRS_05	RW	Compression_05	-	0x40
0x1035	[7:0]	CMPRS_06	RW	Compression_06	-	0x4A
0x1036	[7:0]	CMPRS_07	RW	Compression_07	-	0x54
0x1037	[7:0]	CMPRS_08	RW	Compression_08	-	0x5D
0x1038	[7:0]	CMPRS_09	RW	Compression_09	-	0x66
0x1039	[7:0]	CMPRS_10	RW	Compression_10	-	0x76
0x103A	[7:0]	CMPRS_11	RW	Compression_11	-	0x85
0x103B	[7:0]	CMPRS_12	RW	Compression_12	-	0x94
0x103C	[7:0]	CMPRS_13	RW	Compression_13	-	0xA1
0x103D	[7:0]	CMPRS_14	RW	Compression_14	-	0xBB
0x103E	[7:0]	CMPRS_15	RW	Compression_15	-	0xD3
0x103F	[7:0]	CMPRS_16	RW	Compression_16	-	0xEA

10.13 Automatic exposure programming registers [0x2000 – 0x2072]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x2000	[7:0]	AE_CTRL	RW	Auto Exposure control [7]: ALC_INT enable [6]: FR_ctrl_enable [5]: RESERVED [4]: AE_update_enable [3]: RESERVED [2]: RESERVED [1]: RESERVED [0]: AE enable	-	0x1F
0x2001	[4:0]	AE_CTRL1	RW	AE control 1 [4]: AEtarget_less_enable [3]: AEtarget_great_enable [2]: Emax_remap_enable [1]: AENC_INT enable [0]: STAT_INT enable	-	0x00
0x2002	[1:0]	CNT_ORG_H	RW	AE ROI x start location [9:8]	-	0x00
0x2003	[7:0]		RW	AE ROI x start location [7:0]	-	0x02
0x2004	[0]	CNT_ORG_V	RW	AE ROI y start location [8]	-	0x00
0x2005	[7:0]		RW	AE ROI y start location [7:0]	-	0x03
0x2006	[1:0]	CNT_ST_H	RW	AE ROI x cnt [9:8]	-	0x00
0x2007	[7:0]		RW	AE ROI x cnt [7:0]	-	0x82
0x2008	[0]	CNT_ST_V	RW	AE ROI y cnt [8]	-	0x00
0x2009	[7:0]		RW	AE ROI y cnt [7:0]	-	0x62
0x200A	[3:0]	CTRL_PG_SKIPCNT	RW	AE skip count control	-	0x01
0x200D	[0]	BV_WIN_WEIGHT_EN	RW	AE ROI Weight enable	-	0x01
0x200E	[7:0]	WINARRAY_1	RW	BV window 5x5 enable bit [7]: win23 [6]: win22 [5]: win21 [4]: win15 [3]: win14 [2]: win13 [1]: win12 [0]: win11	-	0xFF
0x200F	[7:0]	WINARRAY_2	RW	BV window 5x5 enable bit [7]: win41 [6]: win35 [5]: win34 [4]: win33 [3]: win32 [2]: win31 [1]: win25 [0]: win24	-	0xFF

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x2010	[7:0]	WINARRAY_3	RW	BV window 5x5 enable bit [7]: win54 [6]: win53 [5]: win52 [4]: win51 [3]: win45 [2]: win44 [1]: win43 [0]: win42	-	0xFF
0x2011	[0]	WINARRAY_4	RW	BV window 5x5 enable bit [0]: win55	-	0xFF
0x2012	[6:0]	WINWEIGHT_1_12	RW	Window weight 000: 0% 001: 12.5% 010: 25.0% 011: 50.0%, 100: 75.0%, 101: 87.5%, 110: 100% [6:4]: WinWeight_1_2 [2:0]: WinWeight_1_1	-	0x66
0x2013	[6:0]	WINWEIGHT_1_34	RW	[6:4]: WinWeight_1_4 [2:0]: WinWeight_1_3	-	0x66
0x2014	[2:0]	WINWEIGHT_1_5	RW	[2:0]: WinWeight_1_5	-	0x06
0x2015	[6:0]	WINWEIGHT_2_12	RW	[6:4]: WinWeight_2_2 [2:0]: WinWeight_2_1	-	0x66
0x2016	[6:0]	WINWEIGHT_2_34	RW	[6:4]: WinWeight_2_4 [2:0]: WinWeight_2_3	-	0x66
0x2017	[2:0]	WINWEIGHT_2_5	RW	[2:0]: WinWeight_2_5	-	0x06
0x2018	[6:0]	WINWEIGHT_3_12	RW	[6:4]: WinWeight_3_2 [2:0]: WinWeight_3_1	-	0x66
0x2019	[6:0]	WINWEIGHT_3_34	RW	[6:4]: WinWeight_3_4 [2:0]: WinWeight_3_3	-	0x66
0x201A	[2:0]	WINWEIGHT_3_5	RW	[2:0]: WinWeight_3_5	-	0x06
0x201B	[6:0]	WINWEIGHT_4_12	RW	[6:4]: WinWeight_4_2 [2:0]: WinWeight_4_1	-	0x66
0x201C	[6:0]	WINWEIGHT_4_34	RW	[6:4]: WinWeight_4_4 [2:0]: WinWeight_4_3	-	0x66
0x201D	[2:0]	WINWEIGHT_4_5	RW	[2:0]: WinWeight_4_5	-	0x06
0x201E	[6:0]	WINWEIGHT_5_12	RW	[6:4]: WinWeight_5_2 [2:0]: WinWeight_5_1	-	0x66
0x201F	[6:0]	WINWEIGHT_5_34	RW	[6:4]: WinWeight_5_4 [2:0]: WinWeight_5_3	-	0x66
0x2020	[2:0]	WINWEIGHT_5_5	RW	[2:0]: WinWeight_5_5	-	0x06
0x2029	[7:0]	MAX_INTG_H	RW	AE max INTG allowance H	-	0x02
0x202A	[7:0]	MAX_INTG_L	RW	AE max INTG allowance L	-	0x10
0x202B	[7:0]	MAX_AGAIN	RW	AE max AGAIN allowance	-	0x04
0x202C	[4:0]	MAX_DGAIN_H	RW	AE max DGAIN allowance H	-	0x03
0x202D	[5:0]	MAX_DGAIN_L	RW	AE max DGAIN allowance L	-	0x3F
0x202E	[7:0]	MIN_INTG	RW	AE min INTG allowance	-	0x00
0x202F	[7:0]	MIN_AGAIN	RW	AE min AGAIN allowance	-	0x00
0x2030	[7:0]	MIN_DGAIN	RW	AE min DGAIN allowance **(u2.6)**	-	0x40
0x2031	[7:0]	T_DAMPING	RW	AE T damping factor **(u1.7)**	-	0x20
0x2032	[4:0]	N_DAMPING	RW	AE N damping factor **(u0.5)**	-	0x00
0x2033	[7:0]	ALC_TH	RW	AE ALC mean difference TH	-	0x05
0x2034	[7:0]	AE_TARGET	RW	AE target	-	0x50
0x2035	[7:0]	MIN_MEAN	RW	AE min mean	-	0x08
0x2036	[7:0]	AE_TARGETZONE	RW	AE IIR Target Zone	-	0x23
0x2037	[7:0]	CONVERGE_IN_TH	RW	AE converge in threshold	-	0x08
0x2038	[7:0]	CONVERGE_OUT_TH	RW	AE converge out threshold	-	0x19
0x2039	[7:0]	RESERVED	RW	RESERVED	-	0x10
0x203A	[7:0]	RESERVED	RW	RESERVED	-	0x02

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x203B	[2:0]	FS_CTRL	RW	[2]: Flicker step hysteresis enable [1]: Flicker step select [0]: Flicker step enable	-	0x0B
0x203C	[7:0]	FS_60HZ_H	RW	AE flicker step H **(60Hz)**	-	0x01
0x203D	[7:0]	FS_60HZ_L	RW	AE flicker step L **(60Hz)**	-	0x1C
0x203E	[7:0]	FS_50HZ_H	RW	AE flicker step H **(50Hz)**	-	0x01
0x203F	[7:0]	FS_50HZ_H	RW	AE flicker step L **(50Hz)**	-	0x54
0x2042	[7:0]	FR_STAGE1_H	RW	Frame rate stage 1 High byte	-	0x02
0x2043	[7:0]	FR_STAGE1_L	RW	Frame rate stage 1 Low byte	-	0x12
0x2044	[7:0]	FR_STAGE2_H	RW	Frame rate stage 2 High byte	-	0x04
0x2045	[7:0]	FR_STAGE2_L	RW	Frame rate stage 2 Low byte	-	0x24
0x2046	[7:0]	FR_STAGE3_H	RW	Frame rate stage 3 High byte	-	0x06
0x2047	[7:0]	FR_STAGE3_L	RW	Frame rate stage 3 Low byte	-	0x36
0x2048	[6:0]	FR_EGPTH12_H	RW	FR ctrl EGP TH 12	-	0x00
0x2049	[7:0]	FR_EGPTH12_M	RW	FR ctrl EGP TH 12	-	0x1F
0x204A	[7:0]	FR_EGPTH12_L	RW	FR ctrl EGP TH 12	-	0x40
0x204B	[6:0]	FR_EGPTH21_H	RW	FR ctrl EGP TH 21	-	0x00
0x204C	[7:0]	FR_EGPTH21_M	RW	FR ctrl EGP TH 21	-	0x0E
0x204D	[7:0]	FR_EGPTH21_L	RW	FR ctrl EGP TH 21	-	0x10
0x204E	[6:0]	FR_EGPTH23_H	RW	FR ctrl EGP TH 23	-	0x00
0x204F	[7:0]	FR_EGPTH23_M	RW	FR ctrl EGP TH 23	-	0x7D
0x2050	[7:0]	FR_EGPTH23_L	RW	FR ctrl EGP TH 23	-	0x00
0x2051	[6:0]	FR_EGPTH32_H	RW	FR ctrl EGP TH 32	-	0x00
0x2052	[7:0]	FR_EGPTH32_M	RW	FR ctrl EGP TH 32	-	0x27
0x2053	[7:0]	FR_EGPTH32_L	RW	FR ctrl EGP TH 32	-	0x10
0x2054	[6:0]	RESERVED	RW	RESERVED	-	0x00
0x2055	[7:0]	RESERVED	RW	RESERVED	-	0xBB
0x2056	[7:0]	RESERVED	RW	RESERVED	-	0x80
0x2057	[6:0]	RESERVED	RW	RESERVED	-	0x00
0x2058	[7:0]	RESERVED	RW	RESERVED	-	0x0B
0x2059	[7:0]	RESERVED	RW	RESERVED	-	0xB8
0x205B	[7:0]	FRAME_CNT_TH	RW	AE ALC frame cnt	-	0x05
0x205D	[7:0]	AE_MEAN	RO	AE mean	-	0x00
0x2060	[0]	AE_CONVERGE	RO	AE converged	-	0x00
0x206F	[7:0]	RESERVED	RW	RESERVED	-	0x08
0x2070	[7:0]	AE_BLI_TGT	RW	AE BLI target	-	0x08
0x2071	[7:0]	AETARGET_TH0	RW	Threshold when AE mean > target_mean	-	0x64
0x2072	[7:0]	AETARGET_TH1	RW	Threshold when AE mean < target_mean	-	0x64

10.14 Interrupt programming registers [0x2061 – 0x2065]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x2061	[0]	PULSE_MODE	RW	0: INT level mode 1: INT pulse mode	-	0x00
0x2062	[7:0]	PULSE_TH_H	RW	INT pulse width	-	0x05
0x2063	[7:0]	PULSE_TH_L	RW	INT pulse width	-	0x80
0x2064	[7:0]	INT_INDIC	RO	INT indicator [7]: RESERVED [6]: AE converge [5]: Early VSYNC [4]: MD flicker INT [3]: MD INT [2]: AENC INT [1]: Stat INT [0]: ALC INT	-	0x00
0x2065	[5:0]	INT_CLEAR	RW	INT clear [5]: Early VSYNC [4]: RESERVED [3]: MD INT [2]: AENC INT [1]: Stat INT [0]: ALC INT	-	0x00

10.15 Motion detection control registers [0x2080 – 0x20C0]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x2080	[7:0]	MD_CTRL	RW	[7]: RESERVED [6]: RESERVED [5:4]: MD latency select [3:2]: RESERVED [1]: RESERVED [0]: Motion detect enable	-	0x01
0x2081	[7:0]	ROI_START_END_V	RW	[7:4]: ROI_END_V [3:0]: ROI_START_V	-	0xF0
0x2082	[7:0]	ROI_START_END_H	RW	[7:4]: ROI_END_H [3:0]: ROI_START_H	-	0xF0
0x2083	[6:0]	MD_TH_MIN	RW	Threshold min value	-	0x01
0x2084	[5:0]	MD_TH_STR_L	RW	Threshold strength	-	0x10
0x2085	[5:0]	MD_TH_STR_H	RW	Threshold strength	-	0x10
0x2086	[7:0]	MD_TH_COEF_0	RW	Motion detect threshold coefficient 0	-	0x01
0x2087	[7:0]	MD_TH_COEF_1	RW	Motion detect threshold coefficient 1	-	0x06
0x2088	[7:0]	MD_TH_COEF_2	RW	Motion detect threshold coefficient 2	-	0x0C
0x2089	[7:0]	MD_TH_COEF_3	RW	Motion detect threshold coefficient 3	-	0x12
0x208A	[7:0]	MD_TH_COEF_4	RW	Motion detect threshold coefficient 4	-	0x1B
0x208B	[7:0]	MD_TH_COEF_5	RW	Motion detect threshold coefficient 5	-	0x27
0x208C	[5:0]	RESERVED	RW	RESERVED	-	0x10
0x208D	[7:0]	RESERVED	RW	RESERVED	-	0x03
0x208E	[7:0]	RESERVED	RW	RESERVED	-	0x09
0x208F	[7:0]	RESERVED	RW	RESERVED	-	0x0F
0x2090	[7:0]	RESERVED	RW	RESERVED	-	0x17
0x2091	[7:0]	RESERVED	RW	RESERVED	-	0x1F
0x2092	[7:0]	RESERVED	RW	RESERVED	-	0x2C
0x2093	[5:0]	MD_TG_COEF_1	RW	md_tg_coef_1	-	0x08
0x2094	[5:0]	MD_TG_COEF_2	RW	md_tg_coef_2	-	0x10
0x2095	[5:0]	MD_TG_COEF_3	RW	md_tg_coef_3	-	0x16
0x2096	[5:0]	MD_TG_COEF_4	RW	md_tg_coef_4	-	0x20
0x2097	[5:0]	MD_TG_COEF_5	RW	md_tg_coef_5	-	0x2D
0x2098	[5:0]	MD_TG_COEF_6	RW	md_tg_coef_6	-	0x3F
0x2099	[6:0]	MD_LIGHT_COEF	RW	md_light_coef	-	0x00
0x209A	[7:0]	MD_IIR_PARAMETER	RW	IIR Filter	-	0x81
0x209B	[7:0]	MD_BLOCK_NUM_TH	RW	MD_block_number threshold	-	0x01
0x209C	[4:0]	MD_LATENCY	RW	MD_latency_frame	-	0x01
0x209D	[7:0]	MD_LATENCY_TH	RW	[7:4]: md_latency_s_threshold [3:0]: md_latency_m_threshold	-	0x11
0x209E	[2:0]	MD_CTRL1	RW	MD_interrupt_control [2]: RESERVED [1]: Motion interrupt enable [0]: Motion interrupt select 0: Original flag 1: Latency flag	-	0x06
0x20A1	[7:0]	MD_ROI_OUT_0	RO	md_roi_map_out[7:0]	-	0x00
0x20A2	[7:0]	MD_ROI_OUT_1	RO	md_roi_map_out[15:8]	-	0x00
0x20A3	[7:0]	MD_ROI_OUT_2	RO	md_roi_map_out[23:16]	-	0x00
0x20A4	[7:0]	MD_ROI_OUT_3	RO	md_roi_map_out[31:24]	-	0x00
0x20A5	[7:0]	MD_ROI_OUT_4	RO	md_roi_map_out[39:32]	-	0x00
0x20A6	[7:0]	MD_ROI_OUT_5	RO	md_roi_map_out[47:40]	-	0x00
0x20A7	[7:0]	MD_ROI_OUT_6	RO	md_roi_map_out[55:48]	-	0x00
0x20A8	[7:0]	MD_ROI_OUT_7	RO	md_roi_map_out[63:56]	-	0x00
0x20A9	[7:0]	MD_ROI_OUT_8	RO	md_roi_map_out[71:64]	-	0x00
0x20AA	[7:0]	MD_ROI_OUT_9	RO	md_roi_map_out[79:72]	-	0x00
0x20AB	[7:0]	MD_ROI_OUT_10	RO	md_roi_map_out[87:80]	-	0x00

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x20AC	[7:0]	MD_ROI_OUT_11	RO	md_roi_map_out[95:88]	-	0x00
0x20AD	[7:0]	MD_ROI_OUT_12	RO	md_roi_map_out[103:96]	-	0x00
0x20AE	[7:0]	MD_ROI_OUT_13	RO	md_roi_map_out[111:104]	-	0x00
0x20AF	[7:0]	MD_ROI_OUT_14	RO	md_roi_map_out[119:112]	-	0x00
0x20B0	[7:0]	MD_ROI_OUT_15	RO	md_roi_map_out[127:120]	-	0x00
0x20B1	[7:0]	MD_ROI_OUT_16	RO	md_roi_map_out[135:128]	-	0x00
0x20B2	[7:0]	MD_ROI_OUT_17	RO	md_roi_map_out[143:136]	-	0x00
0x20B3	[7:0]	MD_ROI_OUT_18	RO	md_roi_map_out[151:144]	-	0x00
0x20B4	[7:0]	MD_ROI_OUT_19	RO	md_roi_map_out[159:152]	-	0x00
0x20B5	[7:0]	MD_ROI_OUT_20	RO	md_roi_map_out[167:160]	-	0x00
0x20B6	[7:0]	MD_ROI_OUT_21	RO	md_roi_map_out[175:168]	-	0x00
0x20B7	[7:0]	MD_ROI_OUT_22	RO	md_roi_map_out[183:176]	-	0x00
0x20B8	[7:0]	MD_ROI_OUT_23	RO	md_roi_map_out[191:184]	-	0x00
0x20B9	[7:0]	MD_ROI_OUT_24	RO	md_roi_map_out[199:192]	-	0x00
0x20BA	[7:0]	MD_ROI_OUT_25	RO	md_roi_map_out[207:200]	-	0x00
0x20BB	[7:0]	MD_ROI_OUT_26	RO	md_roi_map_out[215:208]	-	0x00
0x20BC	[7:0]	MD_ROI_OUT_27	RO	md_roi_map_out[223:216]	-	0x00
0x20BD	[7:0]	MD_ROI_OUT_28	RO	md_roi_map_out[231:224]	-	0x00
0x20BE	[7:0]	MD_ROI_OUT_29	RO	md_roi_map_out[239:232]	-	0x00
0x20BF	[7:0]	MD_ROI_OUT_30	RO	md_roi_map_out[247:240]	-	0x00
0x20C0	[7:0]	MD_ROI_OUT_31	RO	md_roi_map_out[255:248]	-	0x00

10.16 OTP programming registers [0x2500 – 0x25FF]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x2500	[0]	PAGE_NUMBER	RW	[0]: OTP Page Number	-	0x00
0x2501	[5:0]	PAGE_OFFSET	RW	[5:0]: OTP Page Read/Write Start Offset	-	0x00
0x2502	[6:0]	OTP_LENGTH	RW	[6:0]: OTP Read/Write Length	-	0x40
0x2503	[1:0]	OTP_COMMAND	RW	[1]: OTP Read procedure trigger start [0]: OTP Write procedure trigger start	-	0x00
0x2504	[1:0]	OTP_STATUS	RO	[1]: OTP Write Processing Indicator. [0]: OTP Read Processing Indicator.	-	0x00
0x250A	[1]	OTP_ PDSTB _control 1	RW	[1]: OTP PDSTB pin manual control enable	-	0x00
0x2511	[3]	OTP_ PDSTB _control	RW	[3]: OTP PDSTB pin manual control	-	0x00
0x25C0	[7:0]	OTP_USER_BYTE0	RW	OTP data space	-	0x00
0x25C1	[7:0]	OTP_USER_BYTE1	RW	OTP data space	-	0x00
0x25C2	[7:0]	OTP_USER_BYTE2	RW	OTP data space	-	0x00
0x25C3	[7:0]	OTP_USER_BYTE3	RW	OTP data space	-	0x00
0x25C4	[7:0]	OTP_USER_BYTE4	RW	OTP data space	-	0x00
0x25C5	[7:0]	OTP_USER_BYTE5	RW	OTP data space	-	0x00
0x25C6	[7:0]	OTP_USER_BYTE6	RW	OTP data space	-	0x00
0x25C7	[7:0]	OTP_USER_BYTE7	RW	OTP data space	-	0x00
0x25C8	[7:0]	OTP_USER_BYTE8	RW	OTP data space	-	0x00
0x25C9	[7:0]	OTP_USER_BYTE9	RW	OTP data space	-	0x00
0x25CA	[7:0]	OTP_USER_BYTE10	RW	OTP data space	-	0x00
0x25CB	[7:0]	OTP_USER_BYTE11	RW	OTP data space	-	0x00
0x25CC	[7:0]	OTP_USER_BYTE12	RW	OTP data space	-	0x00
0x25CD	[7:0]	OTP_USER_BYTE13	RW	OTP data space	-	0x00
0x25CE	[7:0]	OTP_USER_BYTE14	RW	OTP data space	-	0x00
0x25CF	[7:0]	OTP_USER_BYTE15	RW	OTP data space	-	0x00
0x25D0	[7:0]	OTP_USER_BYTE16	RW	OTP data space	-	0x00
0x25D1	[7:0]	OTP_USER_BYTE17	RW	OTP data space	-	0x00
0x25D2	[7:0]	OTP_USER_BYTE18	RW	OTP data space	-	0x00
0x25D3	[7:0]	OTP_USER_BYTE19	RW	OTP data space	-	0x00
0x25D4	[7:0]	OTP_USER_BYTE20	RW	OTP data space	-	0x00
0x25D5	[7:0]	OTP_USER_BYTE21	RW	OTP data space	-	0x00
0x25D6	[7:0]	OTP_USER_BYTE22	RW	OTP data space	-	0x00
0x25D7	[7:0]	OTP_USER_BYTE23	RW	OTP data space	-	0x00
0x25D8	[7:0]	OTP_USER_BYTE24	RW	OTP data space	-	0x00
0x25D9	[7:0]	OTP_USER_BYTE25	RW	OTP data space	-	0x00
0x25DA	[7:0]	OTP_USER_BYTE26	RW	OTP data space	-	0x00
0x25DB	[7:0]	OTP_USER_BYTE27	RW	OTP data space	-	0x00
0x25DC	[7:0]	OTP_USER_BYTE28	RW	OTP data space	-	0x00
0x25DD	[7:0]	OTP_USER_BYTE29	RW	OTP data space	-	0x00
0x25DE	[7:0]	OTP_USER_BYTE30	RW	OTP data space	-	0x00
0x25DF	[7:0]	OTP_USER_BYTE31	RW	OTP data space	-	0x00
0x25E0	[7:0]	OTP_USER_BYTE32	RW	OTP data space	-	0x00
0x25E1	[7:0]	OTP_USER_BYTE33	RW	OTP data space	-	0x00
0x25E2	[7:0]	OTP_USER_BYTE34	RW	OTP data space	-	0x00
0x25E3	[7:0]	OTP_USER_BYTE35	RW	OTP data space	-	0x00
0x25E4	[7:0]	OTP_USER_BYTE36	RW	OTP data space	-	0x00
0x25E5	[7:0]	OTP_USER_BYTE37	RW	OTP data space	-	0x00
0x25E6	[7:0]	OTP_USER_BYTE38	RW	OTP data space	-	0x00
0x25E7	[7:0]	OTP_USER_BYTE39	RW	OTP data space	-	0x00
0x25E8	[7:0]	OTP_USER_BYTE40	RW	OTP data space	-	0x00
0x25E9	[7:0]	OTP_USER_BYTE41	RW	OTP data space	-	0x00
0x25EA	[7:0]	OTP_USER_BYTE42	RW	OTP data space	-	0x00
0x25EB	[7:0]	OTP_USER_BYTE43	RW	OTP data space	-	0x00
0x25EC	[7:0]	OTP_USER_BYTE44	RW	OTP data space	-	0x00

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x25ED	[7:0]	OTP_USER_BYTE45	RW	OTP data space	-	0x00
0x25EE	[7:0]	OTP_USER_BYTE46	RW	OTP data space	-	0x00
0x25EF	[7:0]	OTP_USER_BYTE47	RW	OTP data space	-	0x00
0x25F0	[7:0]	OTP_USER_BYTE48	RW	OTP data space	-	0x00
0x25F1	[7:0]	OTP_USER_BYTE49	RW	OTP data space	-	0x00
0x25F2	[7:0]	OTP_USER_BYTE50	RW	OTP data space	-	0x00
0x25F3	[7:0]	OTP_USER_BYTE51	RW	OTP data space	-	0x00
0x25F4	[7:0]	OTP_USER_BYTE52	RW	OTP data space	-	0x00
0x25F5	[7:0]	OTP_USER_BYTE53	RW	OTP data space	-	0x00
0x25F6	[7:0]	OTP_USER_BYTE54	RW	OTP data space	-	0x00
0x25F7	[7:0]	OTP_USER_BYTE55	RW	OTP data space	-	0x00
0x25F8	[7:0]	OTP_USER_BYTE56	RW	OTP data space	-	0x00
0x25F9	[7:0]	OTP_USER_BYTE57	RW	OTP data space	-	0x00
0x25FA	[7:0]	OTP_USER_BYTE58	RW	OTP data space	-	0x00
0x25FB	[7:0]	OTP_USER_BYTE59	RW	OTP data space	-	0x00
0x25FC	[7:0]	OTP_USER_BYTE60	RW	OTP data space	-	0x00
0x25FD	[7:0]	OTP_USER_BYTE61	RW	OTP data space	-	0x00
0x25FE	[7:0]	OTP_USER_BYTE62	RW	OTP data space	-	0x00
0x25FF	[7:0]	OTP_USER_BYTE63	RW	OTP data space	-	0x00

10.17 MIPI programming registers [0x2800 – 0x2822]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x2800	[0]	MIPI_EN	RW	[0]: MIPI enable	-	0x05
0x2821	[7:0]	LANE_CFG	RW	[7]: Clock lane on [6:5]: Clock lane option 00: Clock always on 01: Clock on while sending packet 10: Clock on during frame 11: Clock on during line [4]: Use LS/LE [3:0]: RESERVED	-	0xDE
0x2822	[0]	EMB_DATA_CFG	RW	[0]: Embedded data CFG 0: Treat embedded line as pixel data 1: Treat embedded line MIPI protocol	-	0x00

10.18 SYNC function control registers [0x3010 – 0x301C]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3010	[1]	EXP_SYNC_CFG	RW	[1]: Read Field Sync enable	-	0x00
0x3013	[0]	ERR_FLAG_CFG	RW	[0]: Error Flag self-clear enable	-	0x01
0x3019	[7:0]	OFFSET_RDSYNC_H	RW	[7]: Sign bit [6:0]: Adjust the delay between FVLD and FSIN input signal.	-	0x00
0x301A	[7:0]	OFFSET_RDSYNC_L	RW	[7:0]: Adjust the delay between FVLD and FSIN input signal.	-	0x00
0x301B	[7:0]	RDSYNC_DEC_TH_H	RW	Threshold for Out-of-Sync in Read Synchronization mode	-	0x20
0x301C	[7:0]	RDSYNC_DEC_T_L	RW	Threshold for Out-of-Sync in Read Synchronization mode	-	0x80

10.19 Context switch control registers [0x3024 – 0x3025]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3024	[3:0]	PMU_CFG_3	RW	CXT_SEL [3]: CXT disable [2]: AUTO CXT enable [1]: PAD_SEL enable 0: SW, I2C 1: HW, CTX_SEL pin [0]: SW **(I2C)** triggered 0: Context A 1: Context B	-	0x02
0x3025	[7:0]	PMU_CFG_4	RW	CXT_SEQ_FCNT [7:4]: Context B frame counter [3:0]: Context A frame counter	-	0x12

10.20 Operation mode registers [0x3026 – 0x302A]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3026	[3:0]	PMU_CFG_5	RW	Premeter_CFG [3]: Premeter mode at METER pin [2]: Premeter mode at light change [1]: Premeter enable at every wakeup [0]: Premeter enabled at power up	-	0x0F
0x3027	[7:4] [0]	PMU_CFG_6	RW	[7:4]: Premeter time limit Higher value delays output frame but increases accuracy of Premeter at wake up [0]: Enable time limit on Premeter	-	0x21
0x3028	[7:0]	PMU_CFG_7	RW	Output frame count	-	0x01
0x3029	[7:0]	PMU_CFG_8	RW	Sleep count H	-	0x00
0x302A	[7:0]	PMU_CFG_9	RW	Sleep count L	-	0x10

10.21 ROI and sensor control registers [0x3030 – 0x307F]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3030	[0]	WIN_MODE	RW	[0]: Pixel window 0: 656 x 496 resolution 1: 640 x 480 resolution	-	0x00
0x3032	[0]	N_PLUS_MODE_EN	RW	[0]: N+1 CMU update	-	0x01
0x3034	[0]	RESERVED	RW	RESERVED	-	0x00
0x3035	[0]	RESERVED	RW	RESERVED	-	0x00
0x3060	[0]	ROI_CFG	RW	[0]: ROI enable	-	0x00
0x3061	[7:0]	ROI_WIN_NUMBER	RW	[7:4]: Vertical window number [3:0]: Horizontal window number	-	0xFA
0x3062	[1:0]	ROI_WIN_ONE_H	RW	1st row of vertical window	-	0xFF
0x3063	[7:0]	ROI_WIN_ONE_L	RW	1st row of vertical window	-	0xFF
0x3064	[1:0]	ROI_WIN_TWO_H	RW	2nd row of vertical window	-	0xFF
0x3065	[7:0]	ROI_WIN_TWO_L	RW	2nd row of vertical window	-	0xFF
0x3066	[1:0]	ROI_WIN_THIRD_H	RW	3rd row of vertical window	-	0xFF
0x3067	[7:0]	ROI_WIN_THIRD_L	RW	3rd row of vertical window	-	0xFF
0x3068	[1:0]	ROI_WIN_FOUR_H	RW	4th row of vertical window	-	0xFF
0x3069	[7:0]	ROI_WIN_FOUR_L	RW	4th row of vertical window	-	0xFF
0x306A	[1:0]	ROI_WIN_FIVE_H	RW	5th row of vertical window	-	0xFF
0x306B	[7:0]	ROI_WIN_FIVE_L	RW	5th row of vertical window	-	0xFF
0x306C	[1:0]	ROI_WIN_SIX_H	RW	6th row of vertical window	-	0xFF
0x306D	[7:0]	ROI_WIN_SIX_L	RW	6th row of vertical window	-	0xFF
0x306E	[1:0]	ROI_WIN_SEVEN_H	RW	7th row of vertical window	-	0xFF
0x306F	[7:0]	ROI_WIN_SEVEN_L	RW	7th row of vertical window	-	0xFF
0x3070	[1:0]	ROI_WIN_EIGHT_H	RW	8th row of vertical window	-	0xFF
0x3071	[7:0]	ROI_WIN_EIGHT_L	RW	8th row of vertical window	-	0xFF
0x3072	[1:0]	ROI_WIN_NINE_H	RW	9th row of vertical window	-	0xFF
0x3073	[7:0]	ROI_WIN_NINE_L	RW	9th row of vertical window	-	0xFF
0x3074	[1:0]	ROI_WIN_TEN_H	RW	10th row of vertical window	-	0xFF
0x3075	[7:0]	ROI_WIN_TEN_L	RW	10th row of vertical window	-	0xFF
0x3076	[1:0]	ROI_WIN_ELEVEN_H	RW	11th row of vertical window	-	0xFF
0x3077	[7:0]	ROI_WIN_ELEVEN_L	RW	11th row of vertical window	-	0xFF
0x3078	[1:0]	ROI_WIN_TWELVE_H	RW	12th row of vertical window	-	0xFF
0x3079	[7:0]	ROI_WIN_ TWELVE_L	RW	12th row of vertical window	-	0xFF
0x307A	[1:0]	ROI_WIN_THIRTEEN_H	RW	13th row of vertical window	-	0xFF
0x307B	[7:0]	ROI_WIN_THIRTEEN_L	RW	13th row of vertical window	-	0xFF
0x307C	[1:0]	ROI_WIN_FOURTEEN_H	RW	14th row of vertical window	-	0xFF
0x307D	[7:0]	ROI_WIN_FOURTEEN_L	RW	14th row of vertical window	-	0xFF
0x307E	[1:0]	ROI_WIN_FIFTEEN_H	RW	15th row of vertical window	-	0xFF
0x307F	[7:0]	ROI_WIN_FIFTEEN_L	RW	15th row of vertical window	-	0xFF

10.22 Strobe control registers [0x3080 – 0x3089]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3080	[7] [4:0]	STROBE_CFG	RW	[7]: RESERVED [4]: Multiple Strobe Enable 0: always output strobe in frame base 1: output multiple strobe by frame counter value [3]: Programmable Endpoint enable [2]: Static mode [1]: Dynamic mode [0]: Strobe function enable	-	0x00
0x3081	[0]	STROBE_SEL	RW	[0]: strobe selection 0: Align to start of reset field 1: Align to end of reset field	-	0x00
0x3082	[7:0]	STROBE_FRONT_H	RW	Strobe Front Porch **(clk base)**	-	0x00
0x3083	[7:0]	STROBE_FRONT_L	RW	Strobe Front Porch **(clk base)**	-	0x20
0x3084	[7:0]	STROBE_END_H	RW	Strobe End Porch **(clk base)**	-	0x00
0x3085	[7:0]	STROBE_END_L	RW	Strobe End Porch **(clk base)**	-	0x20
0x3086	[7:0]	STROBE_LINE_H	RW	Strobe Line H **(row base)**	-	0x00
0x3087	[7:0]	STROBE_LINE_L	RW	Strobe Line L **(row base)**	-	0x20
0x3088	[7:0]	STROBE_FRAME_H	RW	Multiple Strobe Frame H	-	0x00
0x3089	[7:0]	STROBE_FRAME_H	RW	Multiple Strobe Frame L	-	0x04

10.23 IO and clock control registers [0x3094 – 0x3128]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3094	[7:0]	VSYNC_FRONT	RW	Early VSYNC Front porch register	-	0x00
0x3095	[7:0]	VSYNC_END	RW	Early VSYNC End porch register	-	0x00
0x3096	[7:0]	HSYNC_FRONT_H	RW	Early HSYNC Front porch register	-	0x00
0x3097	[7:0]	HSYNC_FRONT_L	RW	Early HSYNC Front porch register	-	0x00
0x3098	[7:0]	HSYNC_ END_H	RW	Early HSYNC End porch register	-	0x00
0x3099	[7:0]	HSYNC_ END_L	RW	Early HSYNC End porch register	-	0x00
0x309A	[7:0]	READ_PU_FRONT	RW	Read_PU Front porch register	-	0x01
0x309B	[7:0]	READ_PU_End	RW	Read_PU End porch register	-	0x08
0x309C	[0]	EARLY_INT_EN	RW	[0]: Early interrupt enable	-	0x00
0x309E	[1:0]	PCLKO_GATED_EN	RW	[1]: Gated by line [0]: Gated by frame	-	0x01
0x309F	[7:0]	PCLKO_FRAME_FRONT	RW	PCLKO Frame-based front porch register **(row adjustment)**	-	0x02
0x30A0	[7:0]	PCLKO_FRAME_END	RW	PCLKO Frame-based end porch register **(row adjustment)**	-	0x02
0x30A1	[7:0]	PCLKO_LINE_FRONT_H	RW	PCLKO Line-based front porch register **(clock adjustment)**	-	0x00
0x30A2	[7:0]	PCLKO_LINE_FRONT_L	RW	PCLKO Line-based front porch register **(clock adjustment)**	-	0x00
0x30A3	[7:0]	PCLKO_LINE_END_H	RW	PCLKO Line-based end porch register **(clock adjustment)**	-	0x00
0x30A4	[7:0]	PCLKO_LINE_END_L	RW	PCLKO Line-based end porch register **(clock adjustment)**	-	0x00
0x30A5	[2:0]	OUTPUT_EN	RW	[2]: PCLKO continuous mode [1]: Trigger on/off mode [0]: VSYNC mode	-	0x01
0x30A8	[2:0]	FRAME_OUTPUT_EN	RW	[2]: Mask out enable for AE non-converged frame [1]: Mask out enable for MIPI output [0]: Mask out enable for parallel output	-	0x01
0x30A9	[1:0]	MULTI_CAMERA_CONFIG	RW	[1]: MODE 2 [0]: MODE 1	-	0x00
0x30AA	[7:0]	MULTI_CAMERA_TUNE_H	RW	MULTI CAMERA MODE 2 tuning register	-	0x02
0x30AB	[7:0]	MULTI_CAMERA_TUNE_L	RW	MULTI CAMERA MODE 2 tuning register	-	0x34
0x310E	[6:0]	ANA_REGISTER_03	RW	[6:4]: d0_slew_d [3:1]: vld_slew_d [0]: enable_highz_d	-	0x01
0x310F	[7:0]	ANA_REGISTER_04	RW	[7]: srl_enable_1b_d [6]: srl_enable_4b_d [5:3]: d7_slew_d [2:0]: d3_slew_d	-	0x00
0x3110	[7:6] [2:0]	ANA_REGISTER_05	RW	[7]: drv0_enable_d [6]: enable_res_in_pull0_d [2:0]: pclko_slew_d	-	0x44
0x3111	[2:0]	ANA_REGISTER_06	RW	[2:0]: s_d	-	0x00
0x3112	[3:0]	ANA_REGISTER_07	RW	[3]: msb_first_d [2]: PCLKO_polarity [1]: RESERVED [0]: RESERVED	-	0x00
0x3119	[4:0]	User Space Reg Control Byte	RW	[4:1]: RESERVED [0]: otp_pump_en	-	0x1E
0x3128	[7:0]	PLL_POST_DIV_D	RW	[7:0]: PLL post divider	-	0x00

10.24 I2C slave registers [0x3400 – 0x3401]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3400	[0]	I2C_ID_SEL	RW	[0]: I2C ID Selection 0: Vendor defined 1: User defined	-	0x00
0x3401	[6:0]	I2C_ID_REG	RW	[6:0]: User defined I2C ID	-	0x30

10.25 Context switch A registers [0x3500 – 0x3559]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x3500	[7:0]	PLL1CFG	RW	[7]: RESERVED [6]: PLL PRE DIVIDER [3] [5:4]: CLK_I2C divider 00: /2 01: /4 10: /6 11: /8 [3:2]: PCLKO divider 00: /1 01: /1 10: /2 11: /4 [1:0]: CLK_TB divider 00: /1 01: /2 10: /4 11: /8	-	0x04
0x3501	[7:0]	PLL2CFG	RW	[7:6]: Reserved [5:4]: mipi_clk = pll output 00: /2 01: /4 10: /8 11: /16 [3]: Reserved [2:0]: Reserved	-	0x0A
0x3502	[7:0]	PLL3CFG	RW	[7:5]: PLL PRE DIVIDER [2:0] [4:0]: Divider for 24MHz to 1MHz	-	0x78
0x3503	[7:0]	FRAME_LENGTH_LINES_H	RW	Frame_length_lines **(16-bit UINT)**	-	0x02
0x3504	[7:0]	FRAME_LENGTH_LINES_L	RW		-	0x14
0x3505	[7:0]	LINE_LENGTH_PCK_H	RW	Line_length_pck **(16-bit UINT)**	-	0x03
0x3506	[7:0]	LINE_LENGTH_PCK_L	RW		-	0x00
0x3507	[1:0]	H_SUB	RW	[1:0]: Horizontal Operation 00: Full frame 01: Sub2 10: Sub4	-	0x00
0x3508	[1:0]	V_SUB	RW	[1:0]: Vertical Operation 00: Full frame 01: Sub2 10: Sub4	-	0x00
0x3509	[1:0]	BIN_MODE	RW	Binning Operation [1]: Horizontal Binning [0]: Vertical binning	-	0x00
0x350A	[7:0]	RESERVED	RW	RESERVED	-	0xFF
0x350B	[0]	MONO_MODE_ISP	RW	[0]: Mono Mode for ISP block	-	0x01
0x350C	[0]	N_PLUS_MODE_EN	RW	[0]: N+1 CMU update	-	0x01

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x350D	[0]	WIN_MODE	RW	[0]: Pixel window 0: 656 x 496 resolution 1: 640 x 480 resolution	-	0x01
0x350E	[0]	ROI_CFG	RW	[0]: ROI enable	-	0x00
0x350F	[0]	EARLY_INT_EN	RW	[0]: Early interrupt enable	-	0x00
0x3510	[2:0]	FRAME_OUTPUT_EN	RW	[2]: Mask out enable for AE non-converged frame [1]: Mask out enable for MIPI output [0]: Mask out enable for parallel output	-	0x01
0x3511	[0]	EMBEDDED_LINE_EN	RW	[0]: Embedded data enable	-	0x01
0x3512	[7:0]	AE_CTRL	RW	AE control [7]: ALC_INT enable [6]: Frame Rate control enable [5]: RESERVED [4]: AE Update enable [3]: RESERVED [2]: RESERVED [1]: RESERVED [0]: AE enable	-	0x1F
0x3513	[4:0]	AE_CTRL1	RW	AE control 1 [4]: AEtarget_less_enable [3]: AEtarget_great_enable [2]: Exposure remap enable [1]: AENC_INT enable [0]: AE Statistics INT enable	-	0x00
0x3514	[1:0]	CNT_ORG_H	RW	AE ROI x start location [9:8]	-	0x00
0x3515	[7:0]		RW	AE ROI x start location [7:0]	-	0x01
0x3516	[0]	CNT_ORG_V	RW	AE ROI y start location [8]	-	0x00
0x3517	[7:0]		RW	AE ROI y start location [7:0]	-	0x02
0x3518	[1:0]	CNT_ST_H	RW	AE ROI x cnt [9:8]	-	0x00
0x3519	[7:0]		RW	AE ROI x cnt [7:0]	-	0x7F
0x351A	[0]	CNT_ST_V	RW	AE ROI y cnt [8]	-	0x00
0x351B	[7:0]		RW	AE ROI y cnt [7:0]	-	0x5F
0x351C	[3:0]	CTRL_PG_SKIPCNT	RW	AE skip count control	-	0x00
0x351D	[7:0]	MAX_INTG_H	RW	AE max INTG allowance H	-	0x02
0x351E	[7:0]	MAX_INTG_L	RW	AE max INTG allowance L	-	0x10
0x351F	[7:0]	MAX_AGAIN	RW	AE max AGAIN allowance	-	0x04
0x3520	[4:0]	MAX_DGAIN_H	RW	AE max DGAIN allowance H	-	0x03
0x3521	[5:0]	MAX_DGAIN_L	RW	AE max DGAIN allowance L	-	0x3F
0x3522	[7:0]	MIN_INTG	RW	AE min INTG allowance	-	0x00
0x3523	[7:0]	T_DAMPING	RW	AE T damping factor **(u1.7)**	-	0x20
0x3524	[4:0]	N_DAMPING	RW	AE N damping factor **(u0.5)**	-	0x00
0x3525	[7:0]	AE_TARGETZONE	RW	AE IIR Target Zone	-	0x23
0x3526	[7:0]	CONVERGE_IN_TH	RW	AE converge in threshold	-	0x08
0x3527	[7:0]	CONVERGE_OUT_TH	RW	AE converge out threshold	-	0x19
0x3528	[7:0]	RESERVED	RW	RESERVED	-	0x10
0x3529	[7:0]	RESERVED	RW	RESERVED	-	0x02
0x352A	[7:0]	FS_60HZ_H	RW	AE flicker step H **(60Hz)**	-	0x01
0x352B	[7:0]	FS_60HZ_L	RW	AE flicker step L **(60Hz)**	-	0x1C
0x352C	[7:0]	FS_50HZ_H	RW	AE flicker step H **(50Hz)**	-	0x01
0x352D	[7:0]	FS_50HZ_H	RW	AE flicker step L **(50Hz)**	-	0x54
0x352E	[7:0]	FR_STAGE1_H	RW	Frame rate stage 1 High byte	-	0x02
0x352F	[7:0]	FR_STAGE1_L	RW	Frame rate stage 1 Low byte	-	0x12
0x3530	[7:0]	FR_STAGE2_H	RW	Frame rate stage 2 High byte	-	0x04
0x3531	[7:0]	FR_STAGE2_L	RW	Frame rate stage 2 Low byte	-	0x24
0x3532	[7:0]	FR_STAGE3_H	RW	Frame rate stage 3 High byte	-	0x06
0x3533	[7:0]	FR_STAGE3_L	RW	Frame rate stage 3 Low byte	-	0x36
0x354B	[7:0]	MD_CTRL	RW	[7:1]: Motion detect light coefficient [0]: Motion detect enable	-	0x01
0x354C	[7:0]	MD_BLOCK_NUM_TH	RW	MD_block_number threshold	-	0x01

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x354D	[7:0]	ROI_START_END_V	RW	[7:4]: ROI_END_V [3:0]: ROI_START_V	-	0xF0
0x354E	[7:0]	ROI_START_END_H	RW	[7:4]: ROI_END_H [3:0]: ROI_START_H	-	0xF0
0x354F	[7:0]	MD_TH_STR_H	RW	Threshold strength	-	0x10
0x3550	[7:0]	MD_TH_STR_L	RW	Threshold strength	-	0x10
0x3551	[7:0]	RESERVED	RW	RESERVED	-	0x10
0x3552	[7:0]	MD_FLICK_TH_ADJ_N	RW	Motion detect flicker threshold adjustment N	-	0x52
0x3553	[7:0]	MD_FLICK_TH_ADJ_P	RW	Motion detect flicker threshold adjustment P	-	0x53
0x3554	[7:0]	MD_TH_COEF_0	RW	Motion detect threshold coefficient 0	-	0x01
0x3555	[7:0]	MD_TH_COEF_1	RW	Motion detect threshold coefficient 1	-	0x06
0x3556	[7:0]	MD_TH_COEF_2	RW	Motion detect threshold coefficient 2	-	0x0C
0x3557	[7:0]	MD_TH_COEF_3	RW	Motion detect threshold coefficient 3	-	0x12
0x3558	[7:0]	MD_TH_COEF_4	RW	Motion detect threshold coefficient 4	-	0x1B
0x3559	[7:0]	MD_TH_COEF_5	RW	Motion detect threshold coefficient 5	-	0x27

10.26 Context switch B registers [0x355A – 0x35B3]

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x355A	[7:0]	PLL1CFG	RW	[7]: RESERVED [6]: PLL PRE DIVIDER [3] [5:4]: CLK_I2C divider 00: /2 01: /4 10: /6 11: /8 [3:2]: PCLKO divider 00: /1 01: /1 10: /2 11: /4 [1:0]: CLK_TB divider 00: /1 01: /2 10: /4 11: /8	-	0x04
0x355B	[7:0]	PLL2CFG	RW	[7:6]: Reserved [5:4]: mipi_cll = pll output 00: /2 01: /4 10: /8 11: /16 [3]: Reserved [2:0]: Reserved	-	0x0A
0x355C	[7:0]	PLL3CFG	RW	[7:5]: PLL PRE DIVIDER [2:0] [4:0]: Divider for 24MHz to 1MHz	-	0x78
0x355D	[7:0]	FRAME_LENGTH_LINES_H	RW	Frame_length_lines **(16-bit UINT)**	-	0x01
0x355E	[7:0]	FRAME_LENGTH_LINES_L	RW		-	0x0A
0x355F	[7:0]	LINE_LENGTH_PCK_H	RW	Line_length_pck **(16-bit UINT)**	-	0x03
0x3560	[7:0]	LINE_LENGTH_PCK_L	RW		-	0x00
0x3561	[1:0]	H_SUB	RW	[1:0]: Horizontal Operation 00: Full frame 01: Sub2 10: Sub4	-	0x01
0x3562	[1:0]	V_SUB	RW	[1:0]: Vertical Operation 00: Full frame 01: Sub2 10: Sub4	-	0x01
0x3563	[1:0]	BIN_MODE	RW	Binning Operation [1]: Horizontal Binning [0]: Vertical binning	-	0x00
0x3564	[7:0]	RESERVED	RW	RESERVED	-	0x55
0x3565	[0]	MONO_MODE_ISP	RW	[0]: Mono Mode for ISP block	-	0x01
0x3566	[0]	N_PLUS_MODE_EN	RW	[0]: N+1 CMU update	-	0x01
0x3567	[0]	WIN_MODE	RW	[0]: Pixel window 0: 656 x 496 resolution 1: 640 x 480 resolution	-	0x01
0x3568	[0]	ROI_CFG	RW	[0]: ROI enable	-	0x00
0x3569	[0]	EARLY_INT_EN	RW	[0]: Early interrupt enable	-	0x00
0x356A	[2:0]	FRAME_OUTPUT_EN	RW	[2]: Mask out enable for AE non-converged frame [1]: Mask out enable for MIPI output [0]: Mask out enable for parallel output	-	0x01
0x356B	[0]	EMBEDDED_LINE_EN	RW	[0]: Embedded data enable	-	0x01

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x356C	[7:0]	AE_CTRL	RW	AE control [7]: ALC_INT enable [6]: Frame Rate control enable [5]: RESERVED [4]: AE Update enable [3]: RESERVED [2]: RESERVED [1]: RESERVED [0]: AE enable	-	0x1F
0x356D	[4:0]	AE_CTRL1	RW	AE control 1 [4]: AEtarget_less_enable [3]: AEtarget_great_enable [2]: Exposure remap enable [1]: AENC_INT enable [0]: AE Statistics INT enable	-	0x00
0x356E	[1:0]	CNT_ORG_H	RW	AE ROI x start location [9:8]	-	0x00
0x356F	[7:0]		RW	AE ROI x start location [7:0]	-	0x01
0x3570	[0]	CNT_ORG_V	RW	AE ROI y start location [8]	-	0x00
0x3571	[7:0]		RW	AE ROI y start location [7:0]	-	0x02
0x3572	[1:0]	CNT_ST_H	RW	AE ROI x cnt [9:8]	-	0x00
0x3573	[7:0]		RW	AE ROI x cnt [7:0]	-	0x3F
0x3574	[0]	CNT_ST_V	RW	AE ROI y cnt [8]	-	0x00
0x3575	[7:0]		RW	AE ROI y cnt [7:0]	-	0x2F
0x3576	[3:0]	CTRL_PG_SKIPCNT	RW	AE skip count control	-	0x00
0x3577	[7:0]	MAX_INTG_H	RW	AE max INTG allowance H	-	0x01
0x3578	[7:0]	MAX_INTG_L	RW	AE max INTG allowance L	-	0x08
0x3579	[7:0]	MAX_AGAIN	RW	AE max AGAIN allowance	-	0x04
0x357A	[4:0]	MAX_DGAIN_H	RW	AE max DGAIN allowance H	-	0x03
0x357B	[5:0]	MAX_DGAIN_L	RW	AE max DGAIN allowance L	-	0x3F
0x357C	[7:0]	MIN_INTG	RW	AE min INTG allowance	-	0x00
0x357D	[7:0]	T_DAMPING	RW	AE T damping factor **(u1.7)**	-	0x20
0x357E	[4:0]	N_DAMPING	RW	AE N damping factor **(u0.5)**	-	0x00
0x357F	[7:0]	AE_TARGETZONE	RW	AE IIR Target Zone	-	0x23
0x3580	[7:0]	CONVERGE_IN_TH	RW	AE converge in threshold	-	0x08
0x3581	[7:0]	CONVERGE_OUT_TH	RW	AE converge out threshold	-	0x19
0x3582	[7:0]	RESERVED	RW	RESERVED	-	0x10
0x3583	[7:0]	RESERVED	RW	RESERVED	-	0x02
0x3584	[7:0]	FS_60HZ_H	RW	AE flicker step H **(60Hz)**	-	0x01
0x3585	[7:0]	FS_60HZ_L	RW	AE flicker step L **(60Hz)**	-	0x1C
0x3586	[7:0]	FS_50HZ_H	RW	AE flicker step H **(50Hz)**	-	0x01
0x3587	[7:0]	FS_50HZ_H	RW	AE flicker step L **(50Hz)**	-	0x54
0x3588	[7:0]	FR_STAGE1_H	RW	Frame rate stage 1 High byte	-	0x01
0x3589	[7:0]	FR_STAGE1_L	RW	Frame rate stage 1 Low byte	-	0x0A
0x358A	[7:0]	FR_STAGE2_H	RW	Frame rate stage 2 High byte	-	0x02
0x358B	[7:0]	FR_STAGE2_L	RW	Frame rate stage 2 Low byte	-	0x14
0x358C	[7:0]	FR_STAGE3_H	RW	Frame rate stage 3 High byte	-	0x03
0x358D	[7:0]	FR_STAGE3_L	RW	Frame rate stage 3 Low byte	-	0x1E
0x35A5	[7:0]	MD_CTRL	RW	[7:1]: Motion detect light coefficient [0]: Motion detect enable	-	0x01
0x35A6	[7:0]	MD_BLOCK_NUM_TH	RW	MD_block_number threshold	-	0x01
0x35A7	[7:0]	ROI_START_END_V	RW	[7:4]: ROI_END_V [3:0]: ROI_START_V	-	0xF0
0x35A8	[7:0]	ROI_START_END_H	RW	[7:4]: ROI_END_H [3:0]: ROI_START_H	-	0xF0
0x35A9	[7:0]	MD_TH_STR_H	RW	Threshold strength	-	0x10
0x35AA	[7:0]	MD_TH_STR_L	RW	Threshold strength	-	0x10
0x35AB	[7:0]	RESERVED	RW	RESERVED	-	0x10
0x35AC	[7:0]	MD_FLICK_TH_ADJ_N	RW	Motion detect flicker threshold adjustment N	-	0xAC
0x35AD	[7:0]	MD_FLICK_TH_ADJ_P	RW	Motion detect flicker threshold adjustment P	-	0xAD

Address	Byte	Register name	Type	Description	CMU	Default (Hex)
0x35AE	[7:0]	MD_TH_COEF_0	RW	Motion detect threshold coefficient 0	-	0x01
0x35AF	[7:0]	MD_TH_COEF_1	RW	Motion detect threshold coefficient 1	-	0x06
0x35B0	[7:0]	MD_TH_COEF_2	RW	Motion detect threshold coefficient 2	-	0x0C
0x35B1	[7:0]	MD_TH_COEF_3	RW	Motion detect threshold coefficient 3	-	0x12
0x35B2	[7:0]	MD_TH_COEF_4	RW	Motion detect threshold coefficient 4	-	0x1B
0x35B3	[7:0]	MD_TH_COEF_5	RW	Motion detect threshold coefficient 5	-	0x27

11. Electrical Specification

11.1 Absolute maximum ratings

Parameter		Symbol	Spec.			Unit
			Min.	Typ.	Max.	
Ambient storage temperature		T_{ST}	-30	-	85	°C
Operating temperature **(Junction temperature)**		T_{OP}	-20	-	85	°C
Stable image temperature(1) **(Junction temperature)**		T_{SI}	0	-	60	°C
Analog supply voltage		V_{DD-A_MAX}	-0.3	-	4.0	V
Digital supply voltage		V_{DD-D_MAX}	-0.3	-	2.0	V
IO supply voltage		V_{DD-IO_MAX}	-0.3	-	4.0	V
DC input voltage		DC_{IN}	-0.3	-	V_{DD-IO} + 0.3	V
ESD rating	Human Body Model	ESD	-	2000	-	V
	Machine Model		-	200	-	V

Note: (1) The sensor will produce stable images within the temperature range and the operating limits of the electrical specification. The image quality is not guaranteed when operating the sensor beyond the stable image temperature specification.

(2) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 11.1: Absolute maximum ratings

11.2 Operating voltages

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Analog supply voltage	V_{DD-A}	2.6	2.8	3.0	V
Digital supply voltage	V_{DD-D}	1.08	1.2	1.32	V
IO supply voltage	V_{DD-IO}	1.7	1.8 / 2.8	3.0	V
LDO supply voltage	$V_{DD-LDOIN}$	1.7	1.8 / 2.8	3.0	V

Table 11.2: Operating voltages

11.3 DC characteristics

The power consumptions are measured in color bar **(C_L = 5pF)**.

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Average Current Consumption – Parallel 8b, External LDO mode						
Continuous video output	$I_{DD-AVDD1}$	Video, VGA @ 60 FPS, PCLKO gated, V_{DD-A} = 2.8V,V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V	-	1394	-	µA
	$I_{DD-DVDD1}$		-	4718	-	µA
	$I_{DD-IOVDD1}$		-	1665	-	µA
S1 **(Gate single frame with software standby)**	$I_{DD-AVDD1}$	Auto wake up sleep, QQVGA@ 2 FPS, PCLKO gated, V_{DD-A} = 2.8V,V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V, XSLEEP high	-	29.5	-	µA
	$I_{DD-DVDD1}$		-	209.6	-	µA
	$I_{DD-IOVDD1}$		-	4.5	-	µA
S2 **(Gate single frame with hardware standby)**	$I_{DD-AVDD1}$	Auto wake up sleep, QQVGA@ 2 FPS, PCLKO gated, V_{DD-A} = 2.8V,V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V, XSLEEP control by host	-	15.5	-	µA
	$I_{DD-DVDD1}$		-	67.2	-	µA
	$I_{DD-IOVDD1}$		-	3.5	-	µA
Software Standby current	$I_{DD-SLEEP1}$	V_{DD-A} = 2.8V, V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V XSLEEP inactive	-	172	-	µA
Hardware Standby current	$I_{DD-SLEEP2}$	V_{DD-A} = 2.8V, V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V XSLEEP active	-	11	-	µA
Average Current Consumption – MIPI, External LDO mode						
Continuous video output	$I_{DD-AVDD1}$	Video, VGA @ 60 FPS, gated by line, w/o LSLE V_{DD-A} = 2.8V,V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V	-	1466	-	µA
	$I_{DD-DVDD1}$		-	8275	-	µA
	$I_{DD-IOVDD1}$		-	1	-	µA
S1 **(Gate single frame with software standby)**	$I_{DD-AVDD1}$	Auto wake up sleep, QQVGA@ 2 FPS, gated by line, w/o LSLE V_{DD-A} = 2.8V,V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V, XSLEEP high	-	31.9	-	µA
	$I_{DD-DVDD1}$		-	228.1	-	µA
	$I_{DD-IOVDD1}$		-	2	-	µA
S2 **(Gate single frame with hardware standby)**	$I_{DD-AVDD1}$	Auto wake up sleep, QQVGA@ 2 FPS, gated by line, w/o LSLE V_{DD-A} = 2.8V,V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V, XSLEEP control by host	-	16.6	-	µA
	$I_{DD-DVDD1}$		-	84	-	µA
	$I_{DD-IOVDD1}$		-	1	-	µA
Software Standby current	$I_{DD-SLEEP1}$	V_{DD-A} = 2.8V, V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V XSLEEP inactive	-	181	-	µA
Hardware Standby current	$I_{DD-SLEEP2}$	V_{DD-A} = 2.8V, V_{DD-D} = 1.2V, V_{DD-IO} = 1.8V XSLEEP active	-	17.1	-	µA
Average Current Consumption – Hardware shutdown						
Hardware shutdown **(Parallel/MIPI)**	I_{DD}	MCLK off	-	1	-	µA

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Digital Inputs (MCLK, TRIGGER, SCL)						
Input voltage low	V_{IL}	-	GND – 0.3	-	$0.3V_{DD-IO}$	V
Input voltage high	V_{IH}	-	$0.7V_{DD-IO}$	-	V_{DD-IO} + 0.3	V
Digital Output						
Output voltage low	V_{OL}	-	-	-	$0.2V_{DD-IO}$	V
Output voltage high	V_{OH}	-	$0.8V_{DD-IO}$	-	-	V
Tri-state leakage current	I_{OZ}	-	-	-	10	µA

Table 11.3: DC characteristics

11.4 Master Clock (MCLK) input

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input frequency	MCLK	-	6	-	24	MHz
Input clock duty cycle	$MCLK_{DUTY}$	-	45	-	55	%

Table 11.4: Master Clock (MCLK) timing

11.5 MIPI timing characteristics

(Conditions: T_A = 25ºC, C_L < 10pF, UI_{INST} = 2.84ns)

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
MIPI HS Transmitter Output					
UI instantaneous	UI_{INST}	-	2.84	-	ns
High speed transmitter 20%-80% Rise / Fall time	T_R	150	-	-	ps
	T_F	-	-	0.3	UI_{INST}
Data to clock skew	T_{SKEW}	-0.15	-	0.15	UI_{INST}
MIPI LP Transmitter Output					
Period of the LP exclusive-OR clock	$T_{LP-PER-TX}$	90	-	-	ns
Low power transmitter 15%-85% Rise / Fall time	T_{RLP}, T_{FLP}	-	-	25	ns
30%-85% Rise / Fall time	T_{REOT}	-	-	35	ns

Table 11.5: MIPI timing characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
MIPI HS Transmitter Output						
HS static common-mode voltage	V_{CMTX}	Range of ZID is 85~120Ω	150	200	250	mV
HS differential voltage	|VOD|	Range of ZID is 85~120Ω	140	200	270	mV
HS output high voltage	V_{OHHS}	Range of ZID is 85~120Ω	-	-	360	mV
Single ended output impedance	Z_{OS}	-	40	50	62.5	Ω
MIPI LP Transmitter Output						
Single-ended output voltage low	V_{OSL}	-	-50	-	50	mV
Single-ended output Voltage high	V_{OSH}	-	1.1	1.2	1.3	V

Table 11.6: MIPI interface characteristics

11.6 Serial bus characteristics

Parameter	Symbol	Condition	Spec.			Unit
			Min.	Typ.	Max.	
Input clock frequency	F_{SCL}	-	100	-	1000	kHz
Input clock period	t_{SCL}	-	1	-	10	µs
Input clock duty cycle	-	-	40	50	60	%
Rise time of SCL/SDA	t_{RT}	-	-	-	$0.12T_{SCL}$(1)	ns
Fall time of SCL/SDA	t_{FT}	-	-	-	$0.12T_{SCL}$(1)	ns
Start setup time	t_{HD_SU}	Write	T_{MCLK}(2)	-	-	ns
Start hold time	t_{HD_STA}	Write	$3T_{MCLK}$(2)	-	-	ns
Data hold time	t_{HD_DAT}	Write	5	-	-	ns
Data setup time	t_{SU_DAT}	Write	$3T_{MCLK}$(2)	-	-	ns
Stop setup time	t_{SU_STP}	Write	$3T_{MCLK}$(2)	-	-	ns
Stop hold time	t_{HD_STP}	Write	T_{MCLK}(2)	-	-	ns
Data hold time	t_{HD_DATR}	Read	$3T_{MCLK}$(2)	-	-	ns
Data setup time	t_{SU_DATR}	Read	T_{SCL}(1)/2-t_{HD_DATR}	-	-	ns
SDA maximum load capacitance	C_{SDA_LOAD}	-	-	-	4.2	pF
SDA pull-up resistor	R_{SDA}	-	500	-	-	Ω

Note: (1) T_{SCL} = Cycle time of SCL.
(2) T_{MCLK} = Cycle time of MCLK.

Table 11.7: Serial bus interface timing

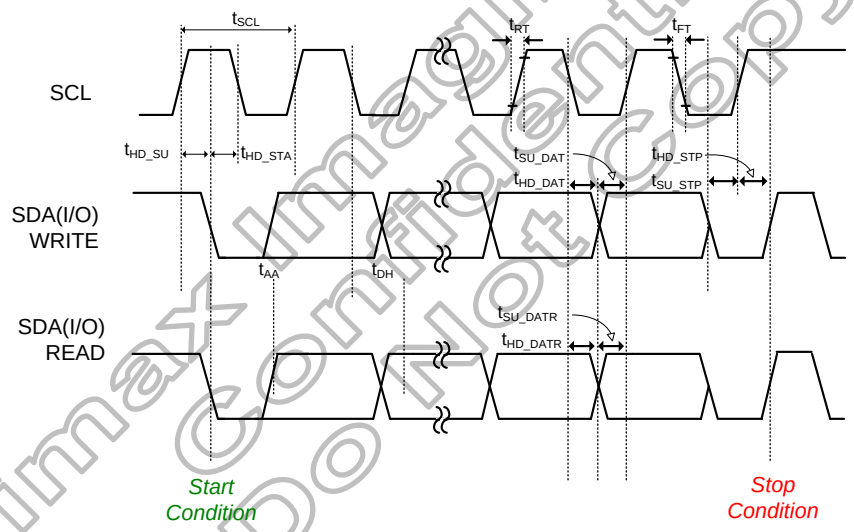


Figure 11.1: 2-Wire serial interface timing diagram

11.7 Parallel interface timing characteristics

Conditions: T_A = 25ºC, C_L = 5pF, F_{PLCKO} = 24MHz

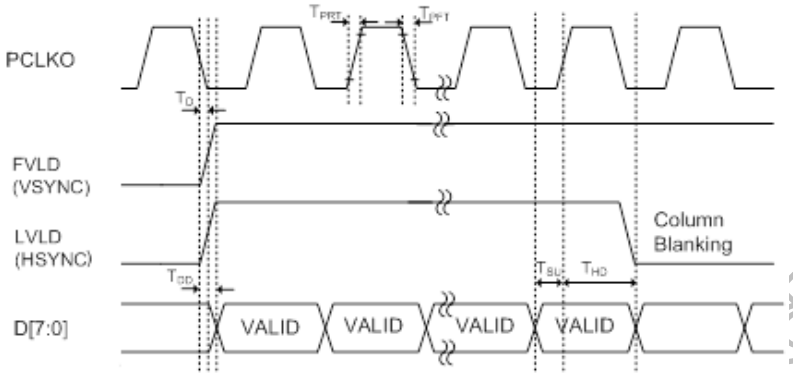


Figure 11.2: 8-bit parallel video interface timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
PCLKO period	T_{PLCKO}	-	41.67	-	ns
PCLKO rise time	T_{PRT}	-	5.55	-	ns
PCLKO fall time	T_{PFT}	-	3.63	-	ns
PCLKO falling edge to HSYNC rising edge delay	T_D	-	7	-	ns
PCLKO falling edge to DATA transition delay	T_{DD}	-	5.4	-	ns
Data bus setup time	T_{SU}	-	16.2	-	ns
Data bus hold time	T_{HD}	-	23.8	-	ns

Table 11.8: 8-bit parallel video interface timing

Conditions: T_A = 25ºC, C_L = 5pF, F_{PLCKO} = 48MHz

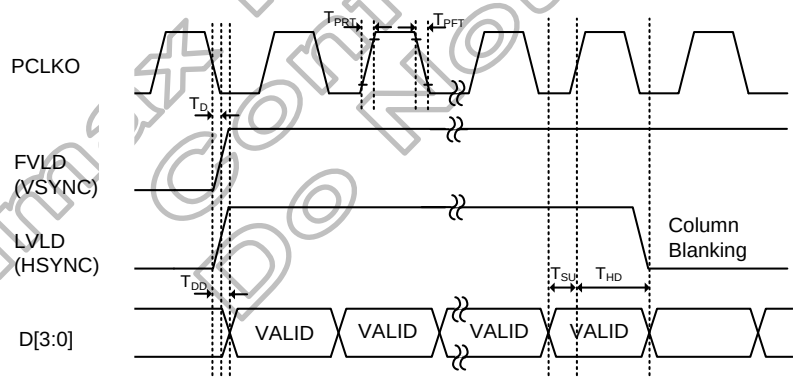


Figure 11.3: 4-bit parallel video interface timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
PCLKO period	T_{PLCKO}	-	20.83	-	ns
PCLKO rise time	T_{PRT}	-	3.51	-	ns
PCLKO fall time	T_{PFT}	-	3.56	-	ns
PCLKO falling edge to HSYNC rising edge delay	T_D	-	4.08	-	ns
PCLKO falling edge to DATA transition delay	T_{DD}	-	2.72	-	ns
Data bus setup time	T_{SU}	-	7.44	-	ns
Data bus hold time	T_{HD}	-	9.76	-	ns

Table 11.9: 4-bit parallel video interface timing

11.8 Serial interface timing characteristics

Conditions: T_A = 25ºC, C_L = 5pF, F_{PLCKO} = 48MHz

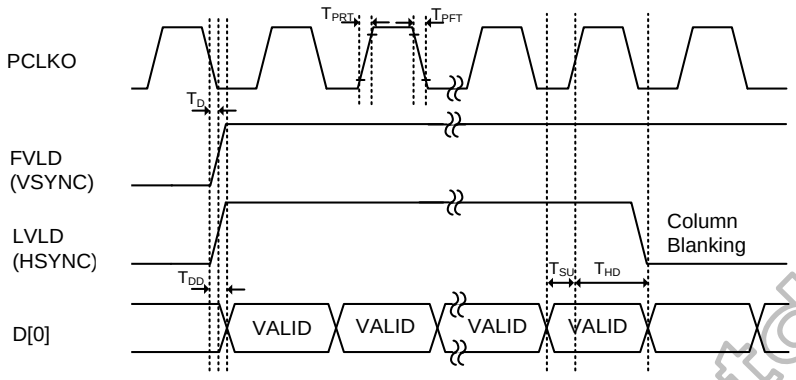


Figure 11.4: Serial video interface timing diagram

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
PCLKO period	T_{PLCKO}	-	20.83	-	ns
PCLKO rise time	T_{PRT}	-	8.78	-	ns
PCLKO fall time	T_{PFT}	-	4.84	-	ns
PCLKO falling edge to HSYNC rising edge delay	T_D	-	1.2	-	ns
PCLKO falling edge to DATA transition delay	T_{DD}	-	2.6	-	ns
Data bus setup time	T_{SU}	-	8.8	-	ns
Data bus hold time	T_{HD}	-	9.6	-	ns

Table 11.10: Serial video interface timing

12. Sensor Chief Ray Angle (CRA)

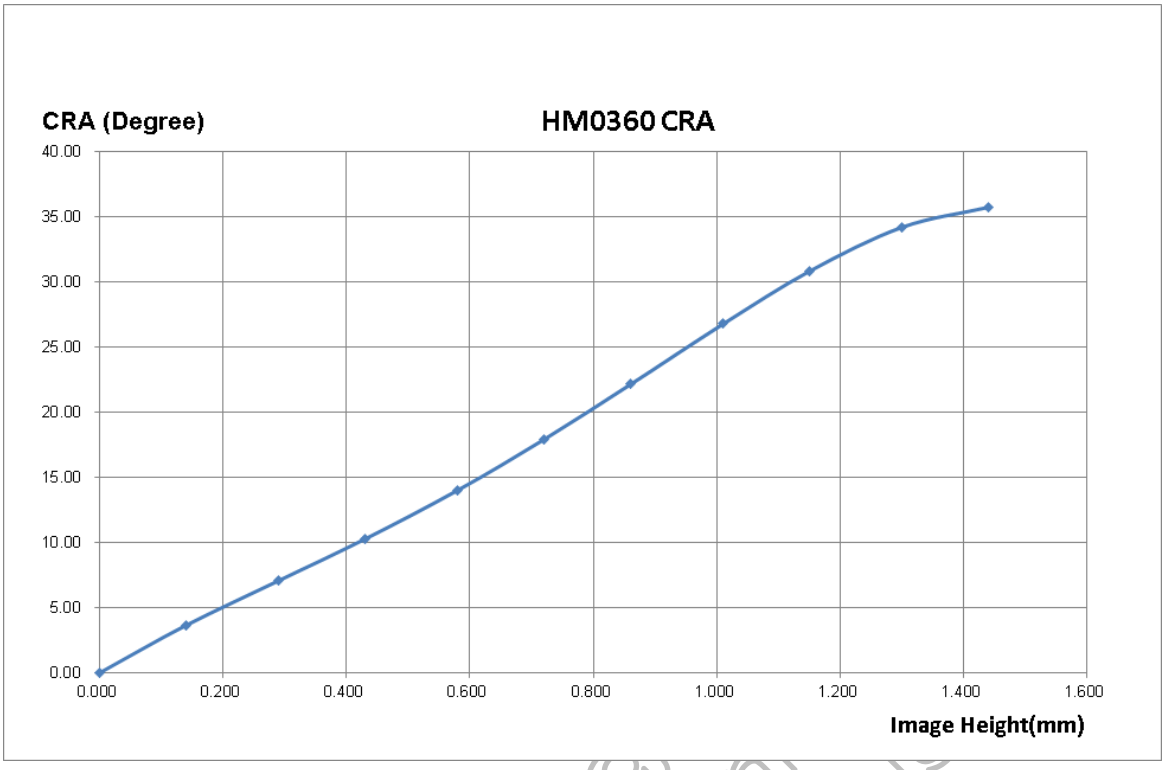


Figure 12.1: Lens CRA profile

Field (%)	Image Height (mm)	CRA (degree)
0.00	0.000	0.00
0.10	0.140	3.65
0.20	0.290	7.08
0.30	0.430	10.28
0.40	0.580	14.02
0.50	0.720	17.92
0.60	0.860	22.14
0.70	1.010	26.78
0.80	1.150	30.83
0.90	1.300	34.21
1.00	1.440	35.74

Table 12.1: CRA profile

13. Quantum Efficiency (QE)

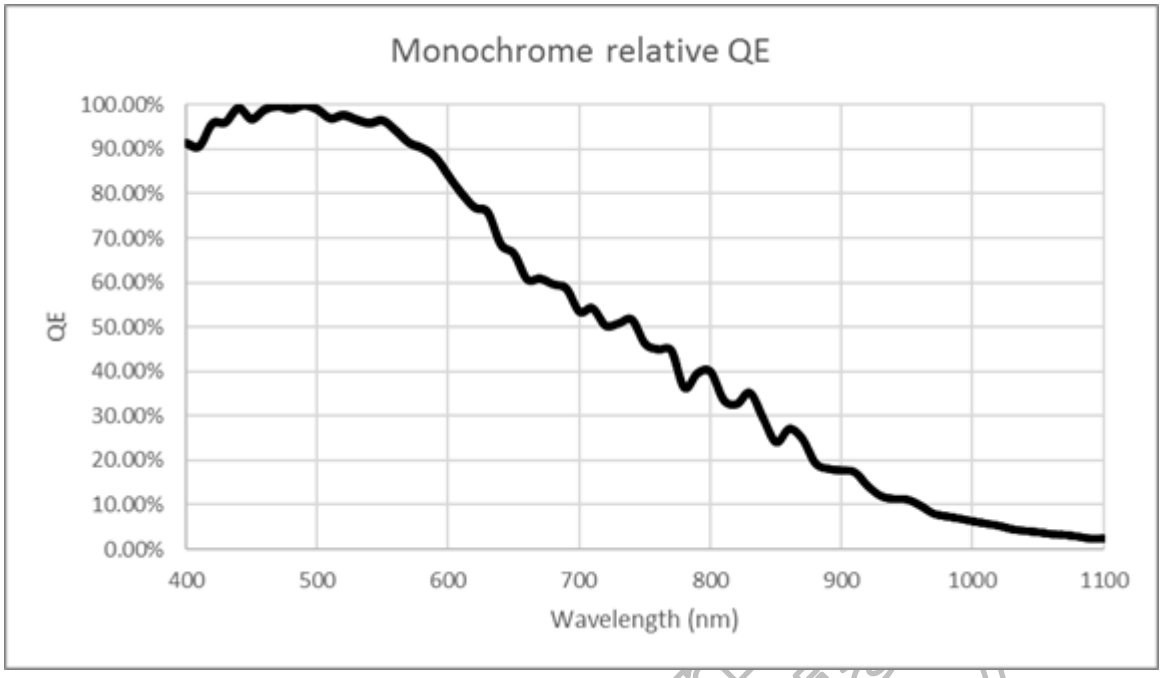


Figure 13.1: QE (Monochrome)

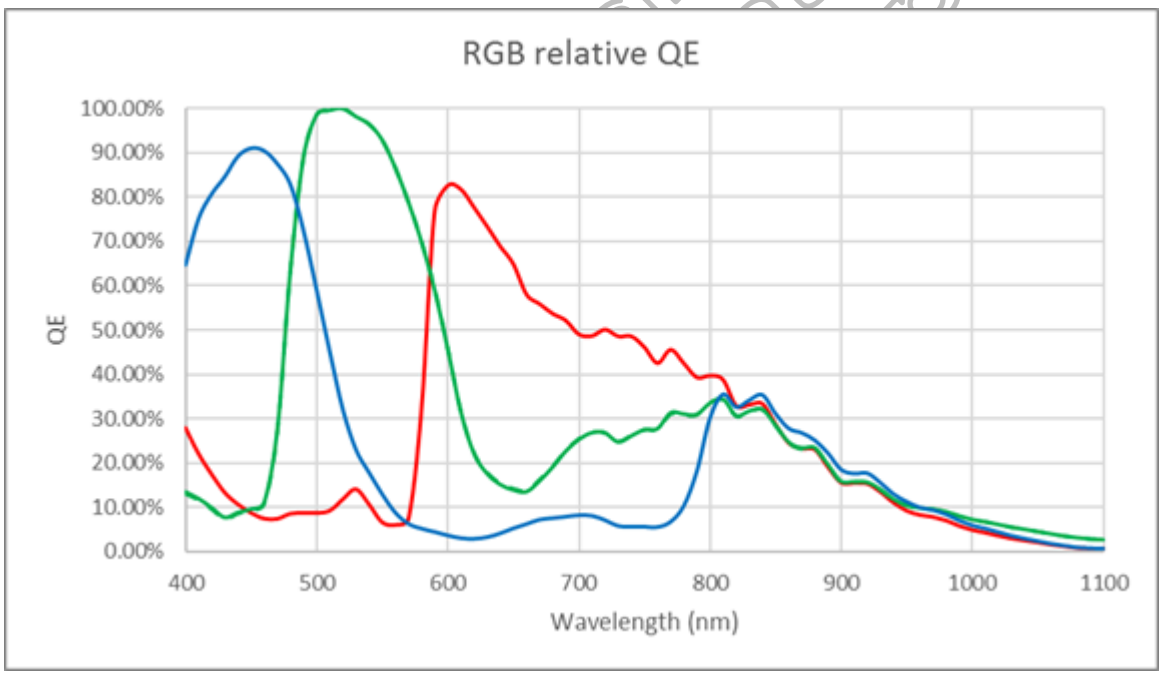


Figure 13.2: QE (Bayer)