Rochester Electronics®

Datasheet

# 54L42, 54LS42, SN5442, 7442

*4-Line to 10-Line Decoders (1-of-10)*

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

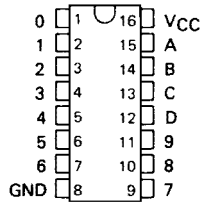
FOR REFERENCE ONLY

'42A, 'L42, 'LS42 . . . BCD-TO-DECIMAL
'43A, 'L43 . . . EXCESS-3-TO-DECIMAL
'44A 'L44 . . . GRAY-TO-DECIMAL

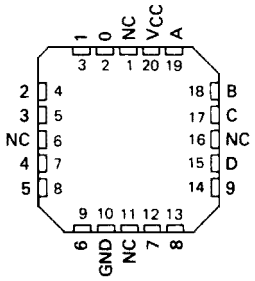
- All Outputs Are High for Invalid Input Conditions
- Also for Application as
  4-Line-to-16-Line Decoders
  3-Line-to-8-Line Decoders
- Diode-Clamped Inputs

| TYPES | TYPICAL POWER DISSIPATION | TYPICAL PROPAGATION DELAYS |
|---|---|---|
| '42A, '43A, '44A | 140 mW | 17 ns |
| 'L42, 'L43, 'L44 | 70 mW | 49 ns |
| 'LS42 | 35 mW | 17 ns |

SN5442A THRU SN5444A, SN54LS42 . . . J OR W PACKAGE
SN54L42 THRU SN54L44 . . . J PACKAGE
SN7442A THRU SN7444A . . . J OR N PACKAGE
SN74LS42 . . . D, J OR N PACKAGE
(TOP VIEW)




SN54LS42 . . . FK PACKAGE
SN74LS42 . . . FN PACKAGE
(TOP VIEW)




NC – No internal connection

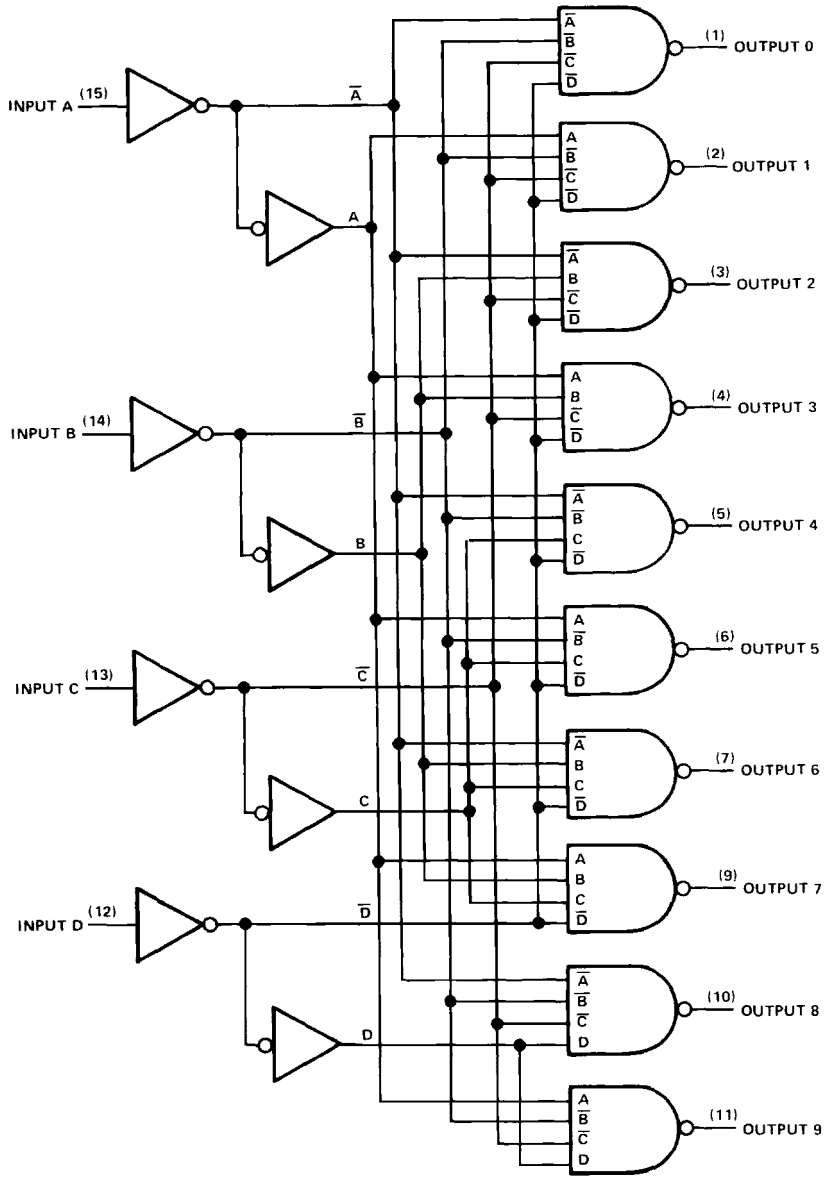
## description

These monolithic decimal decoders consist of eight inverters and ten four- input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The '42A, 'L42, and 'LS42 BCD-to-decimal decoders, the '43A and 'L43 excess-3-to-decimal decoders, and the '44A and 'L44 gray-to-decimal decoders feature inputs and outputs that are compatible for use with most TTL and other saturated low-level logic circuits. DC noise margins are typically one volt.

Series 54, 54L, and 54LS circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74, and 74LS circuits are characterized for operation from 0°C to 70°C.

## logic diagrams




Pin numbers shown on logic notation are for D, J or N packages.





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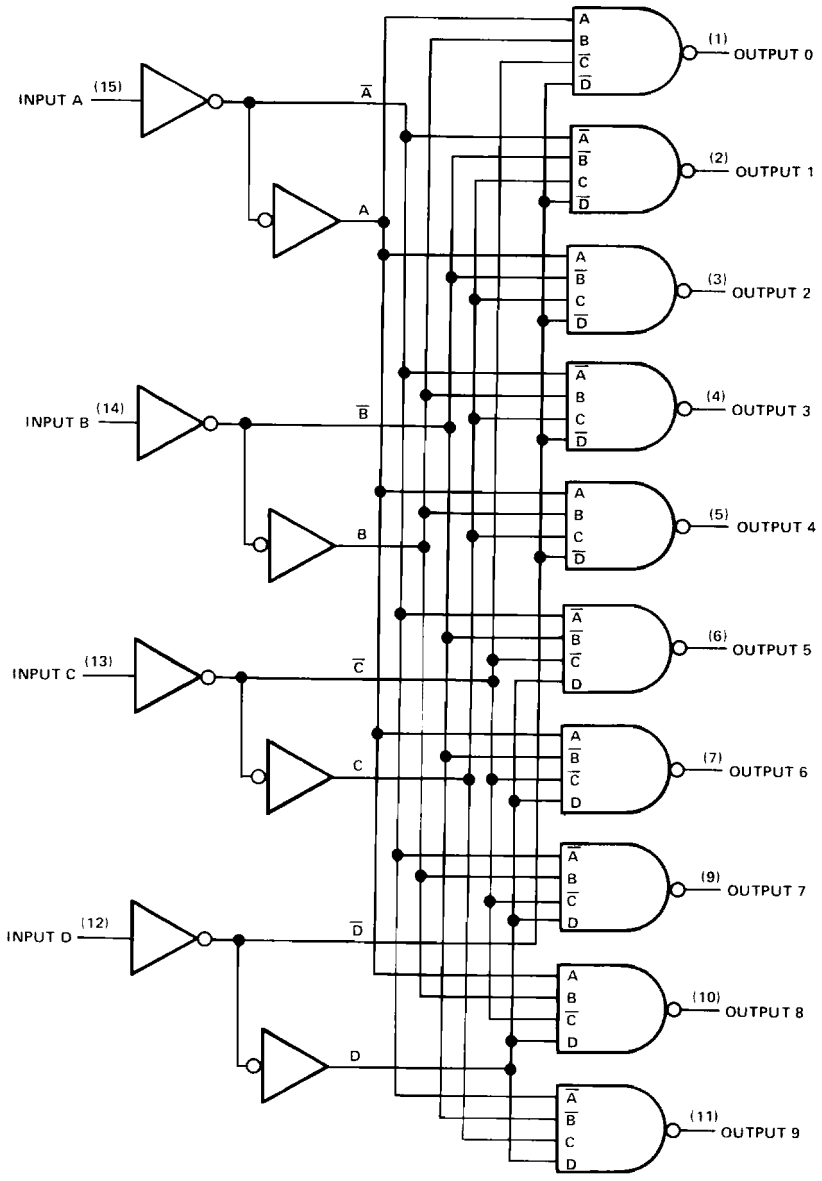
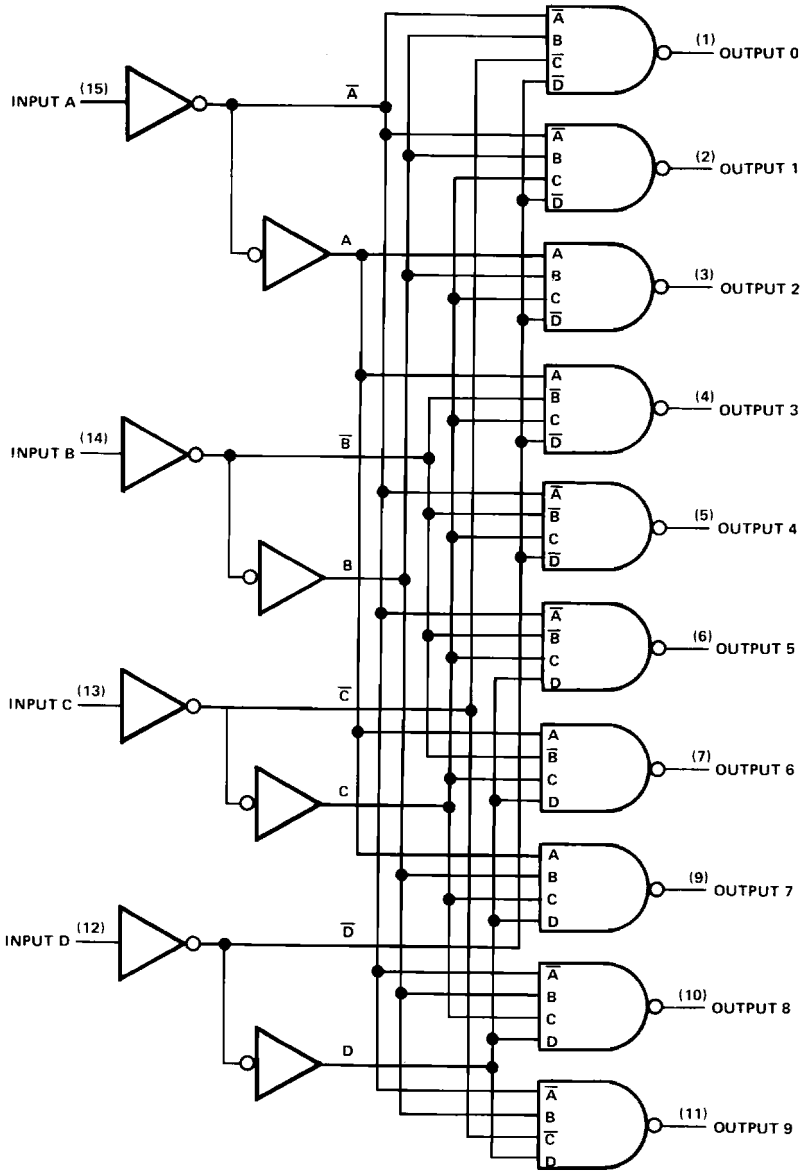
logic diagrams (continued)




Pin numbers shown on logic notation are for D, J or N packages.

logic diagrams (continued)




Pin numbers shown on logic notation are for D, J or N packages.





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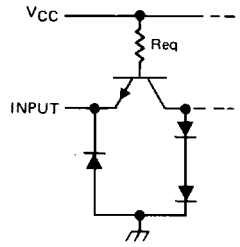
## schematics of inputs and outputs

'42A THRU '44A
'L42 THRU 'L44

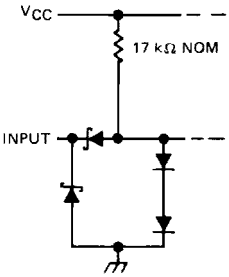
EQUIVALENT OF EACH INPUT




'42A THRU '44A: $R_{eq}$ = 4 kΩ NOM
'L42 THRU 'L44: $R_{eq}$ = 8 kΩ NOM

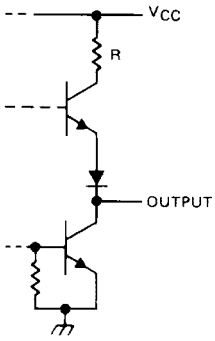
'LS42

EQUIVALENT OF EACH INPUT




'42A THRU '44A
'L42 THRU 'L44

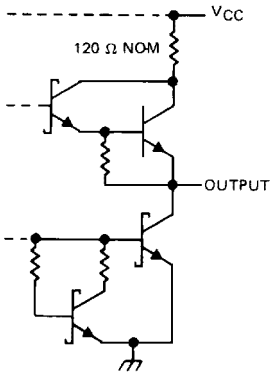
TYPICAL OF ALL OUTPUTS




'42A THRU '44A: R = 130 Ω NOM
'L42 THRU 'L44: R = 260 Ω NOM

'LS42

TYPICAL OF ALL OUTPUTS



**FUNCTION TABLE**

| NO. | '42A, 'L42, 'LS42 BCD INPUT | | | | '43A, 'L43 EXCESS-3-INPUT | | | | '44A, 'L44 GRAY INPUT | | | | ALL TYPES DECIMAL OUTPUT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D | C | B | A | D | C | B | A | D | C | B | A | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| 0 | L | L | L | L | L | L | H | H | L | L | H | L | L | H | H | H | H | H | H | H | H | H |
| 1 | L | L | L | H | L | H | L | L | L | H | H | L | H | L | H | H | H | H | H | H | H | H |
| 2 | L | L | H | L | L | H | L | H | L | H | H | H | H | H | L | H | H | H | H | H | H | H |
| 3 | L | L | H | H | L | H | H | L | L | H | L | H | H | H | H | L | H | H | H | H | H | H |
| 4 | L | H | L | L | L | H | H | H | L | H | L | L | H | H | H | H | L | H | H | H | H | H |
| 5 | L | H | L | H | H | L | L | L | H | H | L | L | H | H | H | H | H | L | H | H | H | H |
| 6 | L | H | H | L | H | L | L | H | H | H | L | H | H | H | H | H | H | H | L | H | H | H |
| 7 | L | H | H | H | H | L | H | L | H | H | H | H | H | H | H | H | H | H | H | L | H | H |
| 8 | H | L | L | L | H | L | H | H | H | H | H | L | H | H | H | H | H | H | H | H | L | H |
| 9 | H | L | L | H | H | H | L | L | H | L | H | L | H | H | H | H | H | H | H | H | H | L |
| INVALID | H | L | H | L | H | H | L | H | H | L | H | H | H | H | H | H | H | H | H | H | H | H |
| | H | L | H | H | H | H | H | L | H | L | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | L | H | H | H | H | H | L | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | L | H | L | L | L | L | L | L | L | L | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | L | L | L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H |
| | H | H | H | H | L | L | H | L | L | L | H | H | H | H | H | H | H | H | H | H | H | H |

H = high level, L = low level

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '42A, '43A, '44A . . . . . 5.5 V
'L42, 'L43, 'L44 . . . . . 5.5 V
'LS42 . . . . . 7 V
Operating free-air temperature: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.





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## recommended operating conditions

| | SN5442A SN5443A SN5444A | | | SN7442A SN7443A SN7444A | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −800 | | | −800 | μA |
| Low-level output current, $I_{OL}$ | | | 16 | | | 16 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | SN5442A SN5443A SN5444A | | | SN7442A SN7443A SN7444A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −12 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OH}$ = −800 μA | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = 0.8 V, $I_{OL}$ = 16 mA | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 1 | | | 1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 40 | | | 40 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | −1.6 | | | −1.6 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | −20 | | −55 | −18 | | −55 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | 28 | 41 | | 28 | 56 | mA |

†For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with all outputs open and all inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic | $C_L$ = 15 pF, $R_L$ = 400 Ω, See Note 3 | | 14 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic | | | 17 | 30 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic | | | 10 | 25 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic | | | 17 | 30 | ns |

NOTE 3: See General Information Section for load circuits and voltage waveforms.

## recommended operating conditions

| | | SN54L42 SN54L43 SN54L44 | | | UNIT |
|---|---|---|---|---|---|
| | | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | 8 | mA |
| $T_A$ | Operating free-air temperature | −55 | | 125 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS† | | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | | | −1.5 | V |
| $V_{OH}$ | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | $I_{OH}$ = −400 μA | 2.4 | 3.4 | | V |
| $V_{OL}$ | $V_{CC}$ = MIN, | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | $I_{OL}$ = 8 mA | | 0.2 | 0.4 | V |
| $I_I$ | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | | 1 | mA |
| $I_{IH}$ | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | | 20 | μA |
| $I_{IL}$ | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | | −0.8 | mA |
| $I_{OS}$§ | $V_{CC}$ = MAX | | | | −9 | | −28 | mA |
| $I_{CC}$ | $V_{CC}$ = MAX, | See Note 2 | | | | 14 | 22 | mA |

† For conditions shown as MIN or MAX, use the appropriate values specified under recommended operating conditions.
All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: $I_{CC}$ is measured with all outputs open and inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic | $C_L$ = 15 pF, $R_L$ = 800 Ω, See Note 3 | 10 | 44 | 60 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic | | | 46 | 70 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic | | 10 | 34 | 50 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic | | | 52 | 70 | ns |

NOTE 3: See General Information Section for load circuits and voltage waveforms.





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## recommended operating conditions

| | SN54LS42 | | | SN74LS42 | | | UNIT |
|---|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX | |
| Supply voltage, $V_{CC}$ | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| High-level output current, $I_{OH}$ | | | −400 | | | −400 | μA |
| Low-level output current, $I_{OL}$ | | | 4 | | | 8 | mA |
| Operating free-air temperature, $T_A$ | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS42 | | | SN74LS42 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IH}$ | High-level input voltage | | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | | 0.7 | | | 0.8 | V |
| $V_{IK}$ | Input clamp voltage | $V_{CC}$ = MIN, $I_I$ = −18 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | High-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max, $I_{OH}$ = −400 μA | | 2.5 | 3.5 | | 2.7 | 3.5 | | V |
| $V_{OL}$ | Low-level output voltage | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = $V_{IL}$ max | $I_{OL}$ = 4 mA | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8 mA | | | | | 0.35 | 0.5 | |
| $I_I$ | Input current at maximum input voltage | $V_{CC}$ = MAX, $V_I$ = 7 V | | | | 0.1 | | | 0.1 | mA |
| $I_{IH}$ | High-level input current | $V_{CC}$ = MAX, $V_I$ = 2.7 V | | | | 20 | | | 20 | μA |
| $I_{IL}$ | Low-level input current | $V_{CC}$ = MAX, $V_I$ = 0.4 V | | | | −0.4 | | | −0.4 | mA |
| $I_{OS}$ | Short-circuit output current§ | $V_{CC}$ = MAX | | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | Supply current | $V_{CC}$ = MAX, See Note 2 | | | 7 | 13 | | 7 | 13 | mA |

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 2. $I_{CC}$ is measured with all outputs open and inputs grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from A, B, C, or D through 2 levels of logic | $C_L$ = 15 pF, $R_L$ = 2 kΩ, See Note 3 | | 15 | 25 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from A, B, C, or D through 3 levels of logic | | | 20 | 30 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from A, B, C, and D through 2 levels of logic | | | 15 | 25 | ns |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from A, B, C, and D through 3 levels of logic | | | 20 | 30 | ns |

Note 3: See General Information Section for load circuits and voltage waveforms.