

# MediaClock™ Mini Disc Clock Generator

## Features

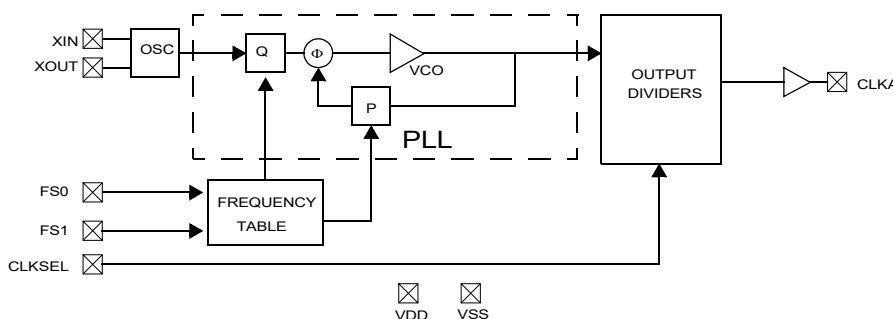
- Integrated phase-locked loop (PLL)
- Low jitter, high accuracy outputs
- 3.3 V operation
- 8-pin SOIC package

## Benefits

- High performance PLL tailored for mini disc applications.
- Meets critical timing requirements in complex system designs.
- Enables application compatibility.
- Industry standard package saves on board space.

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24115-2	1	1 MHz–30 MHz	90.3168 MHz and 180.6336 MHz (selectable)

## Logic Block Diagram



**Table 1. CLKSEL Function, CY24115-2**

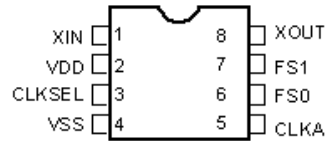
CLKSEL	CLKA	Unit	PPM Error
0	90.3168	MHz	0
1	180.6336	MHz	0

**Table 2. Input Frequency Function, CY24115-2**

FS1	FS0	Xtal Input	Unit
0	0	2.8224	MHz
0	1	5.6448	MHz
1	0	11.2896	MHz
1	1	22.5792	MHz

## Pin Configurations

**Figure 1. 8-pin SOIC pinout**



## Pin Definitions

Pin Name	Pin Number	Pin Description
X <sub>IN</sub>	1	Reference input (crystal or external input)
V <sub>DD</sub>	2	3.3V voltage supply
CLKSEL	3	CLKA select line For 24115-2, see <a href="#">Table 1 on page 1</a> for output values
V <sub>SS</sub>	4	Ground
CLKA	5	24115-2: 90.3168 MHz and 180.6336 MHz (frequency selectable). See <a href="#">Table 1 on page 1</a> .
FS0	6	Input frequency FS0. See <a href="#">Table 2 on page 1</a> .
FS1	7	Input frequency FS1. See <a href="#">Table 2 on page 1</a> .
X <sub>OUT</sub> <sup>[1]</sup>	8	Reference output

**Note**

1. Float X<sub>OUT</sub> if X<sub>IN</sub> is externally driven.

## Absolute Maximum Conditions

Parameter	Description	Min	Max	Unit
$V_{DD}$	Supply Voltage	-0.5	7.0	V
$T_S$	Storage Temperature <sup>[2]</sup>	-65	125	°C
$T_J$	Junction Temperature	–	125	°C
	Digital Inputs	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Digital Outputs Referred to $V_{DD}$	$V_{SS} - 0.3$	$V_{DD} + 0.3$	V
	Electrostatic Discharge	2	–	kV

## Recommended Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
$V_{DD}$	Operating Voltage	3.14	3.3	3.47	V
$T_A$	Ambient Temperature	0	–	70	°C
$C_{LOAD}$	Max. Load Capacitance	–	–	15	pF
$f_{REF}$	Reference Frequency	2.8224	–	22.5792	MHz
$t_1$	Driven Reference Edge Rate	0.8	–	–	V/ns
$DC_{IN}$	Driven Reference Duty Cycle	40	–	60	%
$C_{IN}$	$X_{IN}$ , $X_{OUT}$ capacitance	–	12	–	pF
$t_{PU}$	Power up time for all $V_{DD}$ 's to reach minimum specified voltage (power ramps must be monotonic)	0.05	–	500	ms

## DC Electrical Characteristics

Parameter	Name	Description	Min	Typ	Max	Unit
$I_{OH}$	Output High Current	$V_{OH} = V_{DD} - 0.5$ V, $V_{DD} = 3.3$ V (source)	12	24	–	mA
$I_{OL}$	Output Low Current	$V_{OL} = 0.5$ , $V_{DD} = 3.3$ V (sink)	12	24	–	mA
$C_{IN}$	Input Capacitance	CLKSEL, FS0, FS1, excludes $X_{IN}$ , $X_{OUT}$	–	–	7	pF
$V_{IL}$	Input Low Voltage		–	–	30	% of $V_{DD}$
$V_{IH}$	Input High Voltage		70	–	–	% of $V_{DD}$
$I_{IZ}$	Input Leakage Current		–	5	–	μA
$I_{DD}$	Supply Current	Sum of core and output current	–	–	35	mA

### Note

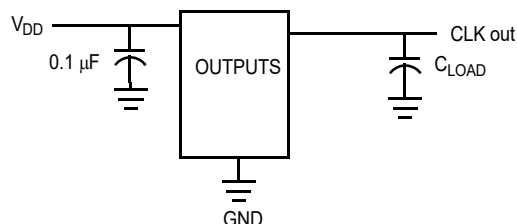
2. Rated for 10 years.

## AC Electrical Characteristics

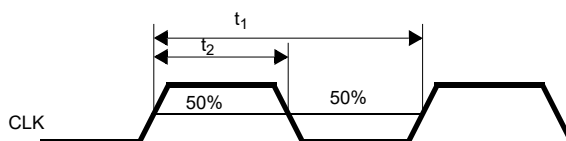
( $V_{DD} = 3.3\text{ V}$ )

Parameter <sup>[3]</sup>	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty cycle is defined in Figure 3, 50% of $V_{DD}$	45	50	55	%
$t_3$	Rising Edge Slew Rate	Output clock rise time, 20%–80% of $V_{DD}$	0.8	1.4	–	V/ns
$t_4$	Falling Edge Slew Rate	Output clock fall time, 80%–20% of $V_{DD}$	0.8	1.4	–	V/ns
$t_9$	Clock Jitter	Peak to peak period jitter	–	–	350	ps
$t_{10}$	PLL Lock Time		–	–	3	ms

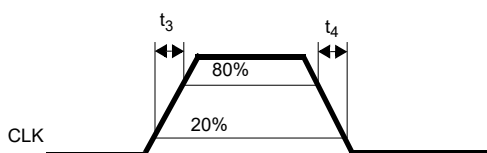
**Figure 2. Test Circuit**



**Figure 3. Duty Cycle Definition;  $DC = t_2/t_1$**



**Figure 4. Rise and Fall Time Definitions**



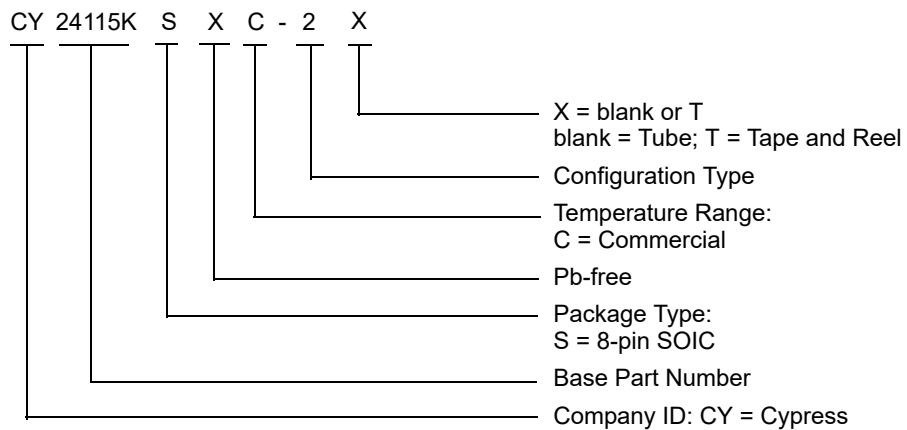
**Note**

3. Not 100% tested.

## Ordering Information

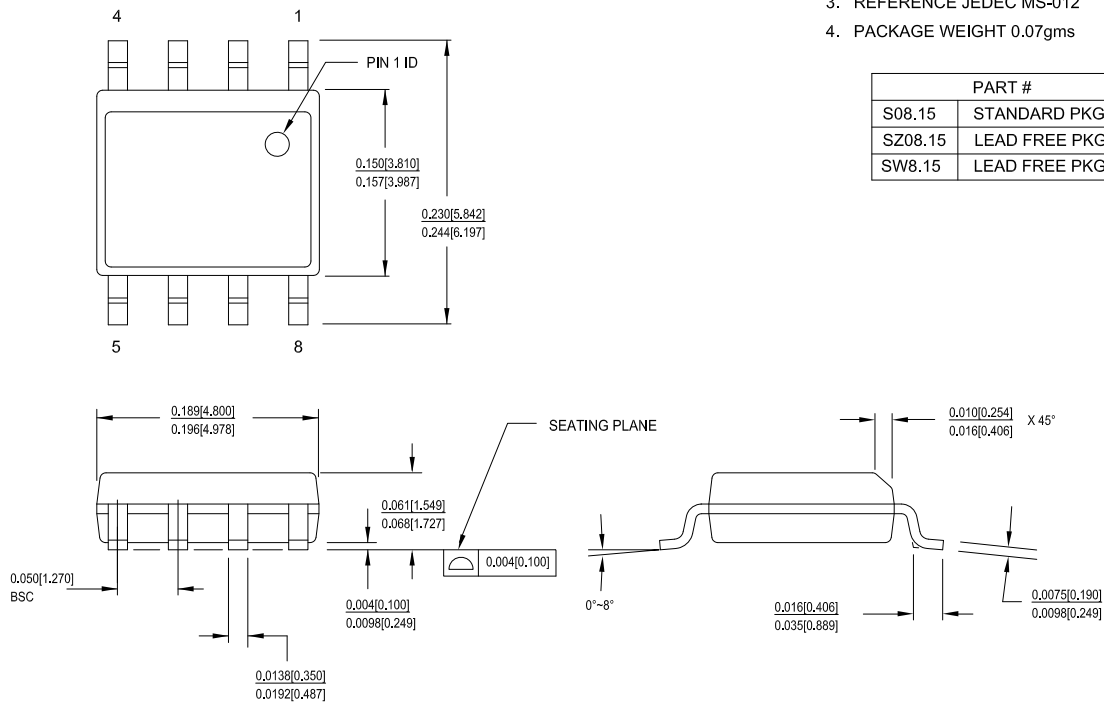
Ordering Code	Package Type	Operating Range	Operating Voltage
<b>Pb-free</b>			
CY24115KSXC-2	8-pin SOIC	Commercial	3.3 V
CY24115KSXC-2T	8-pin SOIC - Tape and Reel	Commercial	3.3 V

## Ordering Code Definitions



## Package Diagram

**Figure 5. 8-pin SOIC (150 Mils) S0815/SZ815/SW815 Package Outline, 51-85066**



1. DIMENSIONS IN INCHES[MM] MIN. MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG

51-85066 \*I

## Acronyms

Acronym	Description
I/O	Input/Output
PLL	Phase-Locked Loop
SOIC	Small-Outline Integrated Circuit

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
kV	kilovolt
MHz	megahertz
μA	microampere
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ps	picosecond
V	volt
W	watt

## Document History Page

**Document Title:** CY24115, MediaClock™ Mini Disc Clock Generator  
**Document Number:** 38-07275

Revision	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110767	CKN	02/06/2002	New data sheet.
*A	113515	CKN	04/30/2002	Changed status from Preliminary to Final. Updated <a href="#">DC Electrical Characteristics</a> : Updated details in "Description" column corresponding to $I_{OH}$ and $I_{OL}$ parameters (Added (source) at the end in description of $I_{OH}$ parameter and (sink) at the end in description of $I_{OL}$ parameter).
*B	121884	RBI	12/14/2002	Updated <a href="#">Recommended Operating Conditions</a> : Added $t_{PU}$ parameter and its details.
*C	252154	RGL	08/26/2004	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagram</a> : spec 51-85066 – Changed revision from *A to *C.
*D	2441946	AESA	05/15/2008	Updated <a href="#">Ordering Information</a> : Added Note "Not recommended for new designs." and referred the same note in existing MPNs. Updated part numbers (Added MPNs CY24115KSXC-2, and CY24115KSXC-2T). Updated to new template.
*E	2781381	CXQ	03/19/2010	Updated <a href="#">Ordering Information</a> : Updated part numbers (Removed MPNs CY24115SC-2, CY24115SC-2T, CY24115SC-1, CY24115SC-1T, CY24115SXC-1, CY24115SXC-1T). Updated <a href="#">Package Diagram</a> : spec 51-85066 – Changed revision from *C to *D. Updated to new template.
*F	3068367	CXQ	10/21/2010	Removed CY24115-1 parts related information in all instances across the datasheet. Updated <a href="#">Ordering Information</a> : Updated part numbers (Removed MPNs CY24115SXC-2 and CY24115SXC-2T). Added <a href="#">Ordering Code Definitions</a> .
*G	4018058	CINM	06/03/2013	Updated <a href="#">Package Diagram</a> : spec 51-85066 – Changed revision from *D to *F. Added <a href="#">Acronyms</a> and <a href="#">Units of Measure</a> . Updated to new template. Completing Sunset Review.
*H	5298871	XHT	06/07/2016	Updated <a href="#">Package Diagram</a> : spec 51-85066 – Changed revision from *F to *H. Updated to new template. Completing Sunset Review.
*I	6013606	XHT	01/04/2018	Updated <a href="#">Package Diagram</a> : spec 51-85066 – Changed revision from *H to *I. Updated to new template.



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