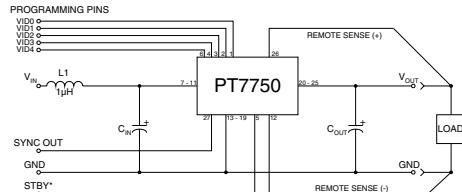


Standard Application

 C_{in} = Required 560uF electrolytic (See input filter note) C_{out} = Required 2000uF electrolytic

L1 = Optional 1uH input choke

The PT7750 series is a +24V input, 15 Amp output, high-performance Integrated Switching Regulator (ISR) housed in a 27-pin SIP package. The 15A capability allows easy integration of the latest high-speed, low-voltage μ Ps and bus drivers into +24V distributed power systems.

The PT7750 series has been designed to work in parallel with one or

more of the PT7747 current boosters for increased I_{out} in increments of 15A.

The output voltage of the PT7750 series can be easily programmed over a wide range with a 5-bit input. A differential remote sense is provided which automatically compensates for any voltage drop from the ISR to the load.

2000 μ F of output capacitance is required for proper operation.

Pin-Out Information

Pin	Function
1	VID0
14	GND
2	VID1
15	GND
3	VID2
16	GND
4	VID3
17	GND
5	STBY* - Stand-by
18	GND
6	VID4
19	GND
7	V _{in}
20	V _{out}
8	V _{in}
21	V _{out}
9	V _{in}
22	V _{out}
10	V _{in}
23	V _{out}
11	V _{in}
24	V _{out}
12	Remote Sense Gnd
25	V _{out}
13	GND
26	Remote Sense V _{out}
27	Sync Out

Features

- +24V bus input
- High Efficiency
- Differential Remote Sense
- 27-pin SIP Package
- Parallelable with PT7747 15A current boosters

Specifications

Characteristics ($T_s = 25^\circ\text{C}$ unless noted)	Symbols	Conditions	PT7750 SERIES			
			Min	Typ	Max	Units
Output Current	I_o	$T_a = +60^\circ\text{C}$, 200 LFM $T_a = +25^\circ\text{C}$, natural convection	0.1 (1) 0.1 (1)	— —	15 (2) 15 (2)	A
Input Voltage Range	V_{in}	$0.1A \leq I_o \leq I_o \text{ max}$	20.0	—	28.0	V
Undervoltage Lockout Threshold	V_{uvl}	$0.1A \leq I_o \leq I_o \text{ max}$	—	18.7	—	V
Output Voltage Tolerance	ΔV_o	$V_{in} = +24V, I_o = 15A$ PT7751 $0^\circ\text{C} \leq T_a \leq +55^\circ\text{C}$ PT7756	— —	— —	± 80 ± 160	mV
Line Regulation	Reg_{line}	$20V \leq V_{in} \leq 28V, I_o = I_o \text{ max}$ (w/remote sense)	—	± 15	—	mV
Load Regulation	Reg_{load}	$V_{in} = +24V, 0.1 \leq I_o \leq I_o \text{ max}$ (w/remote sense)	—	± 10	—	mV
V_o Ripple/Noise	V_n	$V_{in} = +24V, I_o = I_o \text{ max}$	—	75	—	mV
Transient Response with $C_{out} = 2000\mu\text{F}$	$\frac{t_{tr}}{V_{os}}$	I_o step between 7.5A and 15A V_o over/undershoot	— —	100 200	— —	μSec mV
Efficiency	η	$V_{in} = +24V, I_o = 10A$	$V_o = 5.0V$ $V_o = 3.3V$ $V_o = 2.5V$	88 84 80	— — —	%
Switching Frequency	f_o	$20V \leq V_{in} \leq 28V$ $0.1A \leq I_o \leq 15A$	300	350	400	kHz
Absolute Maximum Operating Temperature Range	T_a	—	0	—	$+85$ (3)	$^\circ\text{C}$
Storage Temperature	T_s	—	-40	—	+125	$^\circ\text{C}$
Weight	—	Vertical/Horizontal	—	53/66	—	grams

Notes (1) ISR-will operate down to no load with reduced specifications. Please note that this product is not short-circuit protected.

(2) The PT7750 series can be easily paralleled with one or more of the PT7747 Current Boosters to provide increased output current in increments of 15A.

(3) See safe operating area curves or contact the factory to determine the appropriate derating.

Output Capacitors: The PT7750 series requires a minimum output capacitance of 2000 μ F for proper operation. Do not use Oson type capacitors. The maximum allowable output capacitance is $(42,000 + V_{out})\mu\text{F}$ for the PT7751, $(96,000 + V_{out})\mu\text{F}$ for the PT7756, or 15,000 μ F, whichever is less.

Input Filter: An input inductor is optional for most applications. The input inductor must be sized to handle 94ADC with a typical value of 1 μ H. The input capacitance must be rated for a minimum of 8.0 Arms of ripple current when operated at maximum output current and maximum output voltage. Contact an applications engineer for input capacitor selection for applications at other output voltages and output currents.

PT7750 Series

15 Amp 24V Input "Big Hammer III"
Programmable ISR

Programming Information

VID3	VID2	VID1	VID0	PT7751		PT7756	
				VID4=1	VID4=0	VID4=1	VID4=0
1	1	1	1	2.5V	4.1V	6.6V	9.8V
1	1	1	0	2.6V	4.2V	6.8V	10.0V
1	1	0	1	2.7V	4.3V	7.0V	10.2V
1	1	0	0	2.8V	4.4V	7.2V	10.4V
1	0	1	1	2.9V	4.5V	7.4V	10.6V
1	0	1	0	3.0V	4.6V	7.6V	10.8V
1	0	0	1	3.1V	4.7V	7.8V	11.0V
1	0	0	0	3.2V	4.8V	8.0V	11.2V
0	1	1	1	3.3V	4.9V	8.2V	11.4V
0	1	1	0	3.4V	5.0V	8.4V	11.6V
0	1	0	1	3.5V	5.1V	8.6V	11.8V
0	1	0	0	3.6V	5.2V	8.8V	12.0V
0	0	1	1	3.7V	5.3V	9.0V	12.2V
0	0	1	0	3.8V	5.4V	9.2V	12.4V
0	0	0	1	3.9V	5.5V	9.4V	12.6V
0	0	0	0	4.0V	5.6V	9.6V	12.8V

Logic 0 = Pin 12 potential (remote sense gnd)

Logic 1 = Open circuit (no pull-up resistors)

VID3 and VID4 may not be changed while the unit is operating.

Ordering Information

PT7751□ = 2.5 to 5.6 Volts

PT7756□ = 6.6 to 12.8 Volts

(For dimensions and PC board layout,
see Package Styles 1000 and 1010.)

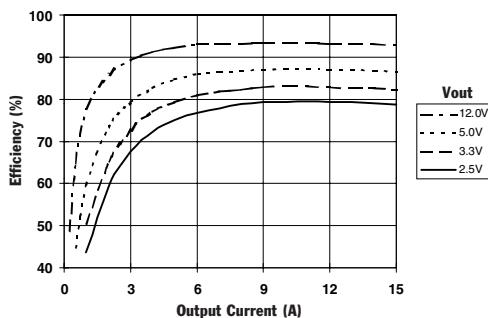
PT Series Suffix (PT1234X)

Case/Pin
Configuration

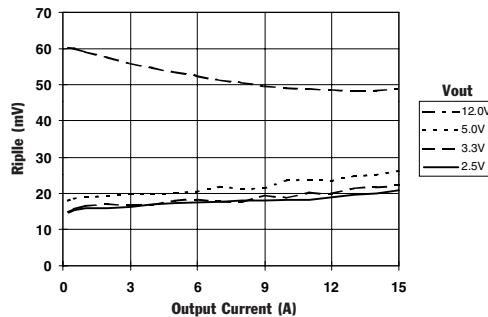
Vertical Through-Hole	N
Horizontal Through-Hole	A
Horizontal Surface Mount	C

TYPICAL CHARACTERISTICS

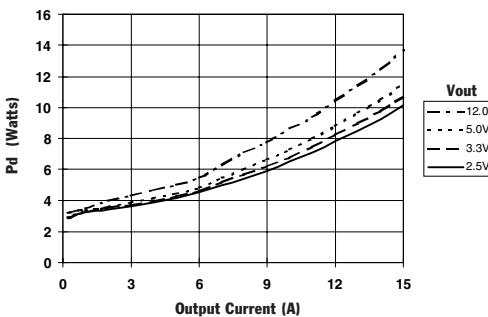
Efficiency vs Output Current (@Vin=+24V)



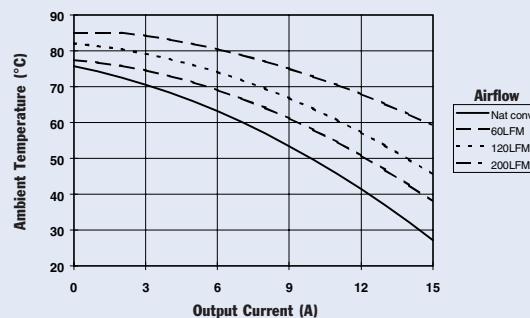
Output Ripple vs Output Current (@Vin=+24V)



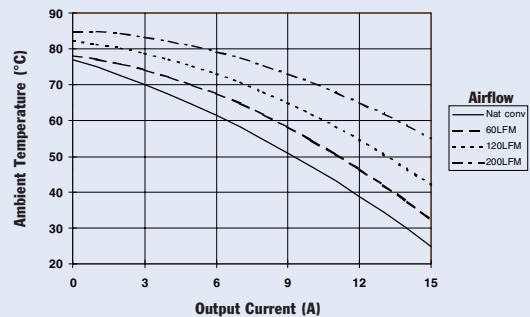
Power Dissipation vs Output Current (@Vin=+24V)



PT7751 Safe Operating Area (@Vin=+24V, Over V_o Range)



PT7756 Safe Operating Area (@Vin=+24V, Over V_o Range)



Note: SOA curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperatures.

Pin-Coded Output Voltage Adjustment on the “Big Hammer III” Series ISRs

Power Trends PT7750 series ISRs incorporating pin-coded voltage control, use pins 1, 2, 3, 4, & 6 to adjust the output voltage. The control pins are identified VID0 - VID4 respectively. When the control pins are left open-circuit, the ISR output will regulate at its factory trimmed output voltage. Each control pin is internally connected to a precision resistor, and when grounded increases the output voltage by a set amount. The internal resistors are binary code weighted, allowing the output voltage of the ISR to be programmed as a function of a binary code. VID0 represents the LSB, and VID4 the MSB (or range change bit). The output voltage ranges offered by these regulators are compatible with some microprocessors, and provide a convenient method of output voltage selection for many other applications. Refer to Figure 1 below for the connection schematic, and the PT7750 Data Sheet for the programming code information.

Notes:

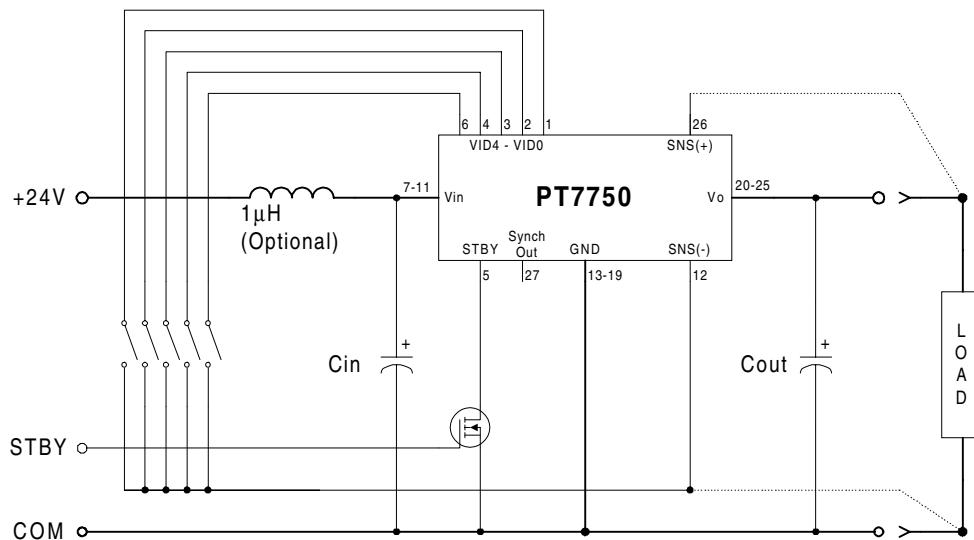
1. The programming convention is as follows:-
 1. Logic 0: Connect to pin12 (Remote Sense Ground).
 2. Logic 1: Open circuit/open drain (See notes 2, & 4)
2. Do not connect pull-up resistors to the voltage programming pins.
3. To minimize output voltage error, always use pin 12 (Remote Sense Ground) as the logic “0” reference. While the regular ground (pins 13-19) can also be used for programming, doing so will degrade the load regulation of the product.
4. If active devices are used to ground the voltage control

pins, low-level open drain MOSFET devices should be used over bipolar transistors. The inherent $V_{ce}(\text{sat})$ in bipolar devices introduces errors in the device's internal divider network. Discrete transistors such as the BSS138, 2N7002, IRLML2402, or the 74C906 hex open-drain buffer are examples of appropriate devices.

Active Voltage Programming:

Special precautions should be taken when making changes to the voltage control program code while the unit is powered. It is highly recommended that the ISR be either powered down or in standby. Changes made to the program code while V_{out} is enabled induces high current transients through the device. This is the result of the electrolytic output capacitors being either charged or discharged to the new output voltage set-point. The transient current can be minimized by making only incremental changes to the binary code, i.e. one LSB at a time. A minimum of 100 μ s settling time between each program state is also recommended. Making non-incremental changes to VID3 and VID4 with the output enabled is discouraged. If they are changed, the transients induced can overstress the device resulting in a permanent drop in efficiency. If the use of active devices prevents the program code being asserted prior to power-up, pull pin 5 (STBY) to the device GND during the period that the input voltage is applied to V_{in} . Releasing pin 5 will then allow the device output to execute a soft-start power-up to the programmed voltage. For more information on the use of the Standby function, consult the related application note, "Using the Standby Function on the 'Big Hammer III' Programmable ISR Series."

Figure 1



Using the Standby Function on the PT7750 "Big Hammer III" Programmable ISRs

For applications requiring output voltage On/Off control, the PT7750 "Big Hammer" ISRs incorporate a standby function¹. This feature may be used for power-up/shutdown sequencing, and to change the output voltage while input power is applied. *See related notes:* "Pin-coded Output Voltage Adjustment on the 'Big Hammer III' Series ISRs."

The standby function is provided by the *STBY** control, pin 5. If pin 5 is left open-circuit the regulator operates normally, providing a regulated output whenever a valid supply voltage is applied to V_{in} (pins 7-11) with respect to GND (pins 13-19). Connecting pin 5 to ground² will set the regulator output to zero volts³. This places the regulator in standby mode, and reduces the input current to typically 30mA (50mA max). If a ground signal is applied to pin 5 prior to power-up, the regulator output will be held at zero volts during the period that input power is applied.

The standby input must be controlled with an open-collector (or open-drain) discrete transistor (See Figure 1). Table 1 gives the threshold requirements.

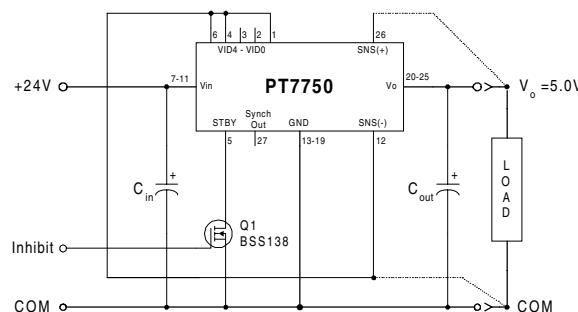
Table 1 Inhibit Control Threshold²

Parameter	Min	Max
Disable (VIL)	-0.1V	0.3V

Notes:

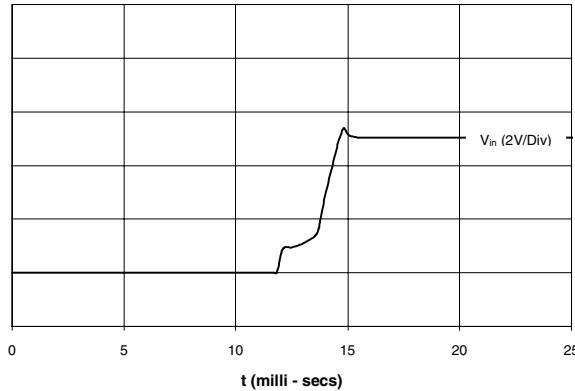
1. The Standby/Inhibit control logic is similar for all Power Trends' modules, but the flexibility and threshold tolerances will be different. For specific information on this function for other regulator models, consult the applicable application note.
2. The Standby input on the PT7750 regulator series must be controlled using an open-collector (or open-drain) discrete transistor. *Do Not* use a pull-up resistor. The control input has an open-circuit voltage of about 1.5Vdc. To set the regulator output to zero, the control pin must be "pulled" to less than 0.3Vdc with a low-level 0.1mA sink to ground.
3. When placed in the standby mode, the regulator output discharges the output capacitance with a low impedance to ground. If an external voltage is applied to the output, it will sink current and possibly over-stress the part.
4. The turn-off time of Q_1 , or rise time of the standby input is not critical on the PT7750 series. Turning Q_1 off slowly, over periods up to 100ms, will not affect regulator operation. However, a slow turn-off time will increase both the initial delay and rise-time of the output voltage.

Figure 1



Turn-On Time: Turning Q_1 in Figure 1 off, removes the low-voltage signal at pin 5 and enables the output. Following a brief delay of 8-18ms, the output voltage of the PT7750 series regulators rise to full regulation within 20ms⁴. Figure 2 shows the typical output voltage waveform of a PT7751 following the prompt turn-off of Q_1 at time $t = 0$ secs. The output voltage in Figure 1 is set to 5.0V by connecting VID0 (pin 1), VID3 (pin 4), and VID4 (pin 6) to the Remote Sense Gnd (pin 12)*. The waveform in Figure 2 was measured with a 24V input source voltage, and 10A resistive load.

Figure 2



* Consult the data sheet for details on other VID codes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT7751A	OBsolete SIP MODULE		EJF	27		TBD	Call TI	Call TI			

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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