

# F2 HERIC Inverter Module with PCM and NTC

## SNXH75M65L3F2STG

The SNXH75M65L3F2STG is the HERIC topology which is providing a high efficiency solution for the solar inverter application. The integrated high speed field stop IGBTs are providing lower conduction and switching losses. And the pre-applied PCM requires no additional process of the thermal interface material printing. Furthermore, the screw clamp provides a fast and reliable mounting method.

### Electrical Features

- High Efficiency
- Low Conduction and Switching Losses
- High Speed Field Stop IGBT
- Built-in NTC for Temperature Monitoring
- This is a Pb-Free Device

### Mechanical Features

- Full Plastic F2 Package
- Soldering Pin
- Al<sub>2</sub>O<sub>3</sub> DBC with Low Thermal Resistance
- Pre-applied PCM (Phase Change Material)

### Applications

- Solar Inverter

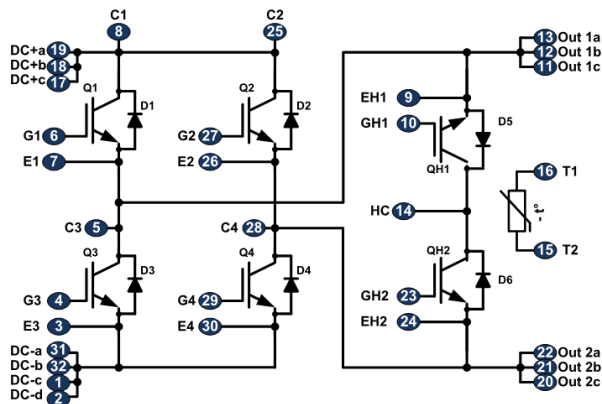
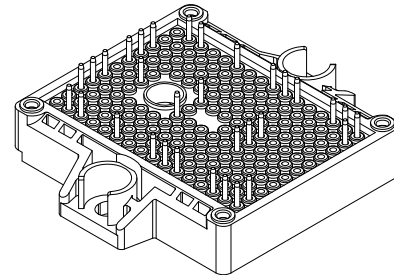


Figure 1. Internal Circuit Diagram



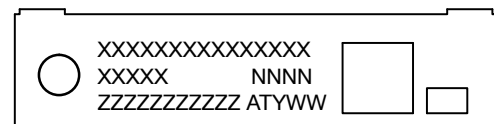
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**CODE: F2  
CASE MODGV**

### MARKING DIAGRAM



XXXX = Specific Device Code  
ZZZ = Lot ID  
AT = Assembly & Test Location  
Y = Year  
W = Work Week  
NNN = Serial Number

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# SNXH75M65L3F2STG

## PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	PCM	Packing Type	Quantity / Tray
SNXH75M65L3F2STG	SNXH75M65L3F2STG	F2	Yes	Tray	20

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Description	Condition	Rating	Units
<b>IGBT</b>				
V <sub>CES</sub>	Collector–Emitter Voltage		650	V
V <sub>GES</sub>	Gate–Emitter Voltage		±25	V
I <sub>C</sub>	Continuous Collector Current	T <sub>C</sub> = 80°C, T <sub>Jmax</sub> = 175°C	75	A
I <sub>CM</sub>	Pulsed Collector Current	limited by T <sub>Jmax</sub>	150	A
P <sub>D</sub>	Maximum Power Dissipation		236	W
T <sub>J</sub>	Operating Junction Temperature		–40 to +150	°C

## FULL-BRIDGE DIODE (D1, D2, D3, D4)

V <sub>RRM</sub>	Peak Repetitive Reverse Voltage		650	V
I <sub>F</sub>	Continuous Forward Current	T <sub>C</sub> = 80°C, T <sub>Jmax</sub> = 175°C	50	A
I <sub>FM</sub>	Maximum Forward Current		100	A
P <sub>D</sub>	Maximum Power Dissipation		208	W
T <sub>J</sub>	Operating Junction Temperature		–40 to +150	°C

## HERIC DIODE (D5, D6)

V <sub>RRM</sub>	Peak Repetitive Reverse Voltage		650	V
I <sub>F</sub>	Continuous Forward Current	T <sub>C</sub> = 80°C, T <sub>Jmax</sub> = 175°C	75	A
I <sub>FM</sub>	Maximum Forward Current		150	A
P <sub>D</sub>	Maximum Power Dissipation		272	W
T <sub>J</sub>	Operating Junction Temperature		–40 to +150	°C

## MODULE

T <sub>STG</sub>	Storage Temperature (Note 1)		–40 to +125	°C
V <sub>ISO</sub>	Isolation Voltage	AC 1 min.	2500	V
Iso_Material	Internal Isolation Material		Al <sub>2</sub> O <sub>3</sub>	–
T <sub>MOUNT</sub>	Mounting Torque (Note 2)	M4	2.4	N•m
Creepage	Terminal to Heat Sink		11.5	mm
	Terminal to Terminal		6.3	mm
Clearance	Terminal to Heat Sink		10.0	mm
	Terminal to Terminal		5.0	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. In the case of PCM pre-applied module, please refer to the application note (AN–4186)
2. Recommendable value : 2.0 ~ 2.4 Nm (M4)

# SNXH75M65L3F2STG

**ELECTRICAL CHARACTERISTICS**  $T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
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## IGBT

### OFF CHARACTERISTICS

$BV_{CES}$	Collector-Emitter Breakdown Voltage	$V_{GE} = 0\text{ V}, I_C = 1\text{ mA}$	650	–	–	V
$I_{CES}$	Collector Cut-off Current	$V_{CE} = V_{CES}, V_{GE} = 0\text{ V}$	–	–	250	$\mu\text{A}$
$I_{GES}$	Gate-Emitter Leakage Current	$V_{GE} = V_{GES}, V_{CE} = 0\text{ V}$	–	–	$\pm 2$	$\mu\text{A}$

### ON CHARACTERISTICS

$V_{GE(th)}$	Gate-Emitter Threshold Voltage	$V_{GE} = V_{CE}, I_C = 75\text{ mA}$	4.2	5.4	6.8	V
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 75\text{ A}, V_{GE} = 15\text{ V}$	–	1.58	2.2	V
		$I_C = 75\text{ A}, V_{GE} = 15\text{ V}, T_C = 125^\circ\text{C}$	–	1.85	–	V
$R_{LEAD}$	Lead Resistance of Pin to Chip	per Chip	–	3.3	–	m $\Omega$

### SWITCHING CHARACTERISTICS (Q2, Q3–D5 / Q1, Q4–D6)

$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 300\text{ V}$ $I_C = 75\text{ A}$ $V_{GE} = 15\text{ V}$ $R_G = 30\ \Omega$ Inductive Load $T_C = 25^\circ\text{C}$	–	75	–	ns
$t_r$	Rise Time		–	54	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	380	–	ns
$t_f$	Fall Time		–	52	–	ns
$E_{ON}$	Turn-On Switching Loss per Pulse		–	0.93	–	mJ
$E_{OFF}$	Turn-Off Switching Loss per Pulse		–	1.26	–	mJ
$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 300\text{ V}$ $I_C = 75\text{ A}$ $V_{GE} = 15\text{ V}$ $R_G = 30\ \Omega$ Inductive Load $T_C = 125^\circ\text{C}$	–	65	–	ns
$t_r$	Rise Time		–	59	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	410	–	ns
$t_f$	Fall Time		–	52	–	ns
$E_{ON}$	Turn-On Switching Loss per Pulse		–	1.66	–	mJ
$E_{OFF}$	Turn-Off Switching Loss per Pulse		–	1.53	–	mJ
$Q_g$	Total Gate Charge	$V_{CC} = 300\text{ V}, I_C = 75\text{ A},$ $V_{GE} = 0 \sim 15\text{ V}$	–	123	–	nC
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.63	$^\circ\text{C/W}$
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{PCM} = 3.4\text{ W/mK}$	–	0.49	–	$^\circ\text{C/W}$

### SWITCHING CHARACTERISTICS (QH1–D6 / QH2–D5)

$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 300\text{ V}$ $I_C = 75\text{ A}$ $V_{GE} = 15\text{ V}$ $R_G = 30\ \Omega$ Inductive Load $T_C = 25^\circ\text{C}$	–	78	–	ns
$t_r$	Rise Time		–	52	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	389	–	ns
$t_f$	Fall Time		–	29	–	ns
$E_{ON}$	Turn-On Switching Loss		–	0.92	–	mJ
$E_{OFF}$	Turn-Off Switching Loss		–	1.043	–	mJ
$t_{d(on)}$	Turn-On Delay Time	$V_{CC} = 300\text{ V}$ $I_C = 75\text{ A}$ $V_{GE} = 15\text{ V}$ $R_G = 30\ \Omega$ Inductive Load $T_C = 125^\circ\text{C}$	–	68	–	ns
$t_r$	Rise Time		–	58	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	429	–	ns
$t_f$	Fall Time		–	26	–	ns
$E_{ON}$	Turn-On Switching Loss		–	1.528	–	mJ
$E_{OFF}$	Turn-Off Switching Loss		–	1.247	–	mJ
$Q_g$	Total Gate Charge	$V_{CC} = 300\text{ V}, I_C = 75\text{ A},$ $V_{GE} = 0 \sim 15\text{ V}$	–	123	–	nC
$R_{\theta JC}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.63	$^\circ\text{C/W}$
$R_{\theta CH}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{PCM} = 3.4\text{ W/mK}$	–	0.49	–	$^\circ\text{C/W}$

# SNXH75M65L3F2STG

## ELECTRICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>FULL-BRIDGE DIODE (D1, D2, D3, D4)</b>						
$V_F$	Diode Forward Voltage	$I_F = 50\text{ A}$	–	2.03	2.8	V
		$I_F = 50\text{ A}, T_C = 125^\circ\text{C}$	–	1.7	–	V
$R_{\text{LEAD}}$	Lead Resistance of Pin to Chip	per Chip	–	3.4	–	$\text{m}\Omega$
$I_R$	Reverse Leakage Current	$V_R = 650\text{ V}$	–	–	250	$\mu\text{A}$
$I_{rr}$	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 50\text{ A}$ $di/dt = 1300\text{ A}/\mu\text{s}$ $T_C = 25^\circ\text{C}$	–	28	–	A
$Q_{rr}$	Reverse Recovery Charge		–	0.5	–	$\mu\text{C}$
$E_{rec}$	Reverse Recovery Energy		–	51	–	$\mu\text{J}$
$I_{rr}$	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 50\text{ A}$ $di/dt = 1300\text{ A}/\mu\text{s}$ $T_C = 125^\circ\text{C}$	–	40	–	A
$Q_{rr}$	Reverse Recovery Charge		–	1.2	–	$\mu\text{C}$
$E_{rec}$	Reverse Recovery Energy		–	145	–	$\mu\text{J}$
$R_{\theta\text{JC}}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.72	$^\circ\text{C}/\text{W}$
$R_{\theta\text{CH}}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{\text{PCM}} = 3.4\text{ W/mK}$	–	0.38	–	$^\circ\text{C}/\text{W}$

## HERIC DIODE (D5, D6)

$V_F$	Diode Forward Voltage	$I_F = 75\text{ A}$	–	2.28	2.9	V
		$I_F = 75\text{ A}, T_C = 125^\circ\text{C}$	–	1.74	–	V
$R_{\text{LEAD}}$	Lead Resistance of Pin to Chip	per Chip	–	1.1	–	$\text{m}\Omega$
$I_R$	Reverse Leakage Current	$V_R = 650\text{ V}$	–	–	250	$\mu\text{A}$
$I_{rr}$	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 75\text{ A}$ $di/dt = 1220\text{ A}/\mu\text{s}$ $T_C = 25^\circ\text{C}$	–	32	–	A
$Q_{rr}$	Reverse Recovery Charge		–	0.79	–	$\mu\text{C}$
$E_{rec}$	Reverse Recovery Energy		–	113	–	$\mu\text{J}$
$I_{rr}$	Reverse Recovery Current	$V_R = 300\text{ V}, I_F = 75\text{ A}$ $di/dt = 1220\text{ A}/\mu\text{s}$ $T_C = 125^\circ\text{C}$	–	52	–	A
$Q_{rr}$	Reverse Recovery Charge		–	1.9	–	$\mu\text{C}$
$E_{rec}$	Reverse Recovery Energy		–	288	–	$\mu\text{J}$
$R_{\theta\text{JC}}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.55	$^\circ\text{C}/\text{W}$
$R_{\theta\text{CH}}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{\text{PCM}} = 3.4\text{ W/mK}$	–	0.39	–	$^\circ\text{C}/\text{W}$

## NTC (Thermistor)

$R_{\text{NTC}}$	Rated Resistance	$T_C = 25^\circ\text{C}$	–	10	–	$\text{k}\Omega$
		$T_C = 100^\circ\text{C}$	–	936	–	$\Omega$
	Tolerance	$T_C = 25^\circ\text{C}$	–3	–	+3	%
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	–	–	20	mW
$B_{\text{Value}}$	B-Constant	$B_{25/50}$	–	3450	–	K
		$B_{25/100}$	–	3513	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

# SNXH75M65L3F2STG

## TYPICAL CHARACTERISTICS – IGBT

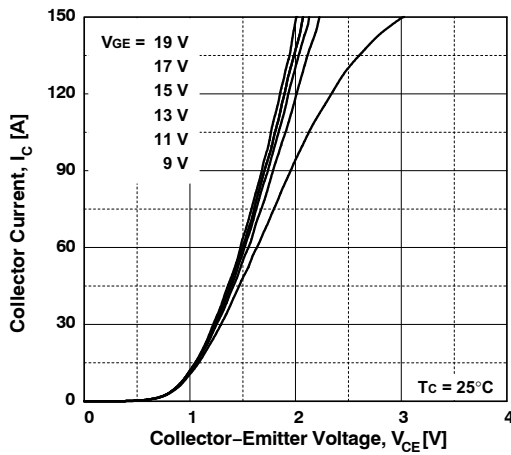


Figure 2. Output Characteristics

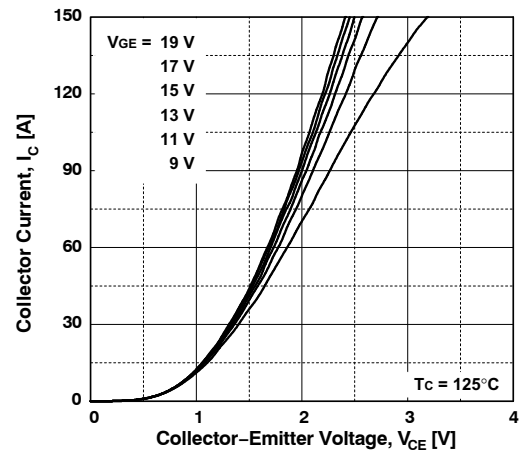


Figure 3. Output Characteristics

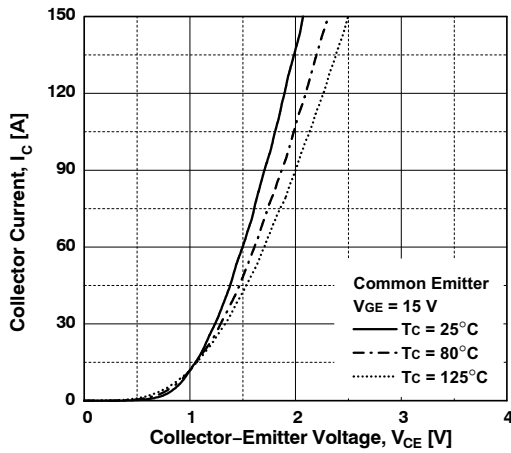


Figure 4. Saturation Voltage Characteristics

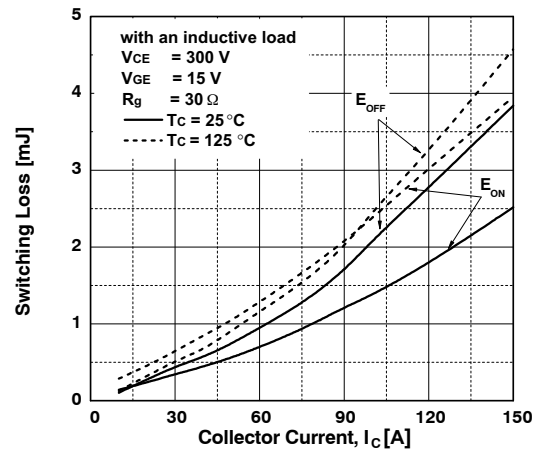


Figure 5. Switching Loss vs. Collector Current

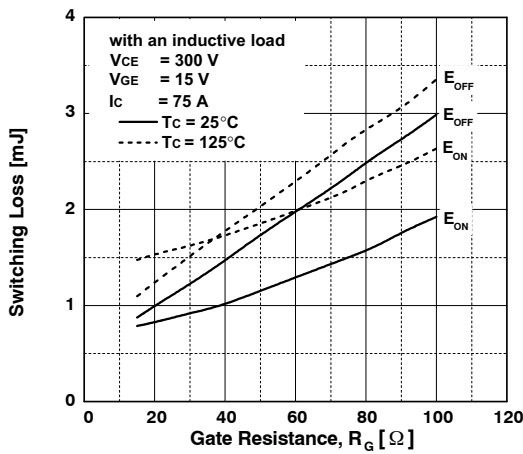


Figure 6. Switching Loss vs. Gate Resistance

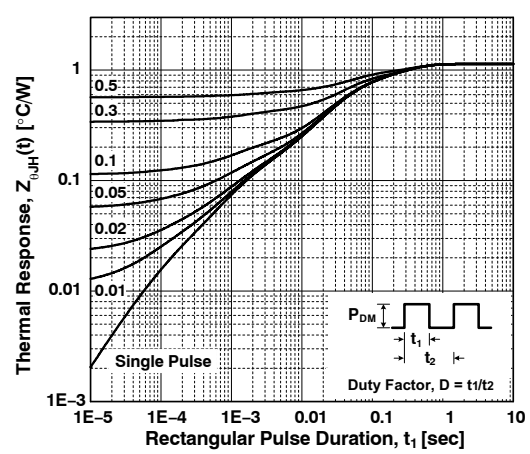


Figure 7. Transient Thermal Impedance

TYPICAL CHARACTERISTICS – FULL-BRIDGE DIODE

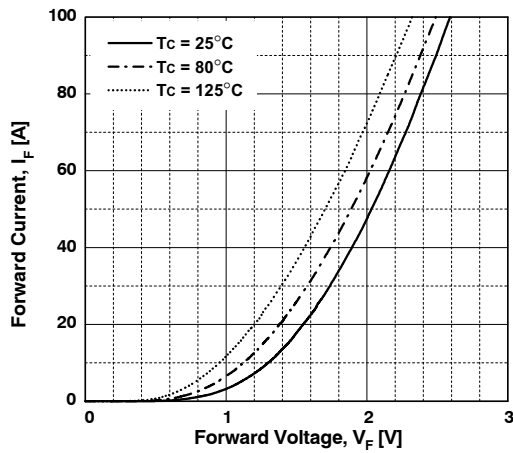


Figure 8. Forward Voltage Drop

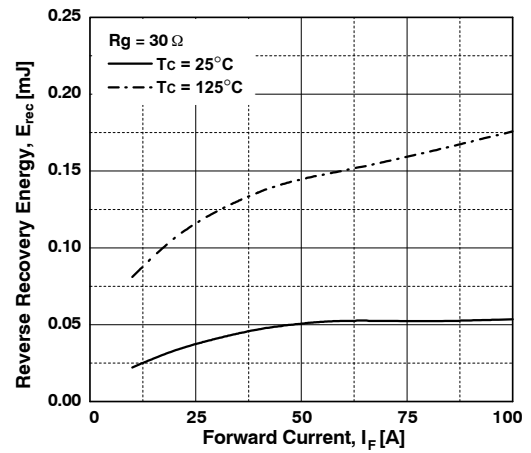


Figure 9. Reverse Recovery Energy vs. Forward Current

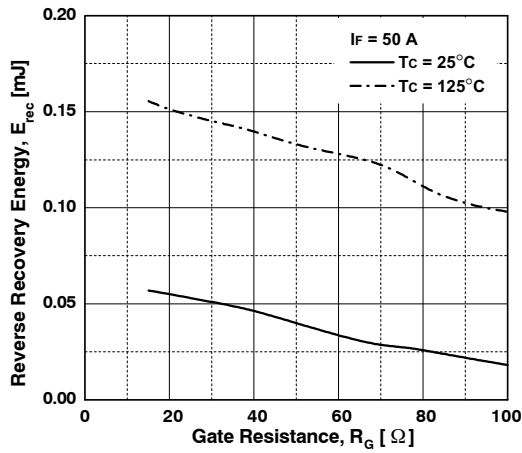


Figure 10. Reverse Recovery Energy vs. Gate Resistance

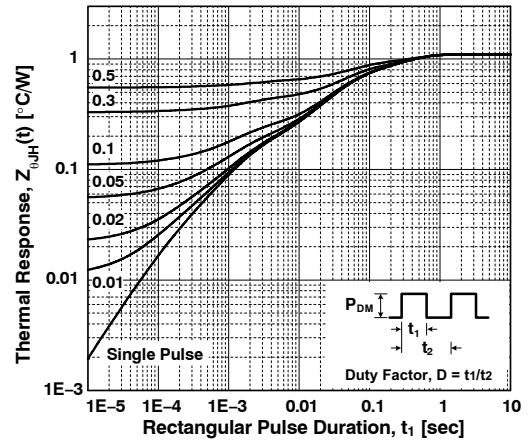


Figure 11. Transient Thermal Impedance

# SNXH75M65L3F2STG

## TYPICAL CHARACTERISTICS – HERIC DIODE

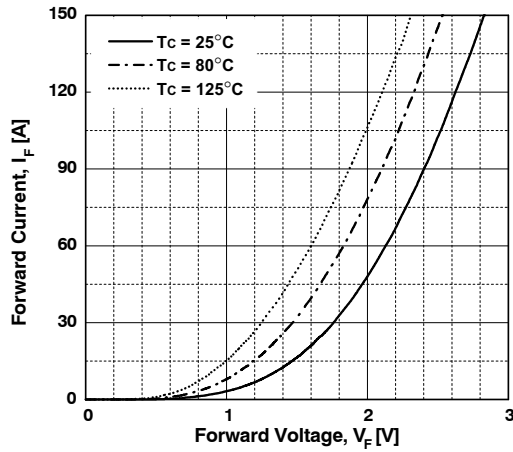


Figure 12. Forward Voltage Drop

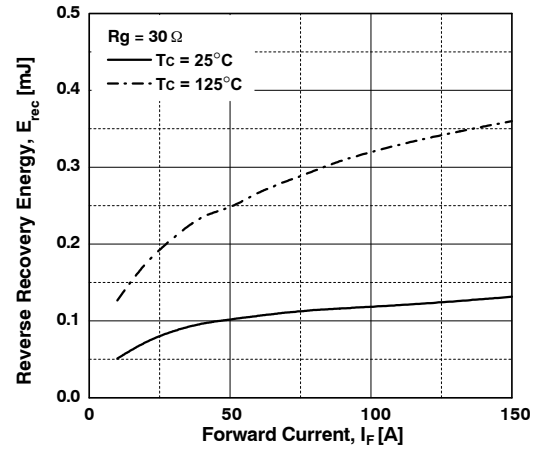


Figure 13. Reverse Recovery Energy vs. Forward Current

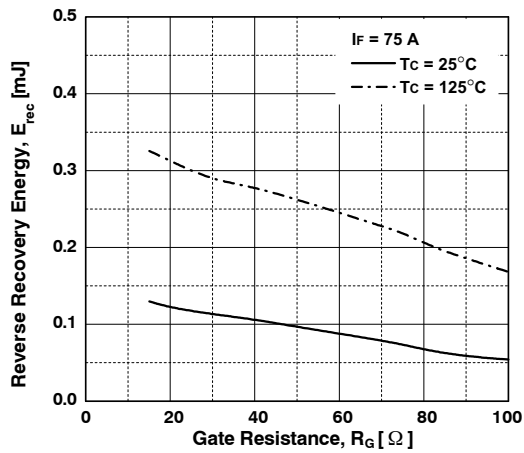


Figure 14. Reverse Recovery Energy vs. Gate Resistance

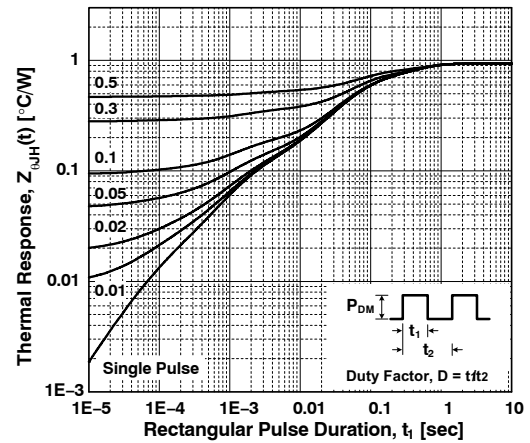


Figure 15. Transient Thermal Impedance

# SNXH75M65L3F2STG

## PACKAGE DIMENSIONS

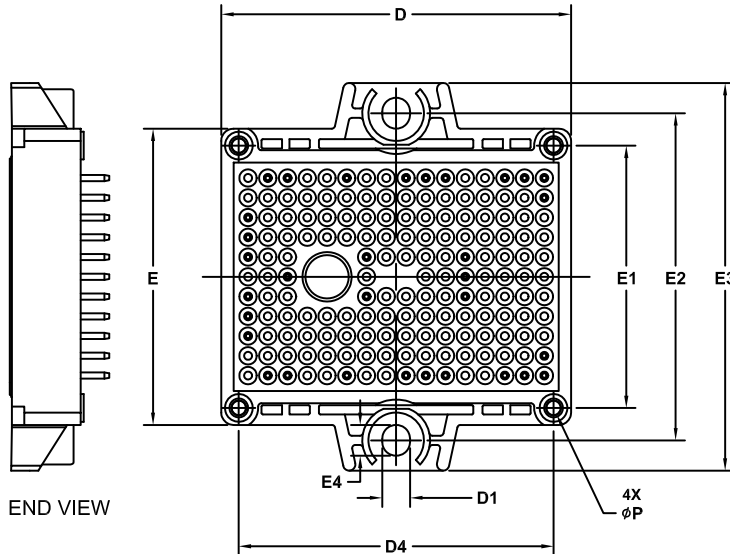
### PIM32 56.7x42.5 (SOLDERING PIN)

CASE MODGV  
ISSUE A

#### NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS

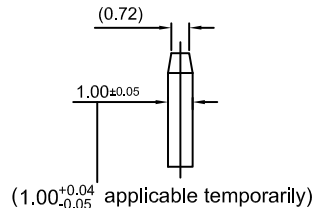
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	15.65	16.15	16.65
D	56.40	56.70	57.00
D1	4.40	4.50	4.60
D4	50.85	51.00	51.15
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40



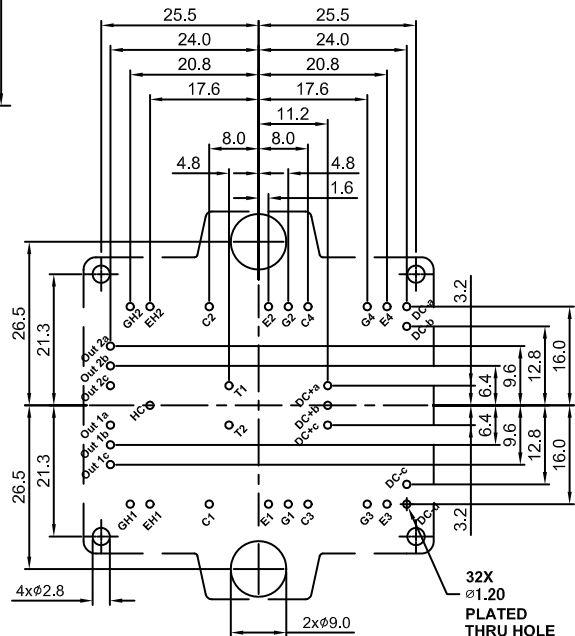
END VIEW

TOP VIEW

SIDE VIEW




PIN DESIGN



PCB HOLE PATTERN

(View from PCB Top Layer downward to backside of PCB Layer)

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