

F2 HERIC Inverter Module with PCM and NTC

SNXH75M65L3F2STG

The SNXH75M65L3F2STG is the HERIC topology which is providing a high efficiency solution for the solar inverter application. The integrated high speed field stop IGBTs are providing lower conduction and switching losses. And the pre-applied PCM requires no additional process of the thermal interface material printing. Furthermore, the screw clamp provides a fast and reliable mounting method.

Electrical Features

- High Efficiency
- Low Conduction and Switching Losses
- High Speed Field Stop IGBT
- Built-in NTC for Temperature Monitoring
- This is a Pb-Free Device

Mechanical Features

- Full Plastic F2 Package
- Soldering Pin
- Al_2O_3 DBC with Low Thermal Resistance
- Pre-applied PCM (Phase Change Material)

Applications

- Solar Inverter

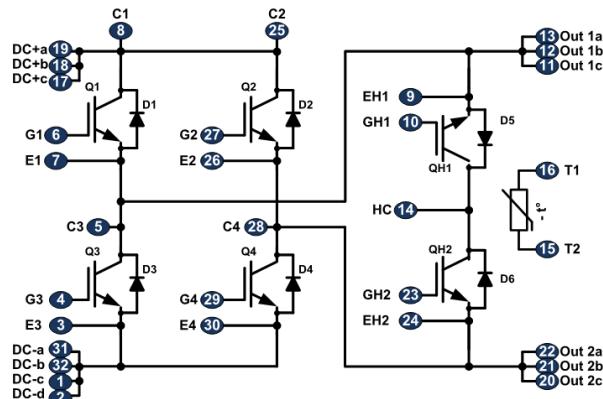
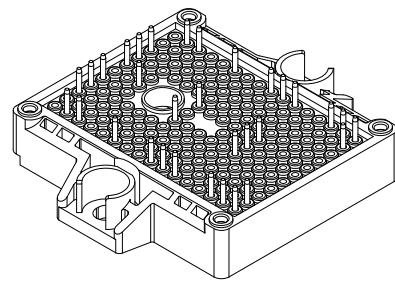


Figure 1. Internal Circuit Diagram



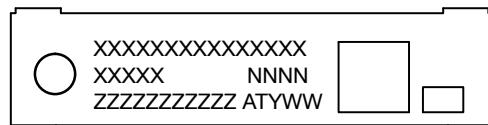
ON Semiconductor®

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CODE: F2
CASE MODGV

MARKING DIAGRAM



XXXX = Specific Device Code
ZZZ = Lot ID
AT = Assembly & Test Location
Y = Year
W = Work Week
NNN = Serial Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

SNXH75M65L3F2STG

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	PCM	Packing Type	Quantity / Tray
SNXH75M65L3F2STG	SNXH75M65L3F2STG	F2	Yes	Tray	20

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Description	Condition	Rating	Units
IGBT				
V_{CES}	Collector-Emitter Voltage		650	V
V_{GES}	Gate-Emitter Voltage		± 25	V
I_C	Continuous Collector Current	$T_C = 80^\circ\text{C}, T_{Jmax} = 175^\circ\text{C}$	75	A
I_{CM}	Pulsed Collector Current	limited by T_{Jmax}	150	A
P_D	Maximum Power Dissipation		236	W
T_J	Operating Junction Temperature		-40 to +150	$^\circ\text{C}$

FULL-BRIDGE DIODE (D1, D2, D3, D4)

V_{RRM}	Peak Repetitive Reverse Voltage		650	V
I_F	Continuous Forward Current	$T_C = 80^\circ\text{C}, T_{Jmax} = 175^\circ\text{C}$	50	A
I_{FM}	Maximum Forward Current		100	A
P_D	Maximum Power Dissipation		208	W
T_J	Operating Junction Temperature		-40 to +150	$^\circ\text{C}$

HERIC DIODE (D5, D6)

V_{RRM}	Peak Repetitive Reverse Voltage		650	V
I_F	Continuous Forward Current	$T_C = 80^\circ\text{C}, T_{Jmax} = 175^\circ\text{C}$	75	A
I_{FM}	Maximum Forward Current		150	A
P_D	Maximum Power Dissipation		272	W
T_J	Operating Junction Temperature		-40 to +150	$^\circ\text{C}$

MODULE

T_{STG}	Storage Temperature (Note 1)		-40 to +125	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	AC 1 min.	2500	V
Iso._Material	Internal Isolation Material		Al ₂ O ₃	-
T_{MOUNT}	Mounting Torque (Note 2)	M4	2.4	Nm
Creepage	Terminal to Heat Sink		11.5	mm
	Terminal to Terminal		6.3	mm
Clearance	Terminal to Heat Sink		10.0	mm
	Terminal to Terminal		5.0	mm

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. In the case of PCM pre-applied module, please refer to the application note (AN-4186)
2. Recommendable value : 2.0 ~ 2.4 Nm (M4)

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ELECTRICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
IGBT						
OFF CHARACTERISTICS						
BV_{CES}	Collector-Emitter Breakdown Voltage	$\text{V}_{\text{GE}} = 0 \text{ V}$, $\text{I}_C = 1 \text{ mA}$	650	–	–	V
I_{CES}	Collector Cut-off Current	$\text{V}_{\text{CE}} = \text{V}_{\text{CES}}$, $\text{V}_{\text{GE}} = 0 \text{ V}$	–	–	250	μA
I_{GES}	Gate-Emitter Leakage Current	$\text{V}_{\text{GE}} = \text{V}_{\text{GES}}$, $\text{V}_{\text{CE}} = 0 \text{ V}$	–	–	± 2	μA
ON CHARACTERISTICS						
$\text{V}_{\text{GE}(\text{th})}$	Gate-Emitter Threshold Voltage	$\text{V}_{\text{GE}} = \text{V}_{\text{CE}}$, $\text{I}_C = 75 \text{ mA}$	4.2	5.4	6.8	V
$\text{V}_{\text{CE}(\text{sat})}$	Collector-Emitter Saturation Voltage	$\text{I}_C = 75 \text{ A}$, $\text{V}_{\text{GE}} = 15 \text{ V}$	–	1.58	2.2	V
		$\text{I}_C = 75 \text{ A}$, $\text{V}_{\text{GE}} = 15 \text{ V}$, $T_C = 125^\circ\text{C}$	–	1.85	–	V
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	–	3.3	–	$\text{m}\Omega$
SWITCHING CHARACTERISTICS (Q2, Q3-D5 / Q1, Q4-D6)						
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$\text{V}_{\text{CC}} = 300 \text{ V}$ $\text{I}_C = 75 \text{ A}$ $\text{V}_{\text{GE}} = 15 \text{ V}$ $\text{R}_G = 30 \Omega$ Inductive Load $T_C = 25^\circ\text{C}$	–	75	–	ns
t_r	Rise Time		–	54	–	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		–	380	–	ns
t_f	Fall Time		–	52	–	ns
E_{ON}	Turn-On Switching Loss per Pulse		–	0.93	–	mJ
E_{OFF}	Turn-Off Switching Loss per Pulse		–	1.26	–	mJ
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$\text{V}_{\text{CC}} = 300 \text{ V}$ $\text{I}_C = 75 \text{ A}$ $\text{V}_{\text{GE}} = 15 \text{ V}$ $\text{R}_G = 30 \Omega$ Inductive Load $T_C = 125^\circ\text{C}$	–	65	–	ns
t_r	Rise Time		–	59	–	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		–	410	–	ns
t_f	Fall Time		–	52	–	ns
E_{ON}	Turn-On Switching Loss per Pulse		–	1.66	–	mJ
E_{OFF}	Turn-Off Switching Loss per Pulse		–	1.53	–	mJ
Q_g	Total Gate Charge	$\text{V}_{\text{CC}} = 300 \text{ V}$, $\text{I}_C = 75 \text{ A}$, $\text{V}_{\text{GE}} = 0 \sim 15 \text{ V}$	–	123	–	nC
$R_{\theta\text{JC}}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.63	$^\circ\text{C}/\text{W}$
$R_{\theta\text{CH}}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{\text{PCM}} = 3.4 \text{ W/mK}$	–	0.49	–	$^\circ\text{C}/\text{W}$
SWITCHING CHARACTERISTICS (QH1-D6 / QH2-D5)						
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$\text{V}_{\text{CC}} = 300 \text{ V}$ $\text{I}_C = 75 \text{ A}$ $\text{V}_{\text{GE}} = 15 \text{ V}$ $\text{R}_G = 30 \Omega$ Inductive Load $T_C = 25^\circ\text{C}$	–	78	–	ns
t_r	Rise Time		–	52	–	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		–	389	–	ns
t_f	Fall Time		–	29	–	ns
E_{ON}	Turn-On Switching Loss		–	0.92	–	mJ
E_{OFF}	Turn-Off Switching Loss		–	1.043	–	mJ
$t_{\text{d}(\text{on})}$	Turn-On Delay Time	$\text{V}_{\text{CC}} = 300 \text{ V}$ $\text{I}_C = 75 \text{ A}$ $\text{V}_{\text{GE}} = 15 \text{ V}$ $\text{R}_G = 30 \Omega$ Inductive Load $T_C = 125^\circ\text{C}$	–	68	–	ns
t_r	Rise Time		–	58	–	ns
$t_{\text{d}(\text{off})}$	Turn-Off Delay Time		–	429	–	ns
t_f	Fall Time		–	26	–	ns
E_{ON}	Turn-On Switching Loss		–	1.528	–	mJ
E_{OFF}	Turn-Off Switching Loss		–	1.247	–	mJ
Q_g	Total Gate Charge	$\text{V}_{\text{CC}} = 300 \text{ V}$, $\text{I}_C = 75 \text{ A}$, $\text{V}_{\text{GE}} = 0 \sim 15 \text{ V}$	–	123	–	nC
$R_{\theta\text{JC}}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.63	$^\circ\text{C}/\text{W}$
$R_{\theta\text{CH}}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{\text{PCM}} = 3.4 \text{ W/mK}$	–	0.49	–	$^\circ\text{C}/\text{W}$

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ELECTRICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FULL-BRIDGE DIODE (D1, D2, D3, D4)						
V_F	Diode Forward Voltage	$I_F = 50 \text{ A}$	–	2.03	2.8	V
		$I_F = 50 \text{ A}, T_C = 125^\circ\text{C}$	–	1.7	–	V
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	–	3.4	–	$\text{m}\Omega$
I_R	Reverse Leakage Current	$V_R = 650 \text{ V}$	–	–	250	μA
I_{rr}	Reverse Recovery Current	$V_R = 300 \text{ V}, I_F = 50 \text{ A}$ $\text{di/dt} = 1300 \text{ A}/\mu\text{s}$ $T_C = 25^\circ\text{C}$	–	28	–	A
Q_{rr}	Reverse Recovery Charge		–	0.5	–	μC
E_{rec}	Reverse Recovery Energy		–	51	–	μJ
I_{rr}	Reverse Recovery Current	$V_R = 300 \text{ V}, I_F = 50 \text{ A}$ $\text{di/dt} = 1300 \text{ A}/\mu\text{s}$ $T_C = 125^\circ\text{C}$	–	40	–	A
Q_{rr}	Reverse Recovery Charge		–	1.2	–	μC
E_{rec}	Reverse Recovery Energy		–	145	–	μJ
$R_{\theta\text{JC}}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.72	$^\circ\text{C}/\text{W}$
$R_{\theta\text{CH}}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{\text{PCM}} = 3.4 \text{ W/mK}$	–	0.38	–	$^\circ\text{C}/\text{W}$
HERIC DIODE (D5, D6)						
V_F	Diode Forward Voltage	$I_F = 75 \text{ A}$	–	2.28	2.9	V
		$I_F = 75 \text{ A}, T_C = 125^\circ\text{C}$	–	1.74	–	V
R_{LEAD}	Lead Resistance of Pin to Chip	per Chip	–	1.1	–	$\text{m}\Omega$
I_R	Reverse Leakage Current	$V_R = 650 \text{ V}$	–	–	250	μA
I_{rr}	Reverse Recovery Current	$V_R = 300 \text{ V}, I_F = 75 \text{ A}$ $\text{di/dt} = 1220 \text{ A}/\mu\text{s}$ $T_C = 25^\circ\text{C}$	–	32	–	A
Q_{rr}	Reverse Recovery Charge		–	0.79	–	μC
E_{rec}	Reverse Recovery Energy		–	113	–	μJ
I_{rr}	Reverse Recovery Current	$V_R = 300 \text{ V}, I_F = 75 \text{ A}$ $\text{di/dt} = 1220 \text{ A}/\mu\text{s}$ $T_C = 125^\circ\text{C}$	–	52	–	A
Q_{rr}	Reverse Recovery Charge		–	1.9	–	μC
E_{rec}	Reverse Recovery Energy		–	288	–	μJ
$R_{\theta\text{JC}}$	Thermal Resistance of Junction to Case	per Chip	–	–	0.55	$^\circ\text{C}/\text{W}$
$R_{\theta\text{CH}}$	Thermal Resistance of Case to Heat sink	per Chip, $\lambda_{\text{PCM}} = 3.4 \text{ W/mK}$	–	0.39	–	$^\circ\text{C}/\text{W}$
NTC (Thermistor)						
R_{NTC}	Rated Resistance	$T_C = 25^\circ\text{C}$	–	10	–	$\text{k}\Omega$
		$T_C = 100^\circ\text{C}$	–	936	–	Ω
P_D	Tolerance	$T_C = 25^\circ\text{C}$	–3	–	+3	%
		$T_C = 25^\circ\text{C}$	–	–	20	mW
B_{Value}	B-Constant	$B_{25/50}$	–	3450	–	K
		$B_{25/100}$	–	3513	–	K

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS – IGBT

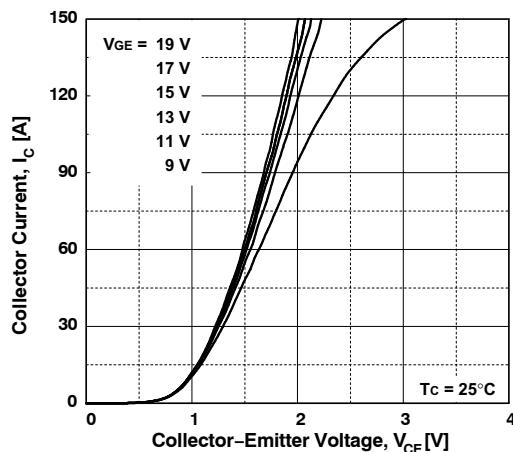


Figure 2. Output Characteristics

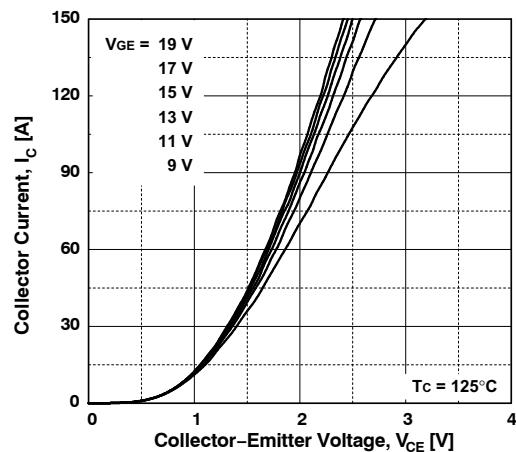


Figure 3. Output Characteristics

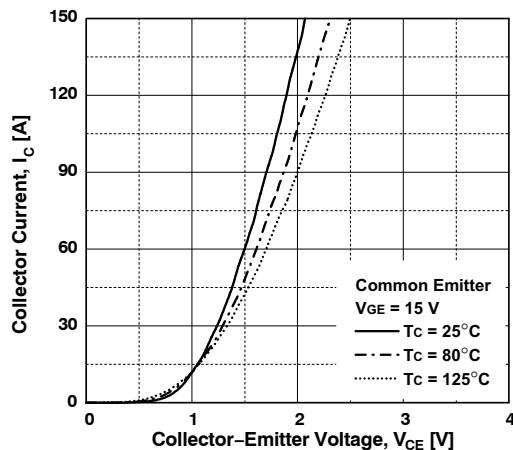


Figure 4. Saturation Voltage Characteristics

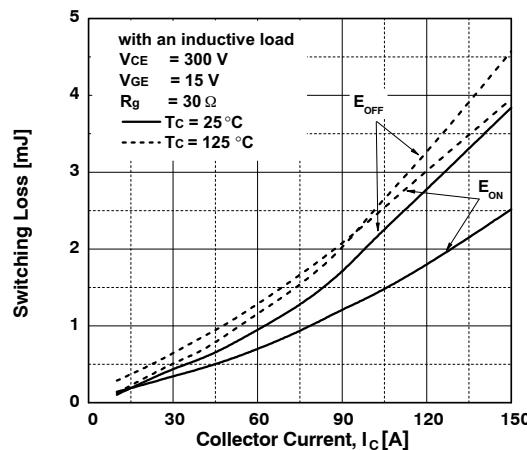


Figure 5. Switching Loss vs. Collector Current

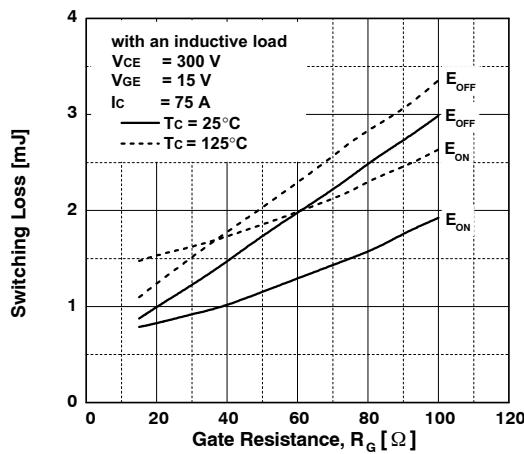


Figure 6. Switching Loss vs. Gate Resistance

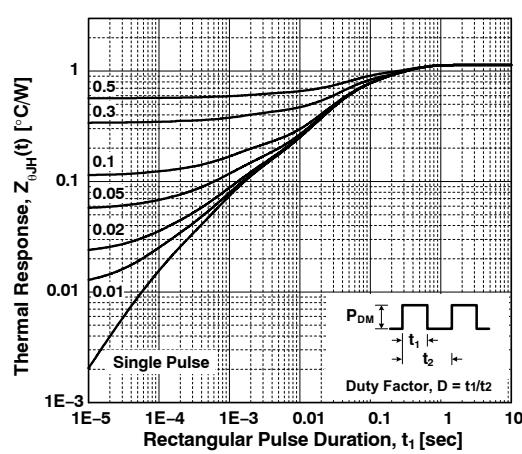


Figure 7. Transient Thermal Impedance

TYPICAL CHARACTERISTICS – FULL-BRIDGE DIODE

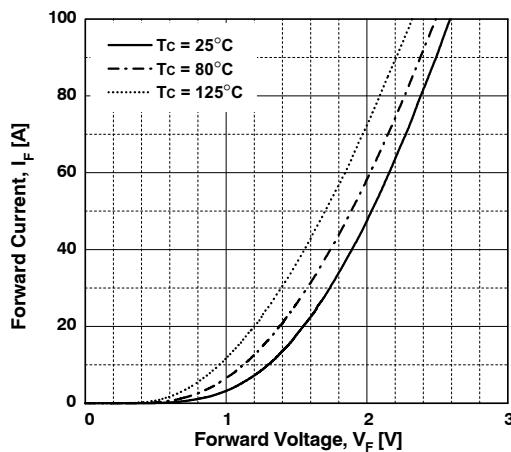


Figure 8. Forward Voltage Drop

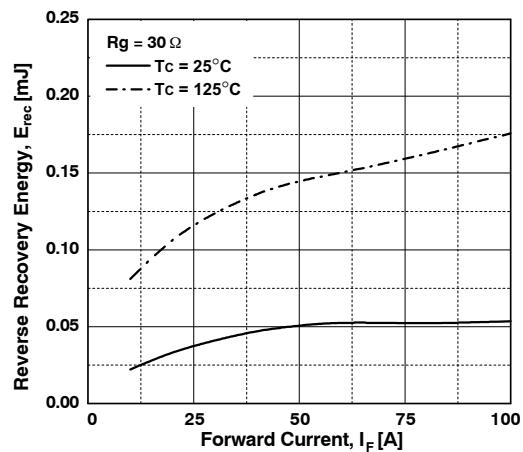


Figure 9. Reverse Recovery Energy vs. Forward Current

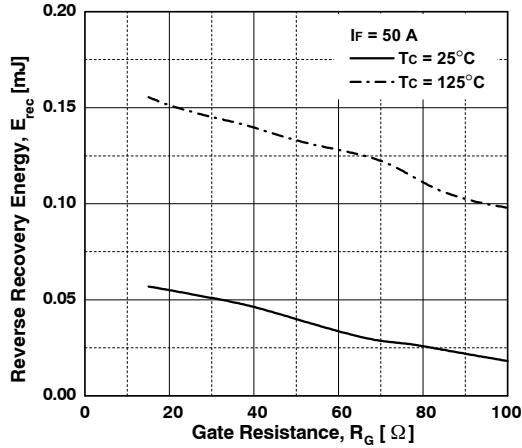


Figure 10. Reverse Recovery Energy vs. Gate Resistance

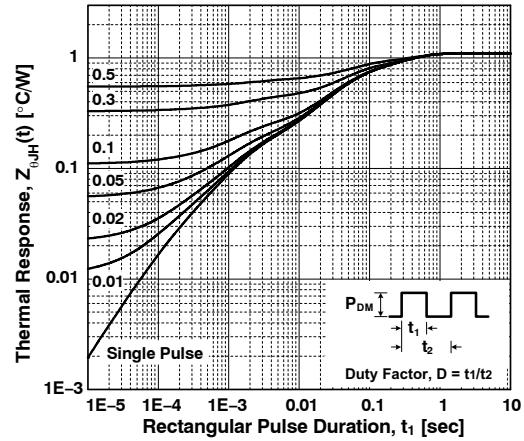


Figure 11. Transient Thermal Impedance

TYPICAL CHARACTERISTICS – HERIC DIODE

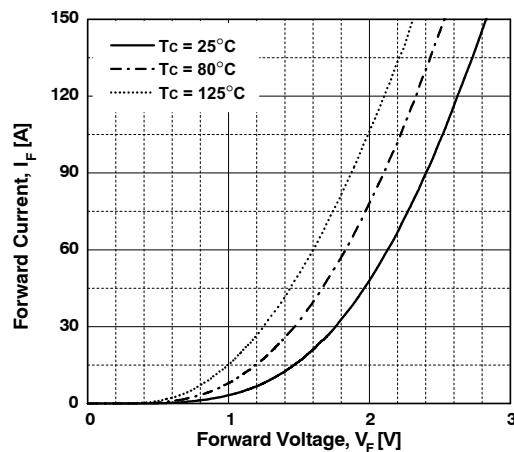


Figure 12. Forward Voltage Drop

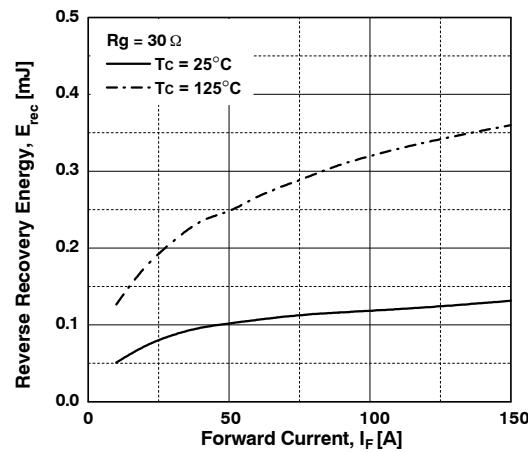


Figure 13. Reverse Recovery Energy vs. Forward Current

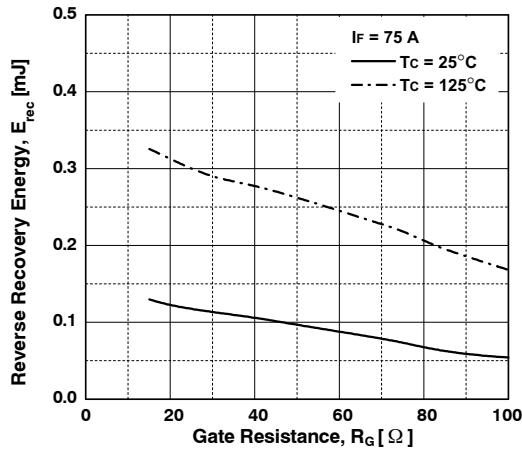


Figure 14. Reverse Recovery Energy vs. Gate Resistance

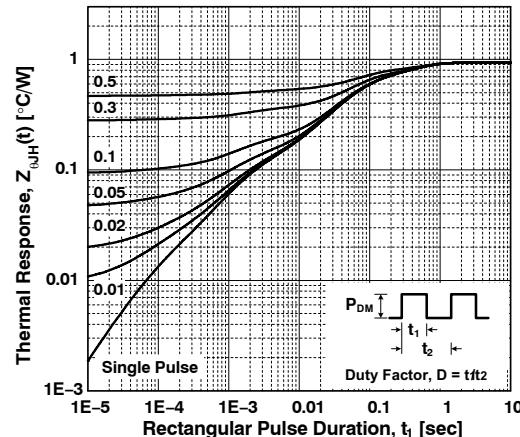
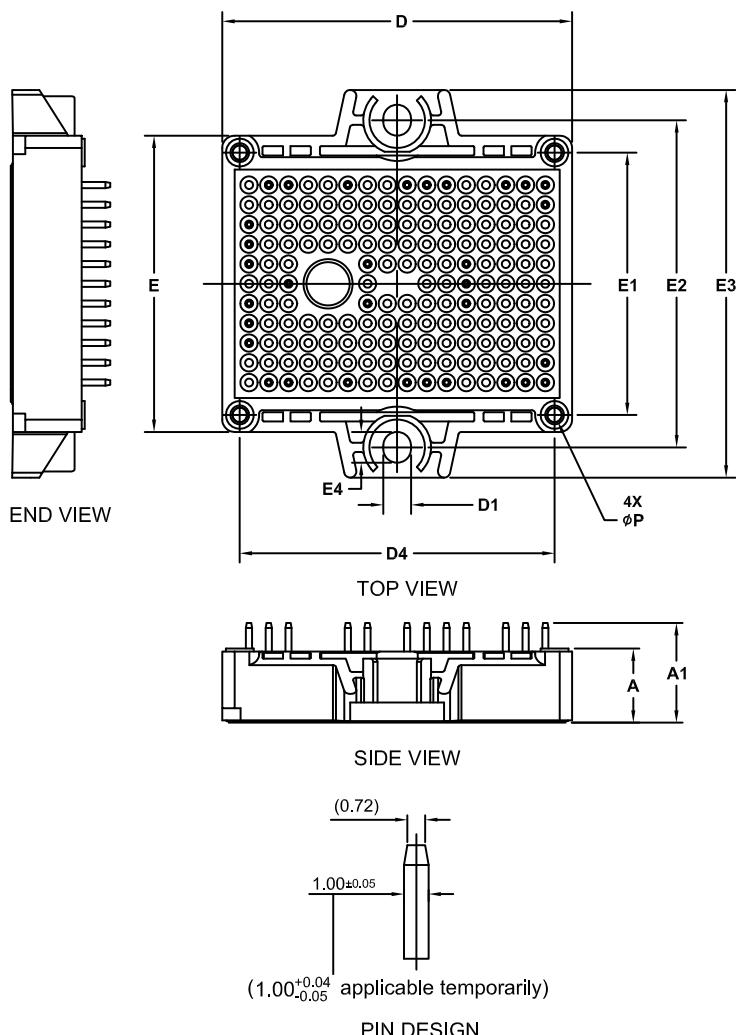


Figure 15. Transient Thermal Impedance

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PACKAGE DIMENSIONS

PIM32 56.7x42.5 (SOLDERING PIN) CASE MODGV ISSUE A

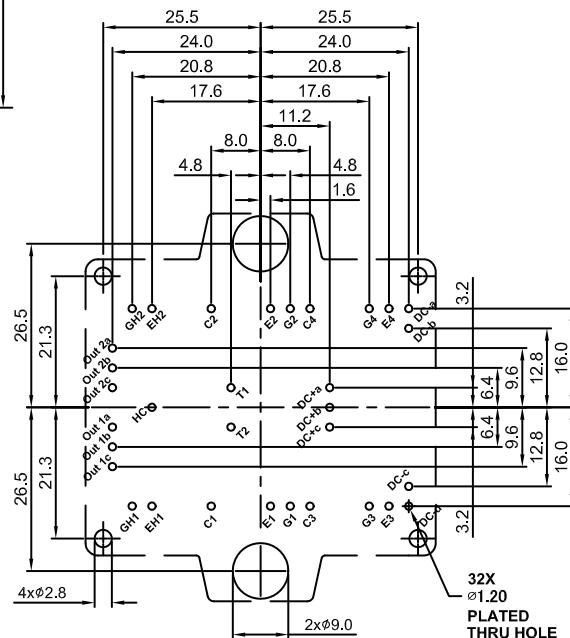


PIN DESIGN

NOTES:

1. CONTROLLING DIMENSION: MILLIMETERS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	11.65	12.00	12.35
A1	15.65	16.15	16.65
D	56.40	56.70	57.00
D1	4.40	4.50	4.60
D4	50.85	51.00	51.15
E	47.70	48.00	48.30
E1	42.35	42.50	42.65
E2	52.90	53.00	53.10
E3	62.30	62.80	63.30
E4	4.90	5.00	5.10
P	2.20	2.30	2.40



PCB HOLE PATTERN

(View from PCB Top Layer downward to backside of PCB Layer)

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