FAIRCHILD
SEMICONDUCTOR™

FEATURING
Extended Commercial Temperature Range
-20°C to 70°C
for Portable Handheld Equipment

ML4851

Low Current, Voltage Boost Regulator

GENERAL DESCRIPTION

The ML4851 is a low power boost regulator designed for DC to DC conversion in 1 to 3 cell battery powered systems. The maximum switching frequency can exceed 100kHz, allowing the use of small, low cost inductors.

The combination of BiCMOS process technology, internal synchronous rectification, variable frequency operation, and low supply current make the ML4851 ideal for 1 cell applications. The ML4851 is capable of start-up with input voltages as low as 1V and is available in 5V and 3.3V output versions with output voltage accuracy of ±3%.

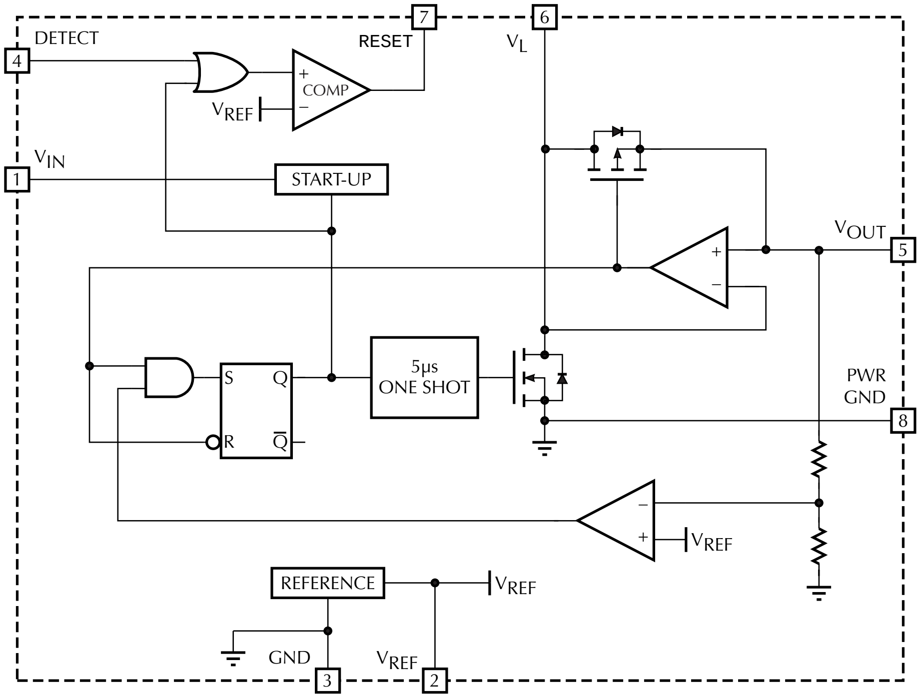
An integrated synchronous rectifier eliminates the need for an external Schottky diode and provides a lower forward voltage drop, resulting in higher conversion efficiency. In addition, low quiescent battery current and variable frequency operation result in high efficiency even at light loads. The ML4851 requires only one inductor and two capacitors to build a very small regulator circuit capable of achieving conversion efficiencies in excess of 90%.

The circuit also contains a $\overline{\text{RESET}}$ output which goes low when the IC can no longer function due to low input voltage, or when the DETECT input drops below 200mV.

FEATURES

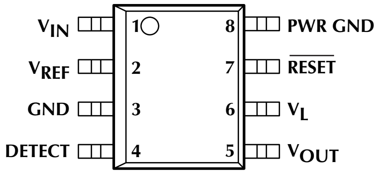
- Guaranteed full load start-up and operation at 1V input
- Maximum switching frequency > 100kHz
- Pulse Frequency Modulation (PFM) and internal synchronous rectification for high efficiency
- Minimum external components
- Low ON resistance internal switching FETs
- Micropower operation
- 5V and 3.3V output versions

BLOCK DIAGRAM



PIN CONFIGURATION

ML4851
8-Pin SOIC (S08)



TOP VIEW

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	V_{IN}	Battery input voltage
2	V_{REF}	200mV reference output
3	GND	Analog signal ground
4	DETECT	Pulling this pin below V_{REF} causes the $\overline{RESET}$ pin to go low
5	V_{OUT}	Boost regulator output
6	V_L	Boost inductor connection
7	$\overline{RESET}$	Output goes low when regulation cannot be achieved, or when DETECT goes below V_{REF}
8	PWR GND	Return for the NMOS output transistor

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{OUT}	7V
Voltage on any other pin	GND – 0.3V to V_{OUT} + 0.3V
Peak Switch Current, $I_{(PEAK)}$	1A
Average Switch Current, $I_{(AVG)}$	250mA
Junction Temperature	150ºC
Storage Temperature Range	–65ºC to 150ºC
Lead Temperature (Soldering 10 sec.)	260ºC

OPERATING CONDITIONS

Temperature Range	
ML4851CS-X	0ºC to 70ºC
ML4851ES-X	–20ºC to 70ºC
V_{IN} Operating Range	
ML4851CS-X	1.0V to V_{OUT} – 0.2V
ML4851ES-X	1.1V to V_{OUT} – 0.2V
Thermal Resistance (θ_{JA})	160ºC/W

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{IN} = Operating Voltage Range, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY							
I_{IN}	V_{IN} Current	V_{IN} = V_{OUT} – 0.2V			50	60	µA
$I_{OUT(Q)}$	V_{OUT} Quiescent Current				8	10	µA
I_L	V_L Quiescent Current					1	µA
REFERENCE							
V_{REF}	Output Voltage	0 < I_{REF} < –5µA		190	200	210	mV
PFM REGULATOR							
t_{ON}	Pulse Width			4.5	5	5.5	µs
OUTPUT VOLTAGE							
V_{OUT}	Output Voltage	t_{ON} = 0 at $V_{OUT(MAX)}$, 4.5µs ≤ t_{ON} ≤ 5.5µs at $V_{OUT(MIN)}$	-3 Suffix	3.2	3.3	3.4	V
			-5 Suffix	4.85	5.0	5.15	V
	Load Regulation	See Figure 1, -3 Suffix V_{IN} = 1.2V, I_{OUT} ≤ 10mA		3.2	3.3	3.4	V
		See Figure 1, -3 Suffix V_{IN} = 2.4V, I_{OUT} ≤ 65mA		3.2	3.3	3.4	V
		See Figure 1, -5 Suffix V_{IN} = 1.2V, I_{OUT} ≤ 18mA		4.85	5.0	5.15	V
		See Figure 1, -5 Suffix V_{IN} = 2.4V, I_{OUT} ≤ 85mA		4.85	5.0	5.15	V
	Undervoltage Lockout Threshold				0.85	0.95	V
$\overline{\text{RESET}}$ COMPARATOR							
	DETECT Threshold			194	200	206	mV
	DETECT Bias Current			–100		100	nA
	$\overline{\text{RESET}}$ Output High Voltage	I_{OH} = 100µA		V_{OUT} – 0.2			V
	$\overline{\text{RESET}}$ Output Low Voltage	I_{OL} = -100µA				0.2	V

Note 1: Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.

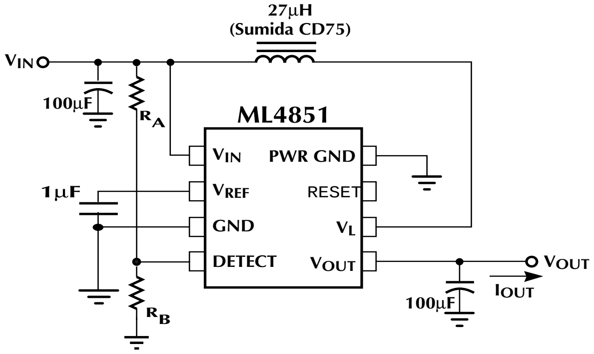


Figure 1. Application Test Circuit

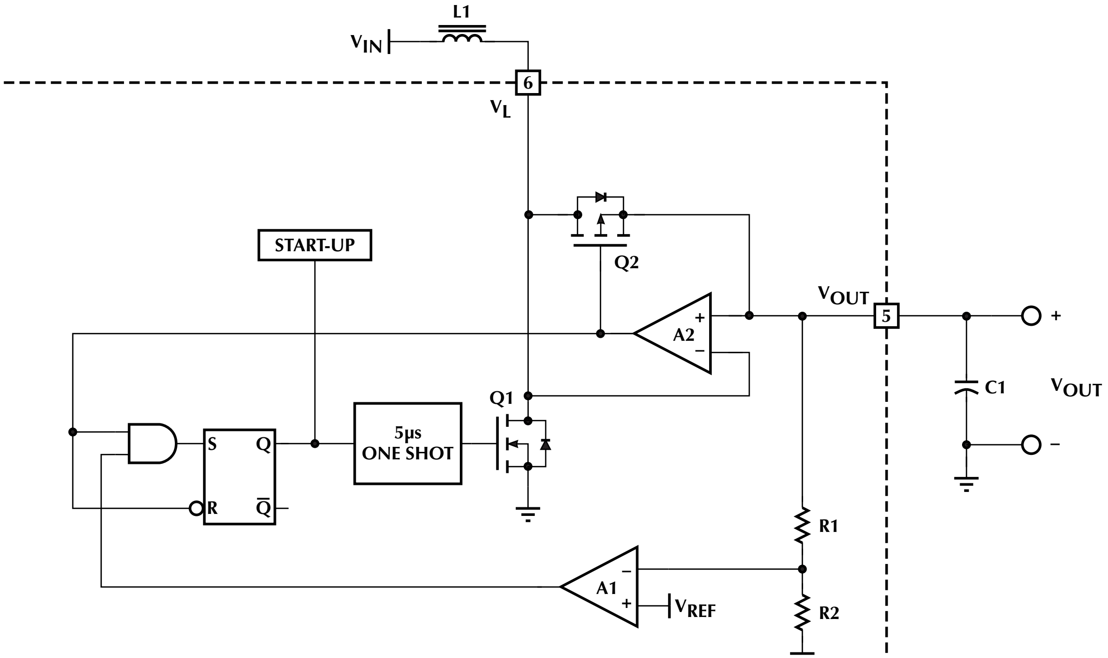


Figure 2. PFM Regulator Block Diagram

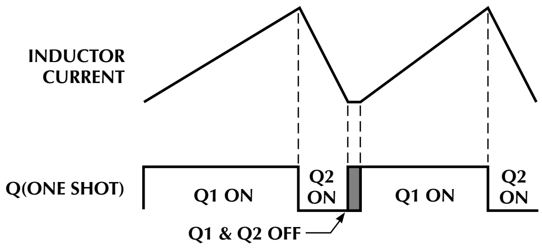


Figure 3. PFM Inductor Current Waveforms and Timing

FUNCTIONAL DESCRIPTION

The ML4851 combines Pulse Frequency Modulation (PFM) and synchronous rectification to create a boost converter that is both highly efficient and simple to use. A PFM regulator charges a single inductor for a fixed period of time and then completely discharges before another cycle begins, simplifying the design by eliminating the need for conventional current limiting circuitry. Synchronous rectification is accomplished by replacing an external Schottky diode with an on-chip PMOS device, reducing switching losses and external component count.

REGULATOR OPERATION

A block diagram of the boost converter is shown in Figure 2. The circuit remains idle when V_{OUT} is at or above the desired output voltage, drawing 50µA from V_{IN}, and 8µA from V_{OUT} through the feedback resistors R1 and R2. When V_{OUT} drops below the desired output level, the output of amplifier A1 goes high, signaling the regulator to deliver charge to the output. Since the output of amplifier A2 is normally high, the flip-flop captures the A1 set signal and creates a pulse at the gate of the NMOS transistor Q1. The NMOS transistor will charge the inductor L1 for 5µs, resulting in a peak current given by:

$$I_{L(PEAK)} = \frac{t_{ON} \times V_{IN}}{L1} = \frac{5\mu s \times V_{IN}}{L1} \tag{1}$$

For reliable operation, L1 should be chosen so that $I_{L(PEAK)}$ does not exceed 1A.

When the one-shot times out, the NMOS transistor releases the V_L pin, allowing the inductor to fly-back and momentarily charge the output through the body diode of PMOS transistor Q2. But, as the voltage across the PMOS transistor changes polarity, its gate will be driven low by the current sense amplifier A2, causing Q2 to short out its body diode. The inductor then discharges into the load through Q2. The output of A2 also serves to reset the flip-flop and one-shot in preparation for the next charging cycle. A2 releases the gate of Q2 when its current falls to zero. If V_{OUT} is still low, the flip-flop will immediately initiate another pulse. The output capacitor (C1) filters the inductor current, limiting output voltage ripple. Inductor current and one-shot waveforms are shown in Figure 3.

$\overline{\text{RESET}}$ COMPARATOR

An additional comparator is provided to detect low V_{IN}, or any other error condition that is important to the user. The inverting input of the comparator is internally connected to V_{REF}, while the non-inverting input is provided externally at the DETECT pin. The output of the comparator is the $\overline{\text{RESET}}$ pin, which swings from V_{OUT} to GND when an error is detected. (Refer to Block Diagram)

DESIGN CONSIDERATIONS

INDUCTOR

Selecting the proper inductor for a specific application usually involves a trade-off between efficiency and maximum output current. Choosing too high a value will keep the regulator from delivering the required output current under worst case conditions. Choosing too low a value causes efficiency to suffer. It is necessary to know the maximum required output current and the input voltage range to select the proper inductor value. The maximum inductor value can be estimated using the following formula:

$$L_{MAX} = \frac{{V_{IN(MIN)}}^2 \times t_{ON(MIN)} \times \eta}{2 \times V_{OUT} \times I_{OUT(MAX)}} \tag{2}$$

where η is the efficiency, typically between 0.8 and 0.9. Note that this is the value of inductance that just barely delivers the required output current under worst case conditions. A lower value may be required to cover inductor tolerance, the effect of lower peak inductor currents caused by resistive losses, and minimum dead time between pulses.

Another method of determining the appropriate inductor value is to make an estimate based on the typical performance curves given in Figures 4 and 5. Figure 4 shows maximum output current as a function of input voltage for several inductor values. These are typical performance curves and leave no margin for inductance and ON-time variations. To accommodate worst case conditions, it is necessary to derate these curves by at least 10% in addition to inductor tolerance.

For example, a two cell to 5V application requires 60mA of output current while using an inductor with 15% tolerance. The output current should be derated by 25% to 80mA to cover the combined inductor and ON-time tolerances. Assuming that 2V is the end of life voltage of a two cell input, Figure 4 shows that with a 2V input, the ML4851-5 delivers 80mA with an 18µH inductor.

Figure 5 shows efficiency under the conditions used to create Figure 4. It can be seen that efficiency is mostly independent of input voltage and is closely related to inductor value. This illustrates the need to keep the inductor value as high as possible to attain peak system efficiency. As the inductor value goes down to 10µH, the efficiency drops to around 75%. With 33µH, the efficiency exceeds 90% and there is little room for improvement. At values greater than 33µH, the operation of the synchronous rectifier becomes unreliable at low input voltages because the inductor current is so small that it is difficult for the control circuitry to detect. The data used to generate Figures 4 and 5 is provided in Table 1.

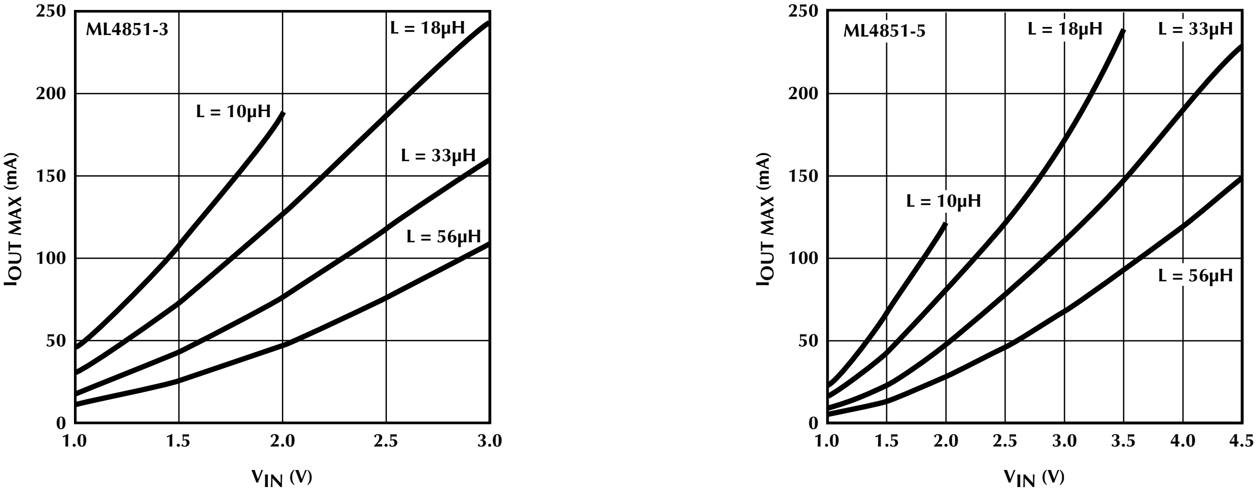


Figure 4. Output Current vs. Input Voltage

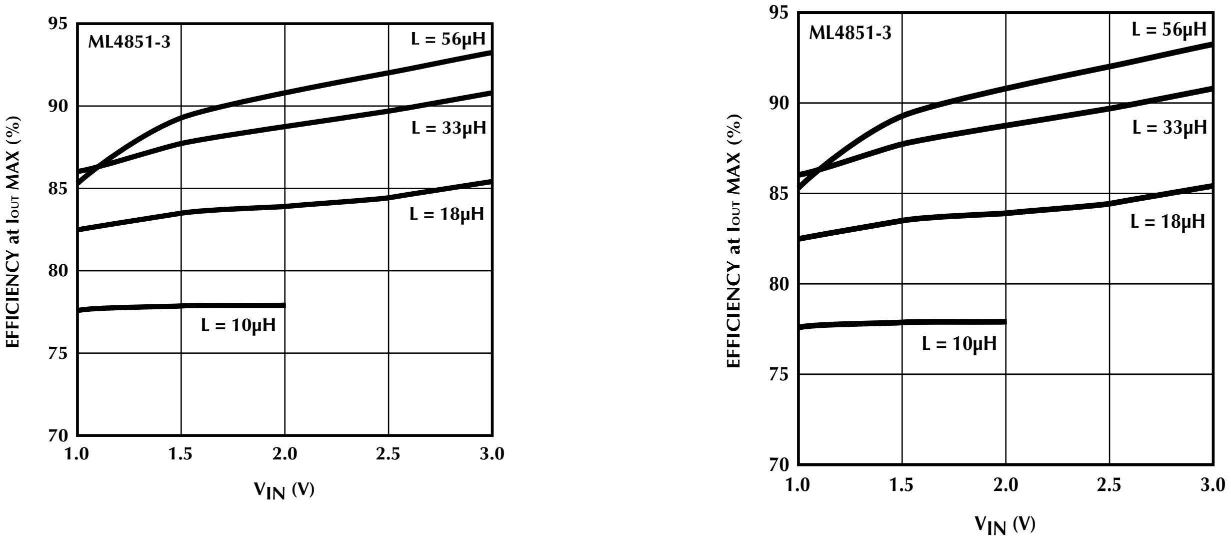


Figure 5. Typical Efficiency as a Function of V_{IN}

DESIGN CONSIDERATIONS (Continued)

After the appropriate inductor value is chosen, it is necessary to find the minimum inductor current rating required. Peak inductor current is determined from the following formula:

$$I_{L(PEAK)} = \frac{t_{ON(MAX)} \times V_{IN(MAX)}}{L_{MIN}} \qquad (3)$$

In the two cell application previously described, a maximum input voltage of 3V would give a peak current of 1A. When comparing various inductors, it is important to keep in mind that suppliers use different criteria to determine their ratings. Many use a conservative current level, where inductance has dropped to 90% of its normal level. In any case, it is a good idea to try inductors of various current ratings with the ML4851 to determine which inductor is the best choice. Check efficiency and maximum output current, and if a current probe is available, look at the inductor current to see if it looks like the waveform shown in Figure 3. For additional information, see Applications Note 29, “Choosing an Inductor for Your ML4861 Application.”

Suitable inductors can be purchased from the following suppliers:

Coilcraft	(847) 639-6400
Coiltronics	(561) 241-7876
Dale	(605) 665-9301
Sumida	(847) 956-0666
XFMRS, Inc.	(317) 834-1066

OUTPUT CAPACITOR

The choice of output capacitor is also important, as it controls the output ripple and optimizes the efficiency of the circuit. Output ripple is influenced by three capacitor parameters: capacitance, ESR, and ESL. The contribution due to capacitance can be determined by looking at the change in capacitor voltage required to store the energy delivered by the inductor in a single charge-discharge cycle, as determined by the following formula:

$$\Delta V_{OUT} = \frac{t_{ON}^{\,2} \times V_{IN}^{\,2}}{2 \times L \times C \times (V_{OUT} - V_{IN})} \qquad (4)$$

For a 2.4V input, and 5V output, a 18µH inductor, and a 47µF capacitor, the expected output ripple due to capacitor value is 33mV.

Capacitor Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL), also contribute to the output ripple due to the inductor discharge current waveform. Just after the NMOS transistor turns off, the output current ramps quickly to match the peak inductor current. This fast change in current through the output capacitor’s ESL causes a high frequency (5ns) spike that can be over 1V in magnitude. After the ESL spike settles, the output voltage still has a ripple component equal to the inductor discharge current times the ESR. This component will have a sawtooth shape and a peak value equal to the peak inductor current times the ESR. ESR also has a negative effect on efficiency by contributing I^2R losses during the discharge cycle.

An output capacitor with a capacitance of 100µF, an ESR of less than 0.1Ω, and an ESL of less than 5nH is a good general purpose choice. Tantalum capacitors which meet these requirements can be obtained from the following suppliers:

Matsuo	(207) 282-5111
Sprague	(207) 324-4140

If ESL spikes are causing output noise problems, an EMI filter can be added in series with the output.

INPUT CAPACITOR

Unless the input source is a very low impedance battery, it will be necessary to decouple the input with a capacitor with a value of between 47µF and 100µF. This provides the benefits of preventing input ripple from affecting the ML4851 control circuitry, and it also improves efficiency by reducing I^2R losses during the charge and discharge cycles of the inductor. Again, a low ESR capacitor (such as tantalum) is recommended.

REFERENCE CAPACITOR

Under some circumstances input ripple cannot be reduced effectively. This occurs primarily in applications where inductor currents are high, causing excess output ripple due to “pulse grouping”, where the charge-discharge pulses are not evenly spaced in time. In such cases it may be necessary to decouple the reference pin (V_{REF}) with a small 10nF to 100nF ceramic capacitor. This is particularly true if the ripple voltage at V_{IN} is greater than 100mV.

SETTING THE $\overline{\text{RESET}}$ THRESHOLD

To use the $\overline{\text{RESET}}$ comparator as an input voltage monitor, as shown in Figure 1, it is necessary to use an external resistor divider tied to the DETECT pin as shown in the block diagram. The resistor values R_A and R_B can be calculated using the following equation:

$$V_{IN(MIN)} = 0.2 \times \frac{(R_A + R_B)}{R_B} \qquad (5)$$

The value of R_B should be 100kΩ or less to minimize bias current errors. R_A is then found by rearranging the equation:

DESIGN CONSIDERATIONS (Continued)

$$R_A = R_B \times \left(\frac{V_{IN(MIN)}}{0.2} - 1 \right) \qquad (6)$$

LAYOUT

Good PC board layout practices will ensure the proper operation of the ML4851. Important layout considerations include:

- Use adequate ground and power traces or planes
- Keep components as close as possible to the ML4851
- Use short trace lengths from the inductor to the V_L pin and from the output capacitor to the V_{OUT} pin
- Use a single point ground for the ML4851 PWR GND pin and the input and output capacitors, and connect GND to PWR GND with a separate trace

A sample PC board layout is shown in Figure 6.

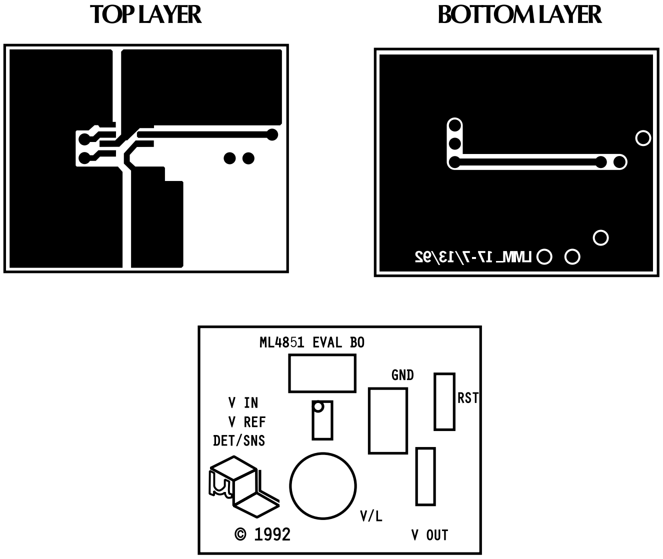


Figure 6. Sample PC Board Layout

ML4851-3

V_{IN}	I_{OUT} (mA)	EFFICIENCY PERCENTAGE
L = 10μH		
1.0	45.8	77.6
1.5	108.3	77.7
2.0	184.1	77.9
L = 18μH		
1.0	30.1	82.5
1.5	70.9	83.5
2.0	125.5	83.9
2.5	185.7	84.5
3.0	243.4	85.4
L = 33μH		
1.0	17.6	86.0
1.5	42.7	87.8
2.0	76.1	88.7
2.5	120.4	89.7
3.0	159.6	90.7
L = 56μH		
1.0	10.6	85.2
1.5	25.9	89.1
2.0	47.6	90.8
2.5	75.8	92.0
3.0	108.0	93.1

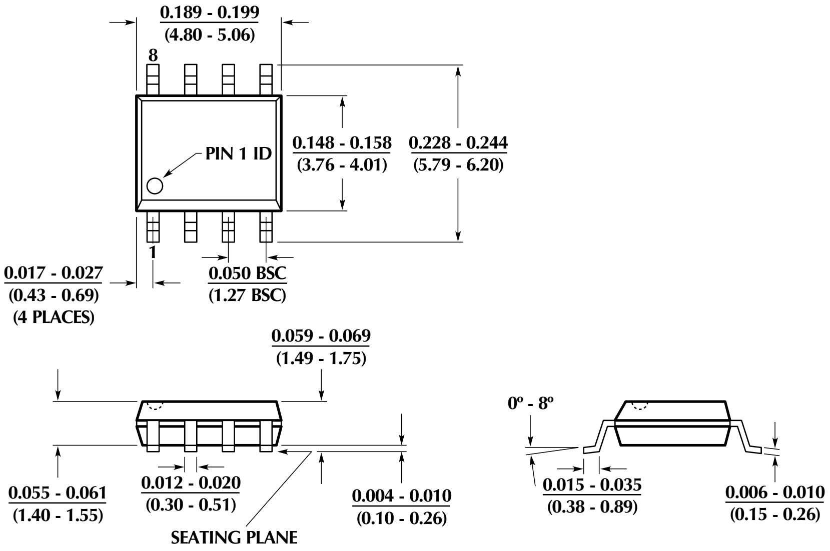
ML4851-5

V_{IN}	I_{OUT} (mA)	EFFICIENCY PERCENTAGE
L = 10μH		
1.0	24.2	78.3
1.5	68.0	79.9
2.0	123.1	80.3
L = 18μH		
1.0	15.7	82.3
1.5	43.3	84.8
2.0	80.4	85.7
2.5	125.3	86.2
3.0	169.9	86.5
3.5	236.9	87.0
L = 33μH		
1.0	9.1	83.5
1.5	24.8	87.0
2.0	47.4	88.6
2.5	74.5	89.5
3.0	106.9	90.3
3.5	147.5	90.8
4.0	190.0	91.4
4.5	227.8	92.1
L = 56μH		
1.0	5.5	80.1
1.5	13.9	85.9
2.0	28.5	88.9
2.5	45.7	90.3
3.0	67.1	91.4
3.5	92.5	92.3
4.0	122.1	92.6
4.5	149.6	93.8

Table 1. Maximum Output Current and Efficiency vs. V_{IN}

PHYSICAL DIMENSIONS inches (millimeters)

Package: S08
8-Pin SOIC



ORDERING INFORMATION

PART NUMBER	OUTPUT VOLTAGE	TEMPERATURE RANGE	PACKAGE
ML4851CS-3 ML4851CS-5	3.3V 5.0V	0ºC to 70ºC 0ºC to 70ºC	8-Pin SOIC (S08) 8-Pin SOIC (S08)
ML4851ES-3 ML4851ES-5	3.3V 5.0V	–20ºC to 70ºC –20ºC to 70ºC	8-Pin SOIC (S08) 8-Pin SOIC (S08)
ML4851IS-3 (obsolete) **ML4851IS-5 (obsolete)**	**3.3V** **5.0V**	**–40ºC to 85ºC** **–40ºC to 85ºC**	**8-Pin SOIC (S08)** **8-Pin SOIC (S08)**

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