Rochester Electronics

Datasheet

PART NUMBER

54L96DMB-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

Rochester Electronics®

Datasheet

54L96

5-Bit Shift Registers

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

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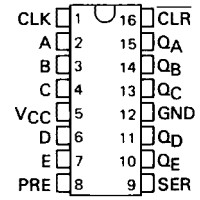
FOR REFERENCE ONLY

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

TYPE	TYPICAL PROPAGATION DELAY TIME	TYPICAL POWER DISSIPATION
'96	25 ns	240 mW
'L96	50 ns	120 mW
'LS96	25 ns	60 mW

SN5496, SN54LS96 . . . J OR W PACKAGE
SN54L96 . . . J PACKAGE
SN7496 . . . J OR N PACKAGE
SN74LS96 . . . D, J OR N PACKAGE
(TOP VIEW)



For chip carrier information on SN54LS96 and SN74LS96, contact the factory.

description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

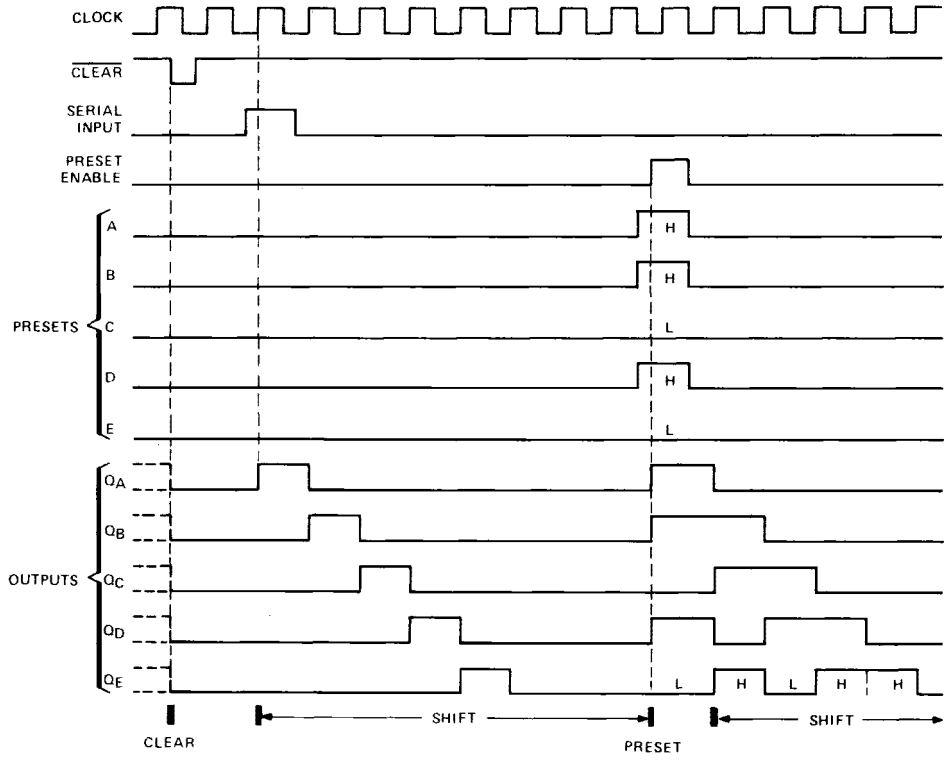
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

FUNCTION TABLE

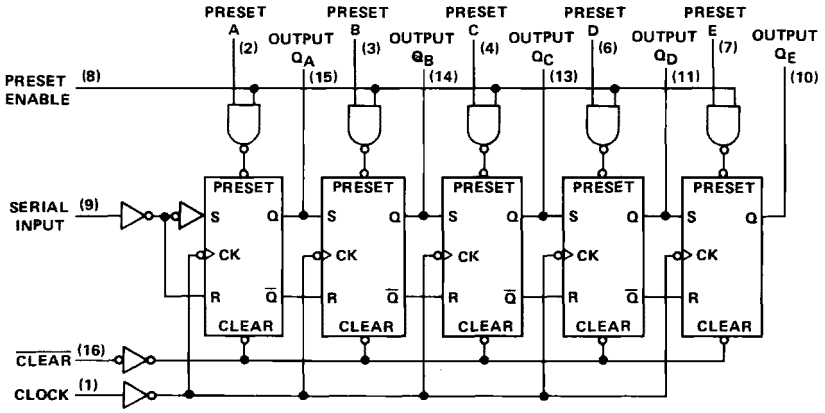
INPUTS									OUTPUTS				
$\overline{\text{CLEAR}}$	PRESET ENABLE	PRESET A	B	C	D	E	CLOCK	SERIAL	Q_A	Q_B	Q_C	Q_D	Q_E
L	L	X	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	H	H	L	H	L	H	L	X	H	Q_{B0}	H	Q_{D0}	H
H	L	X	X	X	X	X	L	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}
H	L	X	X	X	X	X	↑	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}
H	L	X	X	X	X	X	↑	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc = the level of Q_A, Q_B, etc, respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc = the level of Q_A, Q_B, etc, respectively before the most-recent ↑ transition of the clock.

typical clear, shift, preset, and shift sequences



logic diagram



Pin numbers shown on logic notation are for D, J or N packages.

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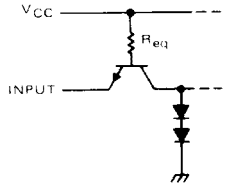
schematics of inputs and outputs

'96

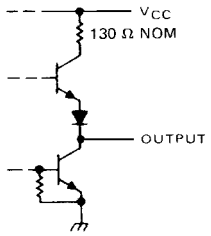
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
Preset enable	800 Ω
All others	4 kΩ

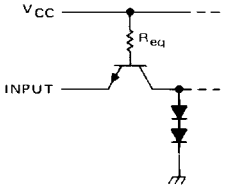
'96

TYPICAL OF ALL OUTPUTS



'L96

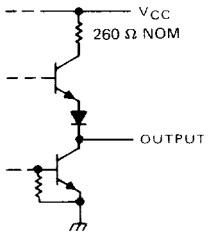
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
Preset enable	1.6 kΩ
All others	8 kΩ

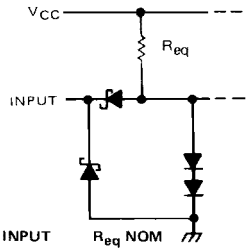
'L96

TYPICAL OF ALL OUTPUTS



'LS96

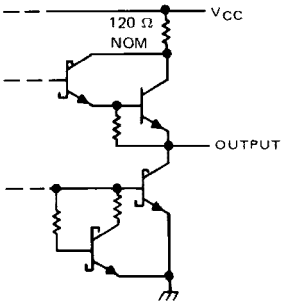
EQUIVALENT OF EACH INPUT



INPUT	R_{eq} NOM
Serial	25 kΩ
Clock, Clear	17 kΩ
Preset enable	3.4 kΩ

'LS96

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 2): '96, 'L96 . . . . . 5.5 V
'LS96 . . . . . 7 V
Operating free-air temperature: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_{w(clock)}$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{su} (see Figure 1)	30			30			ns
Serial input hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN5496			SN7496			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	any input except preset enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
		preset enable				200			200	
I_{IL}	Low-level input current	any input except preset enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
		preset enable				−8			−8	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 3		48	68		48	79	mA

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 400 Ω, See Figure 1		25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				55	ns

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recommended operating conditions

		SN54L96			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			−0.2	mA
I_{OL}	Low-level output current			8	mA
f_{clock}	Clock frequency	0		5	MHz
t_w	Width of clock, preset, or clear input	100			ns
t_{su}	Serial input setup time (See Figure 1)	100			ns
t_h	Serial input hold time (See Figure 1)	0			ns
T_A	Operating free-air temperature	−55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54L96			UNIT
			MIN	TYP‡	MAX	
V_{OH}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −0.2 mA	2.4	3.2		V
V_{OL}		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 8 mA		0.2	0.4	V
I_I		V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	Any input except preset enable	V_{CC} = MAX, V_I = 2.4 V			20	μA
	Preset enable				0.1	mA
I_{IL}	Any input except preset enable	V_{CC} = MAX, V_I = 0.4 V			−0.8	mA
	Preset enable				−4	
I_{OS}§		V_{CC} = MAX	−10		−29	mA
I_{CC}		V_{CC} = MAX, See Note 3		24	34	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Clock	Any	R_L = 800 Ω, C_L = 15 pF, See Figure 1		50	80	ns
t_{PHL}					50	80	ns
t_{PLH}	Preset or Preset enable				56	70	ns
t_{PHL}	Clear					110	ns

recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock input pulse, $t_{w(clock)}$	20			20			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{setup} (see Figure 1)	30			30			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS96			SN74LS96			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH} High-level input voltage				2			2			V
V_{IL} Low-level input voltage						0.7			0.8	V
V_{IK} Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max, I_{OH} = −400 μA		2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I Input current at maximum input voltage	Preset enable	V_{CC} = MAX, V_I = 7 V				0.5			0.5	mA
	All others					0.1			0.1	
I_{IH} High-level input current	Preset enable	V_{CC} = MAX, V_I = 2.7 V				100			100	μA
	All others					20			20	
I_{IL} Low-level input current	Preset enable	V_{CC} = MAX, V_I = 0.4 V				−2			−2	mA
	All others					−0.4			−0.4	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 3			12	20		12	20	mA

‡For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock	C_L = 15 pF, R_L = 2 kΩ, See Figure 1		25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear				55	ns

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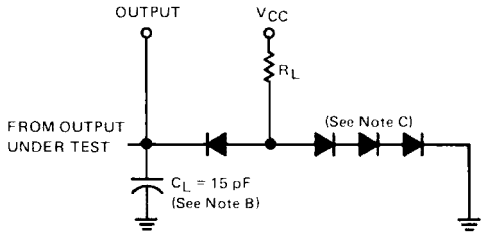
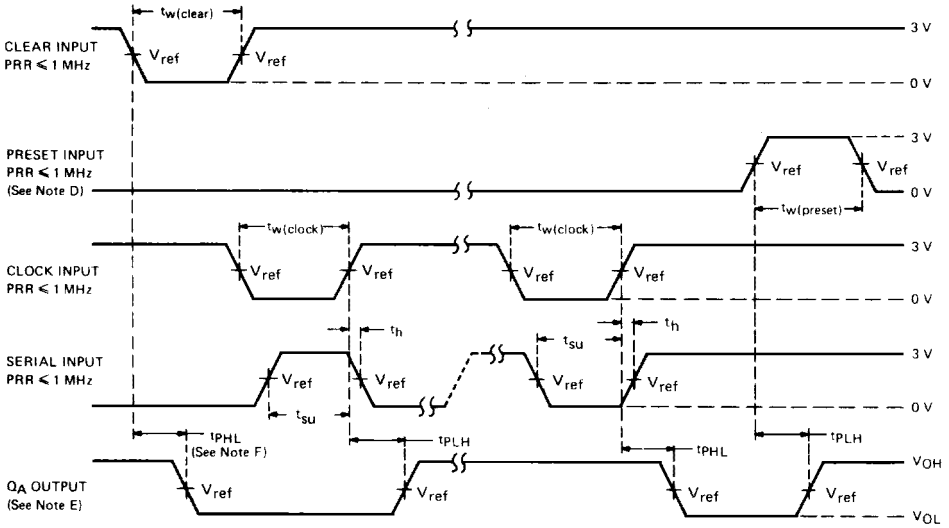
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by pulse generators having the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$; for '96 and 'L96, $t_r \leq 10$ ns, $t_f \leq 10$ ns, and for 'LS96 $t_r = 15$ ns, $t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Preset may be tested by applying a high-level voltage to the individual preset inputs and pulsing the preset enable or by applying a high-level voltage to the preset enable and pulsing the individual preset inputs.
E. Q_A output is illustrated. Relationship of serial input to other Q outputs is illustrated in the typical shift sequence.
F. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.
G. For '96 and 'L96, $V_{ref} = 1.5$ V; for 'LS96 $V_{ref} = 1.3$ V.

FIGURE 1–SWITCHING TIMES