

54H183, SN54184, 74184, SN54185, 74185

BCD-to-Binary and Binary-to-BCD Converters

These monolithic converters are derived from the custom MSI 256-bit read-only memories. Emilter connections are made to provide direct read-out of converted codes at outputs YB through YI as shown in the function tables. These converters demonstrate the versatHity of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits {LSB} of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer (OCM).

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54184, SN54185A, SN74184, SN74185A BCD-TO-BINARY AND BINARY-TO-BCD CONVERTERS

FEBRUARY 1971 - REVISED DECEMBER 1972

SN54184, SN74184 BCD-TO-BINARY CONVERTERS SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

SN54184, SN54185A . . . J OR W PACKA GE SN74184, SN74185A . . . J OR N PACKA GE (TOP VIEW)

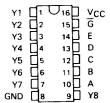


TABLE I SN54184, SN74184 PACKAGE COUNT AND DELAY TIMES FOR BCD-TO-BINARY CONVERSION

INPUT	PACKAGES	TOTAL DELAY TIMES (no						
(DECADES)	REQUIRED	TYP	MAX					
2	2	56	80					
3	6	140	200					
4	11	196	280					
5	19	280	400					
6	28	364	520					

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the '185A and all "don't care" conditions of the '184 are programmed high. The outputs are of the open-collector type.

The SN54184 and SN54185A are characterized for operation over the full military temperature range of -55° C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

SN54184 and SN74184 BCD-to-binary converters

description

The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

These monolithic converters are derived from the

custom MSI 256-bit read-only memories SN5488 and

SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8

through Y1 as shown in the function tables. These

converters demonstrate the versatility of a read-only

memory in that an unlimited number of reference

tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

- a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.
- Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table (following page, right) when the devices are connected as shown above the function table.

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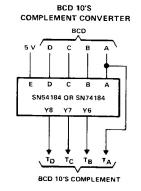


BCD			INP	urs				ΟL	JTPU	TS		
WORDS	(See Note A)						(See Note B)					
	E	D	С	8	Α	G	Y5	Y4	Υ3	Y2	Y1	
0.1	L	L	L	L	L	Ł	L	L	L	L	L	
23	Ł	Ł	L	L,	H	L	L	L	L	L	н	
4.5	Ł	L	L	н	L	L	L	L	L	н	L	
6.7	L	L	L	Н	Н	L	L	L	L	H	н	
8-9	L	L	Н	L	L	L	L	L	Н	L	L	
10 11	L	H	L	L	L	L	L	L	н	L	Н	
12.13	L	H	L	L	H	ι	L	L	н	н	L	
14.15	L	Н	L	н	Ł	L	L	L	Н	Н	н	
16.17	L	H	L	Н	Н	L	L	н	L	L	L	
18 19	L	Н	H	L	L	L	L	Н	L	L	H	
20-21	+1	L.	L	L	L	L	L	Н	L	Н	L	
22 23	н	L	L	L	Н	L	L	Н	L	Н	н	
24 25	Н	L	L	H	L	L	L	Н	Н	L	Ł	
26 27	Н	L	L	Н	н	L	L	Н	Н	L	Н	
28 29	Н	L	H	L	L	L	Ł	н	Н	н	L	
30 31	Н	н	L	L	L	L	L	Н	Н	Н	н	
32 33	Н	11	L	L	Н	ι	н	ŧ	L	L	L	
34 35	Н	н	ŧ	Н	L	L	н	L	L	L	Н	
36.37	н	11	L	Н	H	L	н	L	L	Н	L	
38 39	H	н	н	L	L	L	н	ι	L	н	++	
ANY	Х	×	х	×	×	Н	н	Н	н	н	Н	

H = high level, L = low level, X = irrelevant

- NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.
 - B. Outputs Y6, Y7, and Y8 are not used for BCD-tobinary conversion.

SN54184 OR SN74184 **BCD 9'S COMPLEMENT**



FUNCTION TABLE BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD			INP	UTS			Οι	JTPL	JTS
WORD	(See Note C)							Not	e D)
	Ε†	o	С	В	Α	Ĝ	Y8	Y 7	¥6
0	Ł	L	L	L	L	L	Н	L	н
1	L	Ł	L	L	Н	L	н	L	L
2	,L	L	L.	н	L	L	L	Н	н
3	L	L	L	Н	Н	L	L	Н	L
4	L	Ł	Н	L	L	L	L	н	Н
5	L	L	H	L	Н	L	L	н	L
6	L	Ł	H	Н	L	L	L	L	н
7	L	L	Н	Н	Н	L	L	Ł	L
8	Ł	Н	L	Ł	L	L	L	L	н
9	Ł	Н	L	L	Н	L	L	L	L
0	Н	L	L	L	L	L	L	L	L
1	н	L	L	L	Н	L,	н	L	L
2	н	L	L	Н	L	L	н	L	L
3	Н	L	L	Н	Н	L	L	Н	Н
4	14	L	Н	L	L	L	L	Н	Н
5	н	L	Н	٤	H	L.	L	Н	L
6	H	L	Н	Н	L	L	L	Н	L
7	н	L	Н	Н	H	L	L	L	Н
8	н	Н	L	L	L	L	L	L	Н
9	Н	Н	L	L	н	L	L	L	L
ANY	х	Х	X	Х	х	н	н	н	н

H = high level, L = low level, X = irrelevant

- NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.
 - D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

 $\ensuremath{^{\uparrow}}\xspace$ When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

- Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
- Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
- Repeat step b until the least-significant binary bit is in the least-significant BCD location.

TABLE II SN54185A, SN74185A PACKAGE COUNT AND DELAY TIMES FOR BINARY-TO-BCD CONVERSION

INPUT	PACKAGES	TOTAL DEL	AY TIME (ns)
(BITS)	REQUIRED	TYP	MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-BIT CONVERTER 6-BIT BINARY INPUT E D C B A SN74185A Y5 Y4 Y3 Y2 Y1 B A D C B A MSD LSD 6-BIT BCD OUTPUT

FUNCTION TABLE

		INPUTS					OUTPUTS								
BINARY	BIF	NAR	Y SI	LEC	СТ	ENABLE									
WORDS	E	D	С	В	A	Ğ	Y8	¥7	Y6	Y5	Y4	¥3	¥2	Y1	
0 - 1	L	L	L	L	L	L	н	н	L	Ł	L	L	L	L	
2 3	L	L	L	L	н	L	н	н	L	Ł	L	L	L	н	
4 - 5	L	L	L	н	Ł	L	н	н	Ł	L	L	L	н	L	
6 7	L	ι	Ł	н	н	L	н	н	L	L	L	ι	н	н	
8 9	L	Ł	н	L	L	L	н	Н	L	L	L	н	L	ι	
10 - 11	L	L	н	L	н	L	н	Н	L	L	н	L	L	L	
12 - 13	L	L	н	н	L	L	н	н	L	L	н	L	L	н	
14 - 15	L	L	Н	н	н	L	н	н	L	L	н	L	н	L.	
16 - 17	L	н	L	L	L	L.	н	н	L	L	Н	L	Н	Н	
18 19	Ł	н	L	L	н	L	н	н	L	L	Н	Н	L	L	
20 21	L	н	L	H	L	L	н	Н	L	н	L	L	L	L	
22 - 23	L	н	L	н	Н	L	н	н	L	н	L	L	L.	н	
24 25	L	н	Н	L.	L	L	н	н	L	н	L	L	Н	L	
26 - 27	ı	H	Н	L	Н	L	н	н	L	н	L	Ł	н	н	
28 29	L	н	Н	Н	Ł	L.	H	Н	L	Н	L	н	L	Ł	
30 31	L	н	н	н	н	L	н	Н	L	н	н	L,	Ł	L.	
32 - 33	H	Ļ	L	L	L	L	н	Н	L	н	н	L	L.	Н	
34 35	н	L	L	t	н	L	н	н	L	Н	Н	L	н	L	
36 37	н	L	L	н	L	L	н	H	L	Н	н	ι	Н	Н	
38 39	н	L	Ĺ	Н	н	L	н	н	L	н	Н	н	L	L	
40 - 41	н	L	н	L	L	L	н	н	н	L	L	L	L	L	
42 43	н	L	н	L	н	L	н	н	н	L	L	Ł	L	Н	
44 45	Н	L	н	н	L	Ł	н	н	Н	L	L	L	н	L	
46 47	н	L	н	н	н	l.	н	н	н	L	L	L	н	н	
48 - 49	Н	н	L	L	L	L	н	Н	н	L	L	н	L	L	
50 - 51	н	н	L	L	н	L	Н	н	Н	L	++	L	L	L	
52 - 53	н	н	L	н	L	L	н	Н	н	L	н	L	L	Н	
54 55	н	н	L	н	н	L L	Н	. н	н	Ļ	Н	L	H	L.	
56 57	Н	н	н	L	L	L	н	н	н	L	н	L	Н	Н	
58 59	н	н	н	L	н	L	н	н	H	L	Н	Н	L	Ł	
60 61	н	н	н	н	L	L	н	н	H	н	ι	L	L	L	
62 - 63	н	н	н	н	н	L	Н	Н	н	Н	L	L	, L	Н	
ALL	×	×	х	ж	×	н	н	н	н	н	Н	н	H	Н	

H = high level, L = low level, X = irrelevant

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NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54	SN54184, SN54185A SN74184, SN74185A					
	MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, IOL			12			12	mA
Operating free-air temperature, TA	-55		125	0		70	"C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

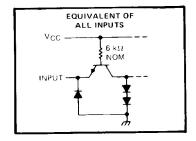
	PARAMETER	TEST CONDITIONS†	MIN	TYP	мах	UNIT
ViH	High-level input voltage		2			V
VIL	Low-level input voltage				0.8	٧
VIK	Input clamp voltage	V _{CC} = MIN, I ₁ = -12 mA			-1.5	ν
lон	High-level output current	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, V _{OH} = 5.5 V			100	μА
VOL	Low-level output voltage	$V_{CC} = MIN$, $V_{IH} = 2 V$, $V_{IL} = 0.8 V$, $I_{OL} = 12 \text{ mA}$			0.4	٧
Ч.	Input current at maximum input voltage	V _{CC} = MAX, V _I = 5.5 V			1	mA
ΊΗ	High-level input current	V _{CC} = MAX, V ₁ = 2.4 V			40	μΑ
1 ₁ L	Low-level input current	V _{CC} = MAX, V _I = 0.4 V			-1	mA
ICCH		V _{CC} « MAX		50 62	99	mA

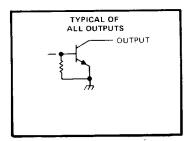
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type. ‡ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25 \text{ °C}$.

switching characteristics, VCC = 5 V, TA = 25°C

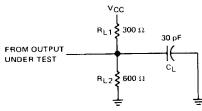
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
tplh Propagation delay time, low-to-high-level output from enable \overline{G}	C _L = 30 pF,		19	30	ns
tPHL Propagation delay time, high-to-low-level output from enable G	$R_{L1} = 300 \Omega$,		22	35	ns
tptH Propagation delay time, low-to-high-level output from binary select	R ₁₂ = 600 \$\$,		27	40	ns
tPHL Propagation delay time, high-to-low-level output from binary select	See Figure 1 and Note 2		23	40	ns

schematics of inputs and outputs





PARAMETER MEASUREMENT INFORMATION



C_L includes probe and jig capacitance.

LOAD CIRCUIT FIGURE 1

NOTE 2: See General Information Section for load circuits and voltage waveforms.

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TYPICAL APPLICATION DATA SN54184, SN74184

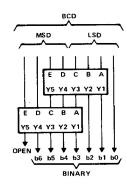


FIGURE 2-BCD-TO-BINARY CONVERTER FOR TWO BCD DECADES

MSD-most significant decade

LSD—least significant decade Each rectangle represents an SN54184 or SN74184

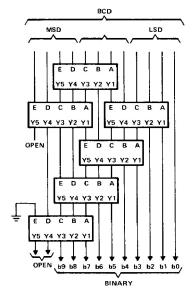


FIGURE 3-BCD-TO-BINARY CONVERTER FOR THREE BCD DECADES

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TYPICAL APPLICATION DATA SN54184, SN74184

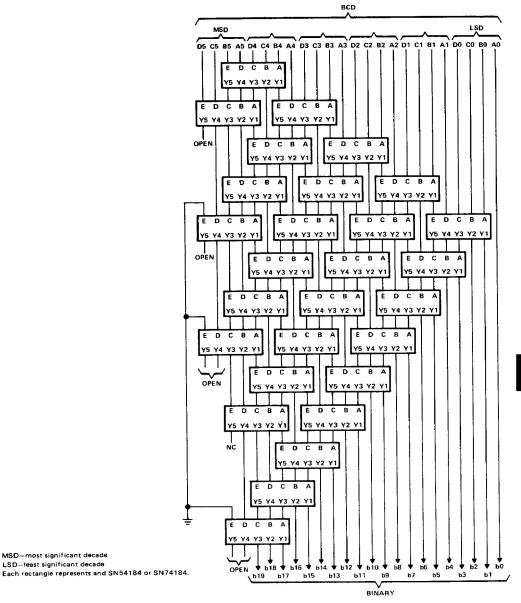


FIGURE 4-BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES



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MSD-most significant decade LSD-least significant decade

FIGURE 5-6-BIT BINARY-TO-BCD CONVERTER

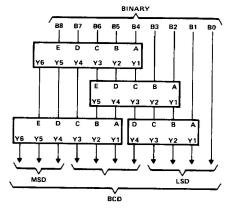


FIGURE 7-9-BIT BINARY-TO-BCD CONVERTER

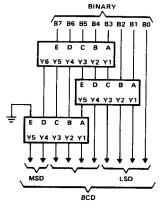


FIGURE 6-8-BIT BINARY-TO-BCD CONVERTER

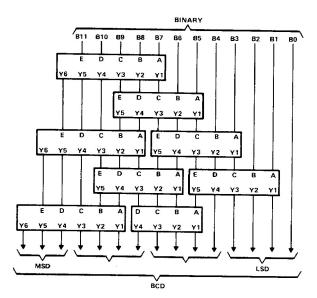


FIGURE 8-12-BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

MSD-Most significant decade

NOTES: A. Each rectangle represents an SN54185A or an SN74185A.

B. All unused E inputs are grounded.

INSTRUMENTS

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FIGURE 9-16 BIT BINARY-TO-BCD CONVERTER (SEE NOTE B)

MSD-most significant decade

LSD—least significant decade

NOTES: A. Each rectangle represents an SN54185A or SN74185A.

B. All unused E inputs are grounded.