T-46-13-29

Microchip

27C256

256K (32K x 8) CMOS UV Erasable PROM

FEATURES

- High speed performance
  —150ns maximum access time
- CMOS Technology for low power consumption
  —20mA Active current
  —100μA Standby current
- OTP (one-time-programming) available
- Auto-insertion-compatible plastic packages
- Auto ID™ aids automated programming
- Separate chip enable and output enable controls
- Two programming algorithms allow improved programming times
  —Fast programming
  —Rapid-pulse programming
- Organized 32K x 8: JEDEC standard pinouts
  —28-pin Dual-in-line package
  —32-pin Chip carrier (leadless or plastic)
- Available for extended temperature ranges:
  —Commercial: 0° C to 70° C
  —Industrial: -40° C to 85° C
  —Military (B): -55° C to 125° C

DESCRIPTION

The Microchip Technology Inc 27C256 is a CMOS 256K bit ultraviolet light Erasable (electrically) Programmable Read Only Memory. The device is organized as 32K words by 8 bits (32K bytes). Accessing individual bytes from an address transition or from power-up (chip enable pin going low) is accomplished in less than 150ns. This very high speed device allows the most sophisticated microprocessors to run at full speed without the need for WAIT states. CMOS design and processing enables this part to be used in systems where reduced power consumption and reliability are requirements.

A complete family of packages is offered to provide the most flexibility in applications. One Time Programming (OTP) is available for low cost (plastic) applications.

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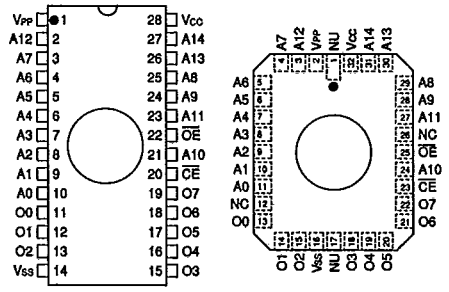
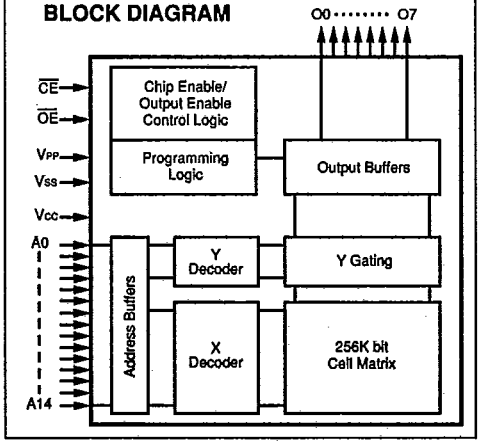
PIN CONFIGURATION
Top View



●Pin 1 Indicator on PLCC on top of package

BLOCK DIAGRAM



** See 27C256 Military Data sheet DS60013

PIN FUNCTION TABLE	
Name	**Function**
$\overline{A0}$ - A14	Address Inputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
VPP	Programming Voltage
O0 - O7	Data Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection; No Internal Connection
NU	Not Used; No External Connection is Allowed

ELECTRICAL CHARACTERISTICS
Maximum Ratings*

VCC and input voltages w.r.t. VSS .....-0.6V to +7.25V
VPP voltage w.r.t. VSS during programming .....-0.6V to +14.0V
Voltage on A9 w.r.t. VSS .....-0.6V to +13.5V
Output voltage w.r.t. VSS .....-0.6V to VCC + 1.0V
Storage temperature .....-65° C to 150° C
Ambient temp. with power applied .....-65° C to 125° C

*Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

READ OPERATION
DC Characteristics

VCC = +5V ±10%
Commercial: Tamb= 0° C to 70° C
Industrial: Tamb= -40° C to 85° C

Parameter	Part*	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	all	Logic "1" Logic "0"	VIH VIL	2.0 -0.5	VCC+1 0.8	V V	
Input Leakage	all		ILI	-10	10	µA	VIN= 0 to VCC
Output Voltages	all	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH= -400µA IOL= 2.1mA
Output Leakage	all		ILO	-10	10	µA	VOUT= 0V to VCC
Input Capacitance	all		CIN		6	pF	VIN= 0V; Tamb = 25° C; f = 1MHz
Output Capacitance	all		COUT		12	pF	VOUT= 0V;Tamb= 25° C; f = 1MHz
Power Suppy Current, Active	S X	TTL input TTL input	ICC1 ICC2		20 25	mA mA	VCC = 5.5V; VPP = VCC; f = 1MHz; $\overline{OE}$ = $\overline{CE}$ = VIL; Iout = 0mA; VIL= -0.1 to 0.8 V; VIH= 2.0 to VCC; Note 1
Power Supply Current, Standby	S X all	TTL input TTL input CMOS input	ICC(S)		2 3 100	mA mA µA	 $\overline{CE}$ = VCC ±0.2V
IPP Read Current	all	Read Mode	IPP		100	µA	VPP = 5.5V
VPP Read Voltage	all	Read Mode	VPP	VCC-0.7	VCC	V	Note 2

* Parts: S = Standard Power; X = Industrial Temp Range;
Notes: (1) AC Power component above 1MHz: 5mA up to maximum frequency.
(2) VCC must be applied before VPP, and be removed simultaneously or after VPP.

READ OPERATION
AC Characteristics

AC Testing Waveform: V_{IH} = 2.4V and V_{IL} = 0.45V; V_{OH} = 2.0V V_{OL} =0.8V
Output Load: 1 TTL Load + 100pF
Input Rise and Fall Times: 10nsec
Ambient Temperature: Commercial: Tamb = 0° C to 70° C
Industrial: Tamb = -40° C to 85° C

Parameter	Sym	27C256-15		27C256-17		27C256-20		27C256-25		Units	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max		
Address to Output Delay	tACC		150		170		200		250	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to Output Delay	tCE		150		170		200		250	ns	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to Output Delay	tOE		60		70		75		100	ns	$\overline{CE}$ = V_{IL}
$\overline{CE}$ or $\overline{OE}$ to O/P High Impedance	tOFF	0	50	0	50	0	55	0	60	ns	
Output Hold from Address $\overline{CE}$ or $\overline{OE}$, whichever goes first	tOH	0		0		0		0		ns	

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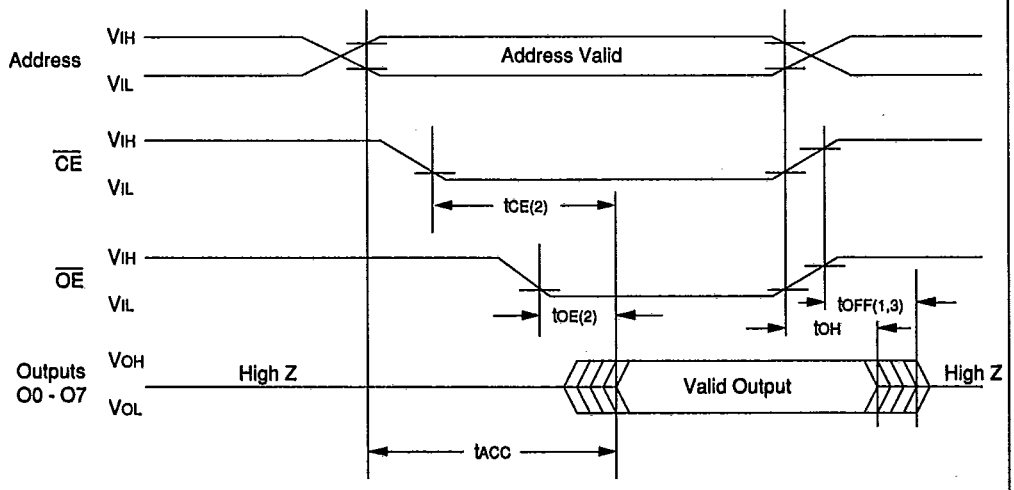
READ WAVEFORMS



Notes: (1) tOFF is specified for $\overline{OE}$ or $\overline{CE}$, whichever occurs first
(2) $\overline{OE}$ may be delayed up to tCE - tOE after the falling edge of $\overline{CE}$ without impact on tCE
(3) This parameter is sampled and is not 100% tested.

PROGRAMMING
DC Characteristics

Ambient Temperature: Tamb = 25° C ±5° C
For VPP and Vcc Voltages refer to Programming Algorithms

Parameter	Status	Symbol	Min	Max	Units	Conditions
Input Voltages	Logic "1" Logic "0"	VIH VIL	2.0 -0.1	Vcc+1 0.8	V V	
Input Leakage		ILI	-10	10	µA	VIN = 0V to Vcc
Output Voltages	Logic "1" Logic "0"	VOH VOL	2.4	 0.45	V V	IOH = -400µA IOL = 2.1mA
Vcc Current, program & verify		ICC2		20	mA	Note 1
VPP Current, program		IPP2		25	mA	Note 1
A9 Product Identification		VH	11.5	12.5	V	

Note: (1) Vcc must be applied simultaneously or before VPP and removed simultaneously or after VPP

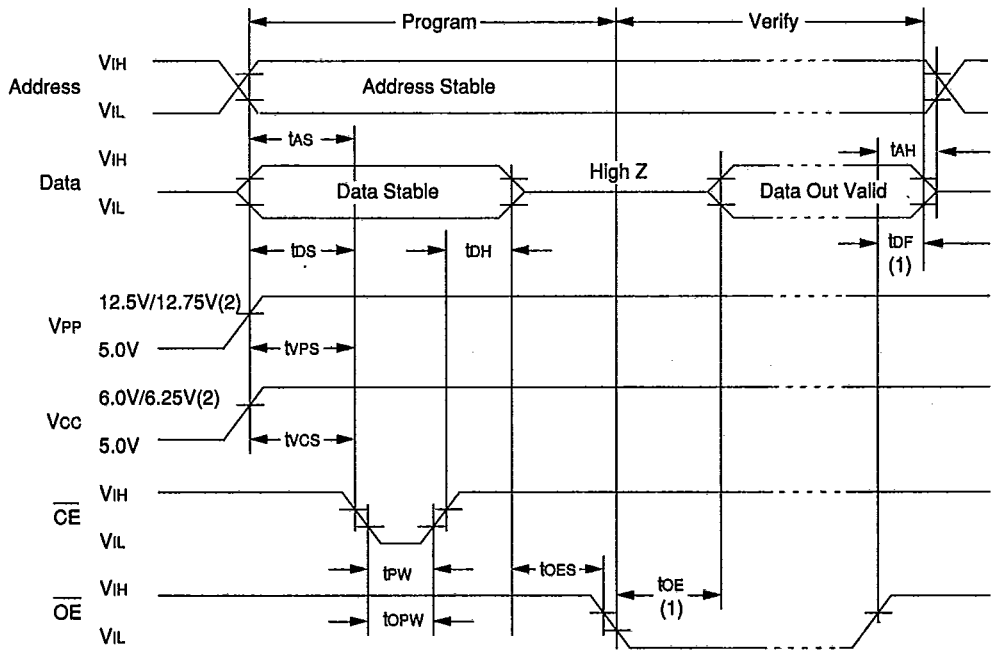
PROGRAMMING
AC Characteristics
for Program, Program Verify and Program Inhibit Modes

AC Testing Waveform: VIH = 2.4 V and VIL = 0.45 V; VOH = 2.0 V; VOL = 0.8 V
Output Load: 1 TTL Load + 100 pF
Ambient Temperature: Tamb = 25° C ±5° C
For VPP and Vcc Voltages, refer to Programming Algorithms

Parameter	Symbol	Min	Max	Units	Remarks
Address Set-Up Time	tAS	2		µs	
Data Set-Up Time	tDS	2		µs	
Data Hold Time	tDH	2		µs	
Address Hold Time	tAH	0		µs	
Float Delay (3)	tDF	0	130	ns	
Vcc Set-Up Time	tVCS	2		µs	
Program Pulse Width (1)	tPW	0.95	1.05	ms	1ms typical
Program Pulse Width (1)	tPW	95	105	µs	100µs typical
$\overline{CE}$ Set-Up Time	tCES	2		µs	
$\overline{OE}$ Set-Up Time	tOES	2		µs	
VPP Set-Up Time	tVPS	2		µs	
Overprogram Pulse Width (2)	tOPW	2.85	78.75	ms	
Data Valid from $\overline{OE}$	tOE		100	ns	

Notes: (1) For rapid-pulse programming algorithm, initial programming width tolerance is 100µsec ±5%. For fast programming algorithm, initial program pulse width tolerance is 1msec ± 5%.
(2) For fast programming algorithm, the length of the overprogram pulse may vary from 2.85 to 78.75msec as a function of the iteration counter value.
(3) This parameter is only sampled and not 100% tested. Output float is defined as the point where data is no longer driven (see timing diagram).

PROGRAMMING
Waveforms



Notes: (1) tDF and tOE are characteristics of the device but must be accommodated by the programmer
(2) VCC = 6.0 V ±0.25 V, VPP = VH = 12.5 V ±0.50 V for fast programming algorithm
VCC = 6.25 V ±0.25 V, VPP = VH = 12.75 V ±0.25 V for rapid pulse programming algorithm

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MODES

Operation Mode	$\overline{CE}$	$\overline{OE}$	VPP	A9	O0 - O7
Read	VIL	VIL	VCC	X	DOUT
Program	VIL	VIH	VH	X	DIN
Program Verify	VIH	VIL	VH	X	DOUT
Program Inhibit	VIH	VIH	VH	X	High Z
Standby	VIH	X	VCC	X	High Z
Output Disable	VIL	VIH	VCC	X	High Z
Identity	VIL	VIL	VCC	VH	Identity Code

X = Don't Care

Read Mode

(See Timing Diagrams and AC Characteristics)

Read Mode is accessed when

a) the $\overline{CE}$ pin is low to power up (enable) the chip

b) the $\overline{OE}$ pin is low to gate the data to the output pins.

For Read operations, if the addresses are stable, the address access time (tACC) is equal to the delay from $\overline{CE}$ to output (tCE). Data is transferred to the output after a delay from the falling edge of $\overline{OE}$ (tOE).

Standby Mode

The standby mode is defined when the $\overline{CE}$ pin is high (V_{IH}) and a program mode is not defined.

When these condition are met, the supply current will drop from 20mA to 100µA.

Output Enable

This feature eliminates bus contention in multiple bus microprocessor systems and the outputs go to a high impedance when the following condition is true:

- The $\overline{OE}$ pin is high and a program is not defined.

Erase Mode

Windowed products offer the ability to erase the memory array. The memory matrix is erased to the all 1's state as a result of being exposed to ultraviolet light. To ensure complete erasure, a dose of 15 watt-second/cm² is required. This means that the device window must be placed within one inch and directly underneath an ultraviolet lamp with a wavelength of 2537 Angstroms, intensity of 12,000µW/cm² for 20 minutes.

Programming Mode

Two programming algorithms are available. The fast programming algorithm is the industry-standard programming mode that requires both initial programming pulses and overprogramming pulses. A flowchart of the fast programming algorithm is shown in Figure 1.

The rapid-pulse programming algorithm has been developed to improve on the programming throughput times in a production environment. Up to 25 100-microsecond pulses are applied until the byte is verified. No overprogramming is required. A flowchart of the rapid-pulse programming algorithm is shown in Figure 2.

Programming takes place when:

a) V_{PP} is brought to proper V_H level,
b) V_{CC} is brought to proper voltage and
c) the $\overline{CE}$ pin is low.

Since the erased state is "1" in the array, programming of "0" is required. The address to be programmed is set via pins A0-A14 and the data to be programmed is presented to pins O0-O7. When data and address are stable, a low-going pulse on the $\overline{CE}$ line programs that location.

Verify

After the array has been programmed it must be verified to ensure all the bits have been correctly programmed. This mode is entered when all the following conditions are met:

a) V_{PP} is at the proper V_H level,
b) V_{CC} is at the proper level,
c) the $\overline{OE}$ line is low.

Inhibit

When programming multiple devices in parallel with different data, only $\overline{CE}$ need be under separate control to each device. By pulsing the $\overline{CE}$ line low on a particular device, that device will be programmed; all other devices with $\overline{CE}$ held high will not be programmed with the data, although address and data will be available on their input pins.

Identity Mode

In this mode specific data is outputted which identifies the manufacturer as Microchip Technology Inc and device type. This mode is entered when Pin A9 is taken to V_H (11.5V to 12.5V). The $\overline{CE}$ and $\overline{OE}$ lines must be at V_{IL}. A0 is used to access any of the two non-erasable bytes whose data appears on O0 through O7.

Pin →	Input	Output								
Identity ↓	A0	O7	O6	O5	O4	O3	O2	O1	O0	Hex
Manufacturer	V_{IL}	0	0	1	0	1	0	0	1	29
Device Type*	V_{IH}	1	0	0	0	1	1	0	0	8C

* Code subject to change.

FIGURE 1 - PROGRAMMING - FAST ALGORITHM

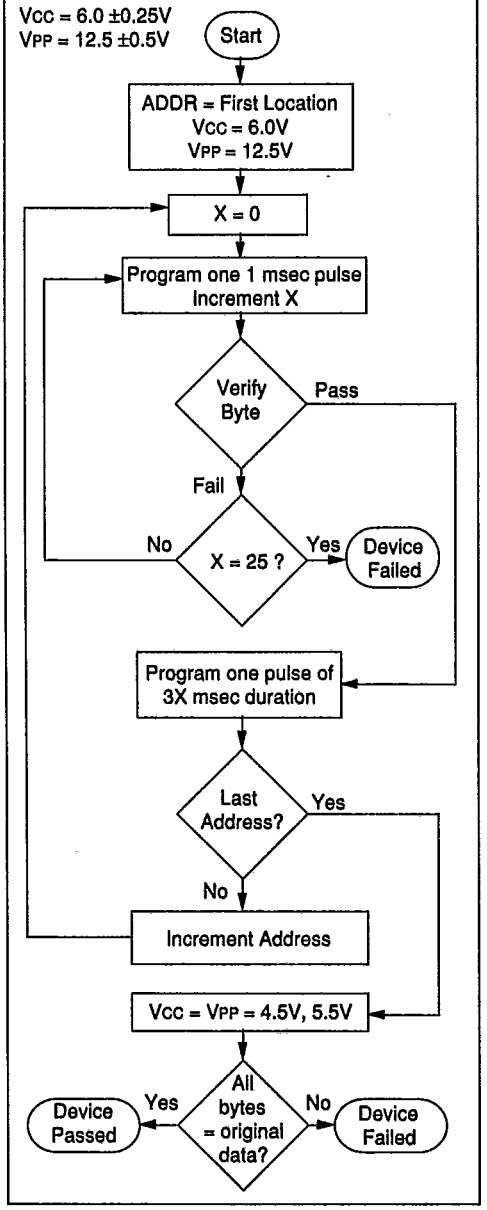
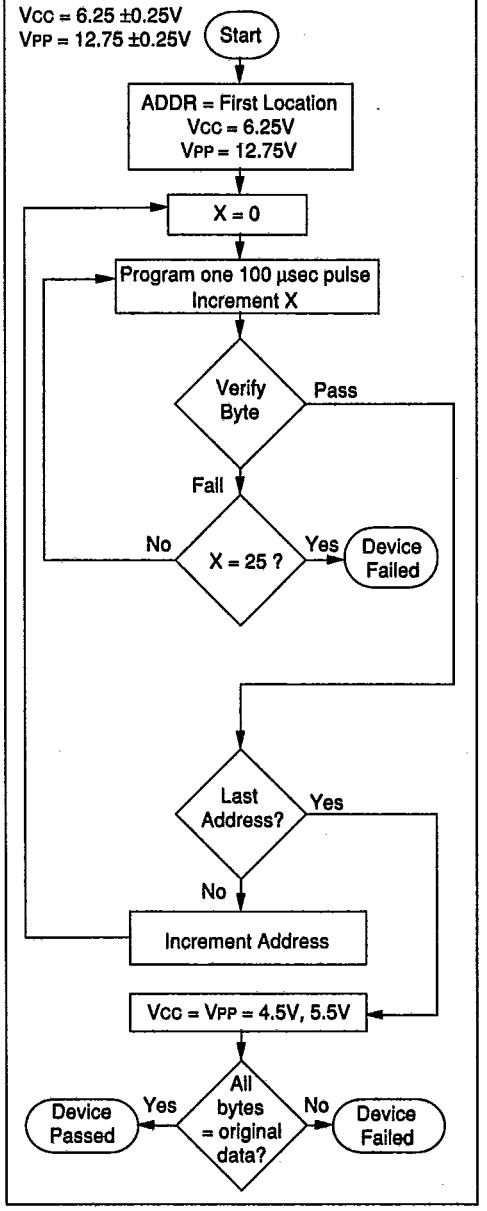


FIGURE 2 - PROGRAMMING - RAPID PULSE ALGORITHM



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SALES AND SUPPORT

To order or to obtain information, e.g., on pricing or delivery, please use the listed part numbers, and refer to the factory or the listed sales offices.

PART NUMBERS

27C256 - 25 I / P

Package:		J	CERDIP
		K	Ceramic Leadless Chip Carrier
		L	Plastic Leaded Chip Carrier (OTP Available)
		P	Plastic DIP (OTP Available)
		SO	SOIC 28 Pin
Temperature Range:		Blank	0° C to 70° C
		I	-40° C to 85° C
Access Time:		15	150 nsec
		17	170 nsec
		20	200 nsec
		25	250 nsec
Device:		27C256	256K (32K x 8) CMOS EPROM