Ordering number : EN 1911C

SANYO Semiconductors

DATA SHEET

CMOS LSI

LC7980 — Controller for the LCD Dot Matrix Graphic Display

Overview

The LC7980 is a controller LSI for the liquid crystal dot matrix graphic display. It stores display data sent from the 8-bit microcomputer in the display RAM attached externally and generates dot matrix LC drive signals.

The LC7980 has two modes — the graphic mode, in which each bit of data from the external RAM either lights or does not light a dot in the LCD, and the character mode, in which character codes stored in the external RAM generate dot patterns through the built-in character-generator ROM. These two ways enable the LC7980 to cover a wide variety of applications.

As the LC7980 is fabricated using CMOS process technology, combining it with a CMOS microcomputer produces an LCD device of low power demand.

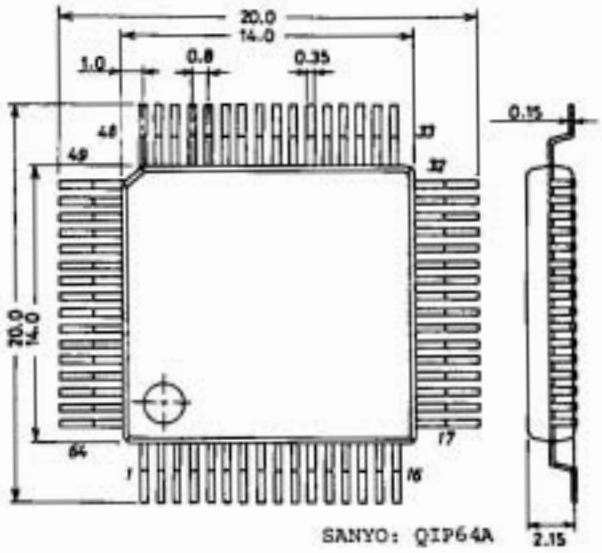
Features

1. Liquid crystal dot matrix graphic display controller
2. Display control capacity.
   Graphic mode ····· 512K dots (2^{16} bytes)
   Character mode ····· 65,536 characters (2^{16} characters)
3. Character generator ROM ····· 7360 bits
   Character font 5 × 7 dots 160 types
   Character font 5 × 11 dots 32 types
   > Total 192 types
   (Extendable to 4K bytes with an external ROM)
4. Interfacing allowed with the 80- and 68-series MPU
5. Display duty (selectable by program)
   From static to 1/256 duty
6. A variety of instruction fucntions
   Scroll, cursor on/off/blink, character blink, bit manipulation
7. Built-in terminal for controlling external RAM
8. Display system ····· B system
9. Data output format.
   Format 1 ····· The output D1 controls the upper screen, and the output D2 the lower screen.
   Format 2 (with ODD/EVEN function) ····· The outputs D1 and D3 control the upper screen, and the outputs D2 and D4 the lower screen
10. Data transfer rate ····· 10M bits/sec. max.
11. Built-in oscillator (X'tal, capacitor attached externally)
12. Low power demand
13. Single +5V power supply

Package Dimensions

unit : mm

3057-QFP64A



SANYO: QIP64A

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Specifications

Absolute Maximum Ratings/T_a=25°C, GND=0V

				unit
Maximum Supply Voltage	V_{DD} max		−0.3 to +7.0	V
Input Voltage	V_I		−0.3 to V_{DD}+0.3	V
Output Voltage	V_O		−0.3 to V_{DD}+0.3	V
Allowable Power demand	Pd max	Ta=75°C	200	mW
Operating Temperature	Topr		−20 to +75	°C
Storage Temperature	Tstg		−55 to +125	°C

Allowable Operation Conditions/T_a=−20 to +75°C, GND=0V

			min	typ	max	unit
Supply Voltage	V_{DD}		4.75		5.25	V
Input "H"-Level Voltage	V_{IH1}	All input, I/O terminals except XT1	2.2		V_{DD}	V
Input "L"-Level Voltage	V_{IL1}	〃 〃	0		0.8	V
Input "H"-Level Voltage	V_{IH2}	XT1	0.7V_{DD}		V_{DD}	V
Input "L"-Level Voltage	V_{IL2}	XT1	0		0.3V_{DD}	V
Output "H"-Level Voltage	V_{OH1}	I_{OH}=−0.6mA, DB0 to 7, $\overline{WE}$, MA0 to 15, RA0 to 3, MD0 to 7, $\overline{CE}$	2.4		V_{DD}	V
Output "L"-Level Voltage	V_{OL1}	I_{OL}=1.6mA, DB0 to 7, $\overline{WE}$, MA0 to 15, RA0 to 3, MD0 to 7, $\overline{CE}$	0		0.4	V
Output "H"-Level Voltage	V_{OH2}	I_{OH}=−0.4mA, FLM, CL1, CL2, D1, D2, D3, D4, MB	V_{DD}−0.4		V_{DD}	V
Output "L"-Level Voltage	V_{OL2}	I_{OL}=0.6mA, FLM, CL1, CL2, D1, D2, D3, D4, MB	0		0.4	V
Clock Frequency	fosc				10	MHz

Electrical Characteristics/T_a=−20 to +75°C, GND=0V, V_{DD}=5V±5%

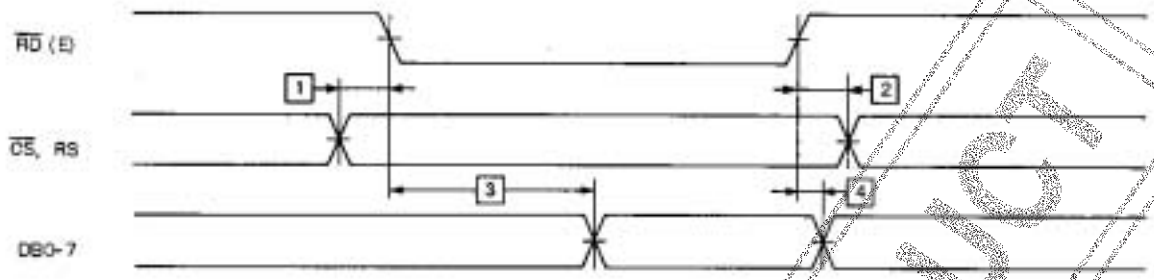
			min	typ	max	unit
Input Leak Current	I_{IN}	V_{IN}= 0 to V_{DD}, $\overline{CS}$, $\overline{RD}$(E), RS, $\overline{WR}$(R/W), $\overline{RES}$, MS	−5		5	μA
Supply Current	I_{DD}	X'tal oscillation, fosc=10MHz		6	9	mA
Pull-up Current	I_{PL}	V_{IN}=GND, DB0 to 7, RD0 to 7, MD0 to 7		10	20	μA

Timing Characteristics

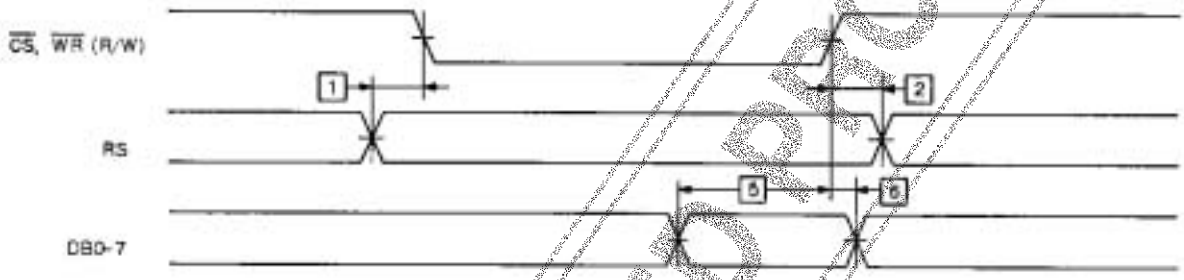
(1) Bus read/write operation 1 (interface with the 68 series MPU)
(2) Bus read/write operation 2 (interface with the 80 series MPU)
(3) Bus read/write operation 3
(4) Interface with external RAM and ROM
(5) Interface with the driver LSI

(1) Bus read/write operation 1 (interface with the 80-series MPU)

READ CYCLE



WRITE CYCLE



(Ta=−20 to +75°C, V_{DD}=5 V±5 %, GND=0 V)

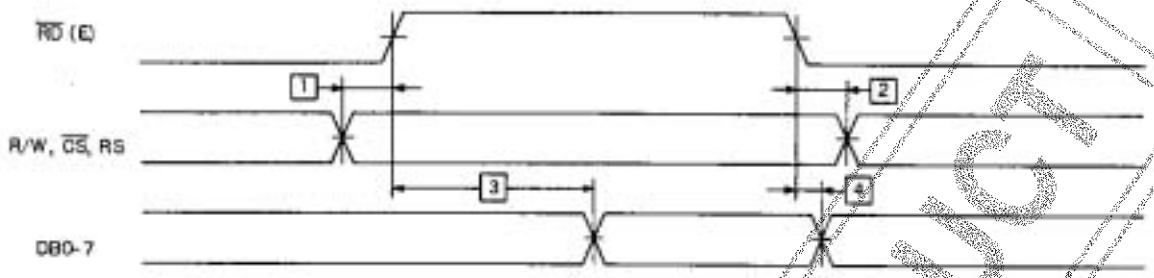
No.	Item	Symbol	min	typ	max	unit	Condition
1	Address set-up time	t_{AS}	10	—	—	ns	
2	Address hold time	t_{AH}	60	—	—	ns	
3	Data delay time	t_{DDR}	—	—	130	ns	C_L=50pF
4	Data hold time (read)	t_{DHR}	0	—	—	ns	
5	Data set-up time	t_{DSW}	125	—	—	ns	
6	Data hold time (write)	t_{DHW}	28	—	—	ns	

Note (1) Definition of the test waveform

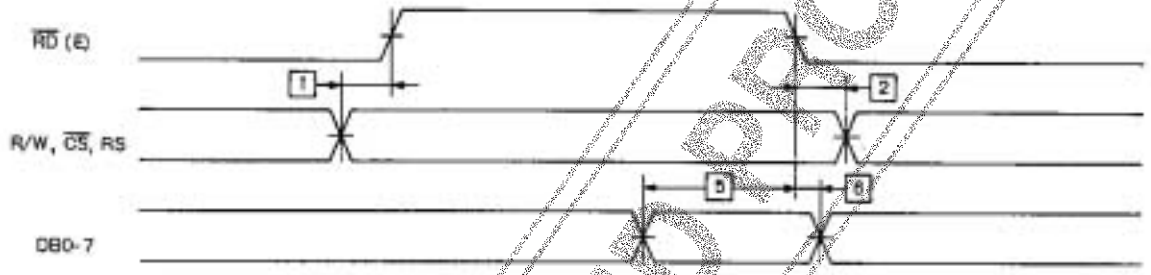
The input terminals are driven at 2.4V and 0.45V. Timing is measured at 1.5V.

(2) Bus read/write operation 2 (interface with the 68-series MPU)

READ CYCLE



WRITE CYCLE



(Ta=−20to+75℃, V_{DD}=5 V±5%, GND=0 V)

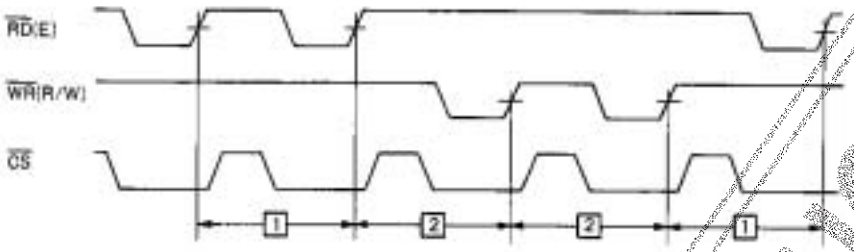
No.	Item	Symbol	min	typ	max	unit	Condition
1	Address set-up time	t_{AS}	90	—	—	ns	
2	Address hold time	t_{AH}	10	—	—	ns	
3	Data delay time (read)	t_{DDR}	—	—	140	ns	C_L=50pF
4	Data hold time (read)	t_{DHR}	10	—	—	ns	
5	Data set-up time (write)	t_{DSW}	220	—	—	ns	
6	Data hold time (write)	t_{DHW}	20	—	—	ns	

Note (1) Definition of the test waveform

The input terminals are driven at 2.4V and 0.45V. Timing is measured at 1.5V.

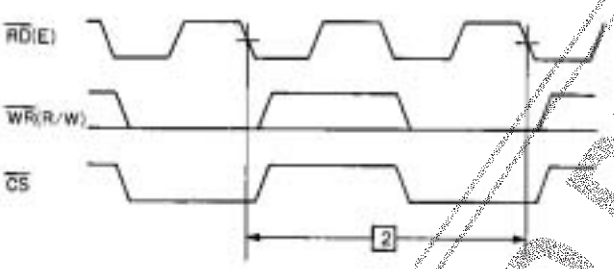
(3) Bus read/write operation 3

80-series MPU interface (MS=GND, RS=GND)

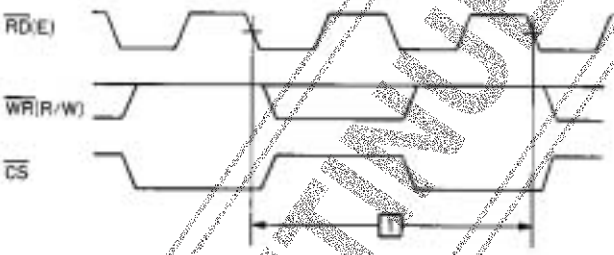


68-series MPU interface (MS=V_{DD}, RS=GND)

ⓐDATA WRITE CYCLE



ⓑDATA READ CYCLE



($Ta=-20$ to $+75°C$, $V_{DD}=5\,V\pm5\,\%$, GND=0 V)

No.	Item	Symbol	min	typ	max	unit	Instruction register value
1	Read cycle time	t_{RCY}	–	–	$\frac{2\times10^3\times(Hp+2)}{F_{OSC}}+200$	ns	0DH
2	Write cycle time	t_{WCY1}	–	–	$\frac{2\times10^3\times(2Hp+2)}{F_{OSC}}+200$	ns	0EH, 0FH
2	Write cycle time	t_{WCY2}	–	–	$\frac{2\times10^3\times(Hp+2)}{F_{OSC}}+200$	ns	0CH
2	Write cycle time	t_{WCY3}	–	–	$\frac{4000}{F_{OSC}}+200$	ns	00H, 01H, 02H, 03H, 04H, 08H, 09H, 0AH, 0BH

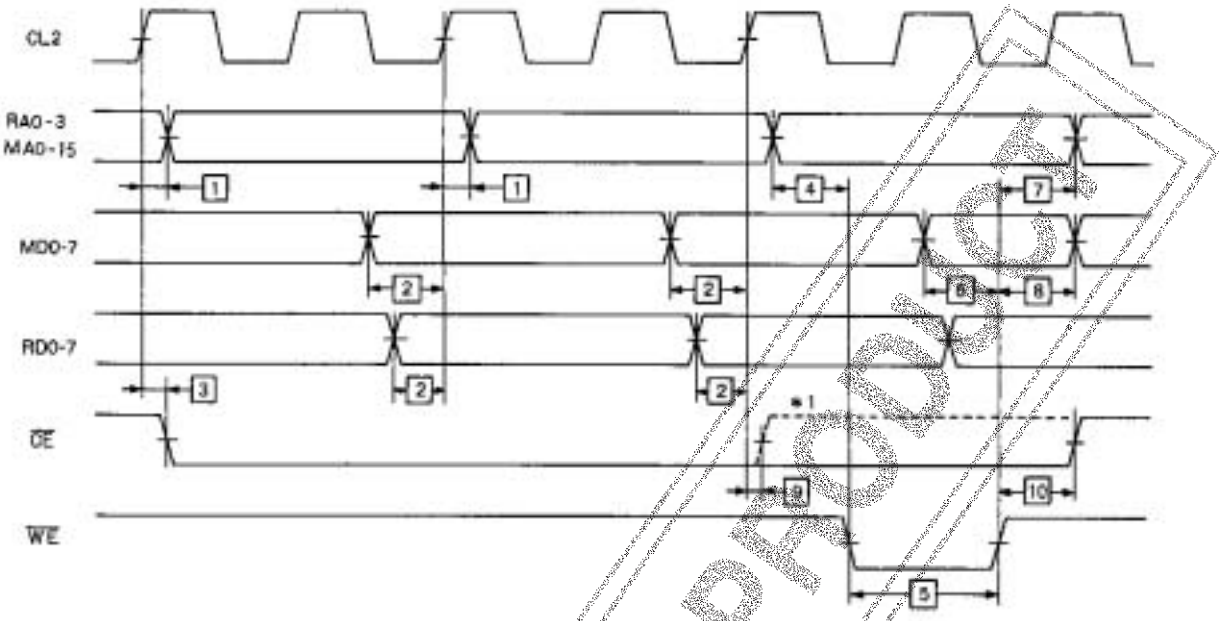
Notes

(1) In the character mode, Hp is the number of horizontal dots per character in a character display. In the graphic mode, Hp indicates how many bits from RAM appear in a 1-byte display.

(2) F_{OSC} is the oscillating frequency, expressed in MHz.

(3) All measurement points are at 1.5V.

(4) Interface with external RAM and ROM



READ CYCLE (Ta=−20 to +75°C, VDD=5 V±5 %, GND=0 V)

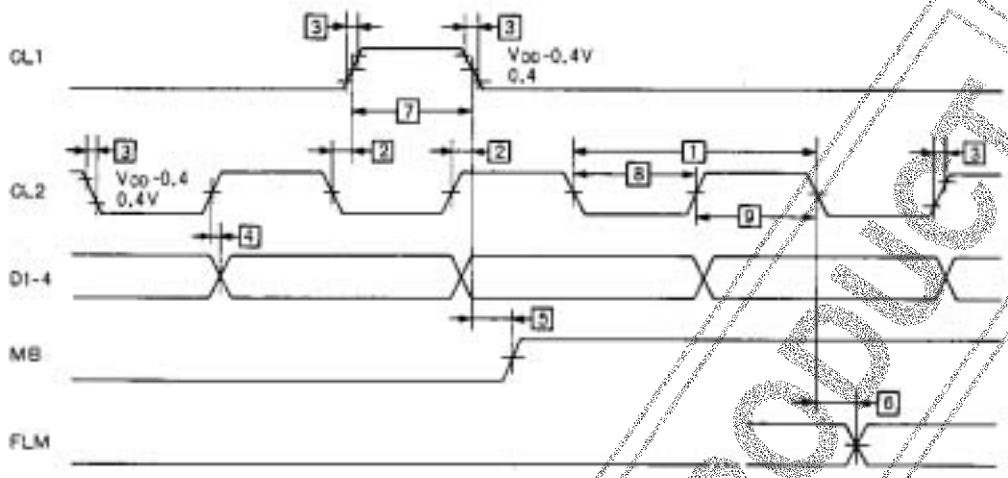
No.	Item	Symbol	min	typ	max	unit	Condition
1	MA0-15, RA0-3 read address delay time	tDMRA	—	—	95	ns	
2	MD0-7, RD0-7 set-up time	tSMRD	105	—	—	ns	
3	$\overline{CE}$ delay time	tDCE	—	—	95	ns	
9	$\overline{CE}$ hold time	tHCER	0	—	—	ns	

WRITE CYCLE (Ta=−20 to +75°C, VDD=5 V±5 %, GND=0 V)

No.	Item	Symbol	min	typ	max	unit	Condition
4	Memory address set-up time	tSMAW	0	—	—	ns	
5	$\overline{WE}$ pulse width	tWWE	170	—	—	ns	
6	Memory data set-up time	tSMDW	100	—	—	ns	
7	Memory address hold time	tHMAW	0	—	—	ns	
8	Memory data hold time	tHMDW	0	—	—	ns	
10	$\overline{CE}$ hold time	tHCEW	0	—	—	ns	

Notes
(1) *1 is timing in which display data is not written into or read from the MPU.
(2) All output terminals are under no load.
(3) All measurement points are at 1.5V.

(5) Interface with the driver LSI

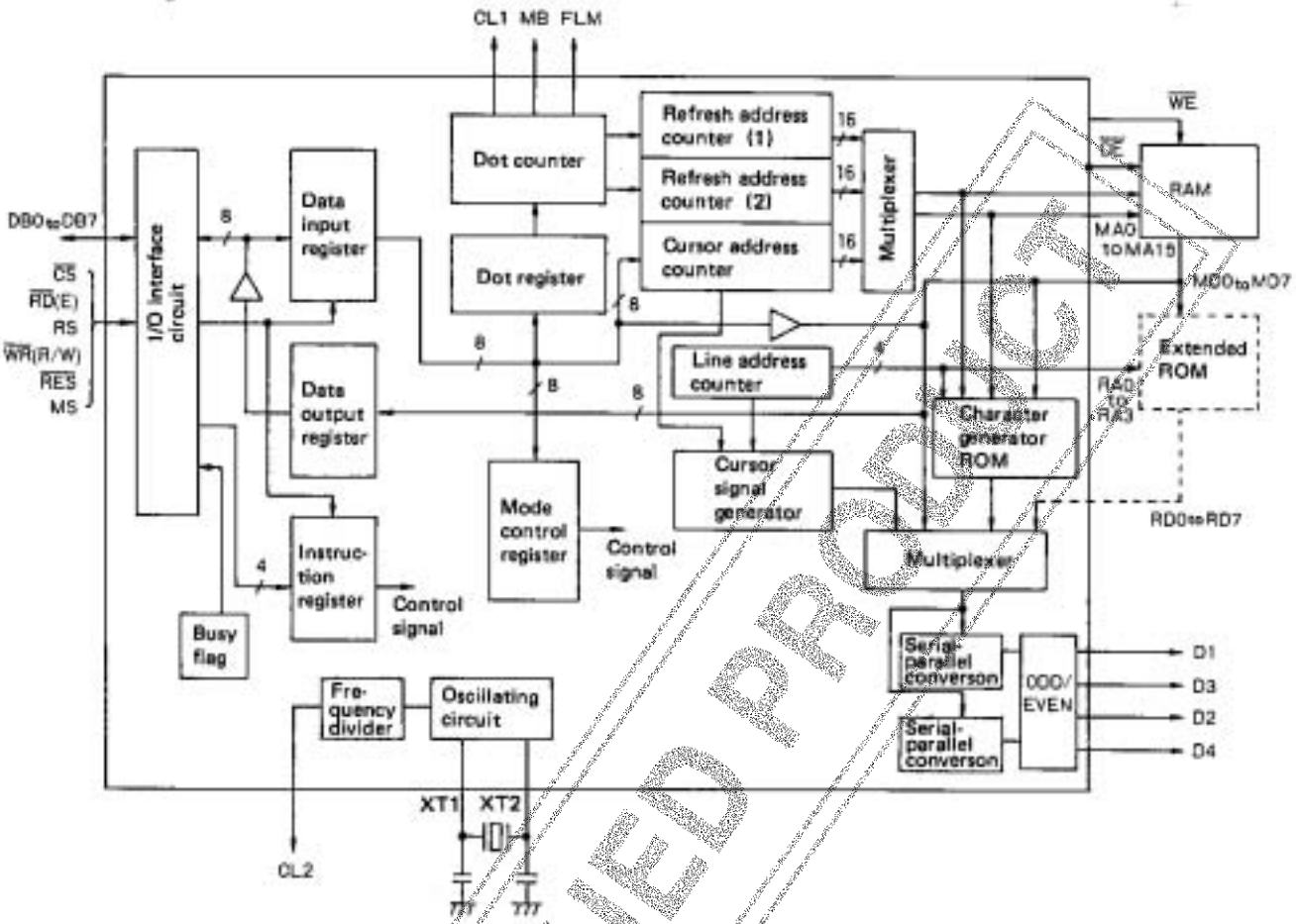


Ta=−20to+75℃, V_{DD}=5 V±5 %, GND=0 V

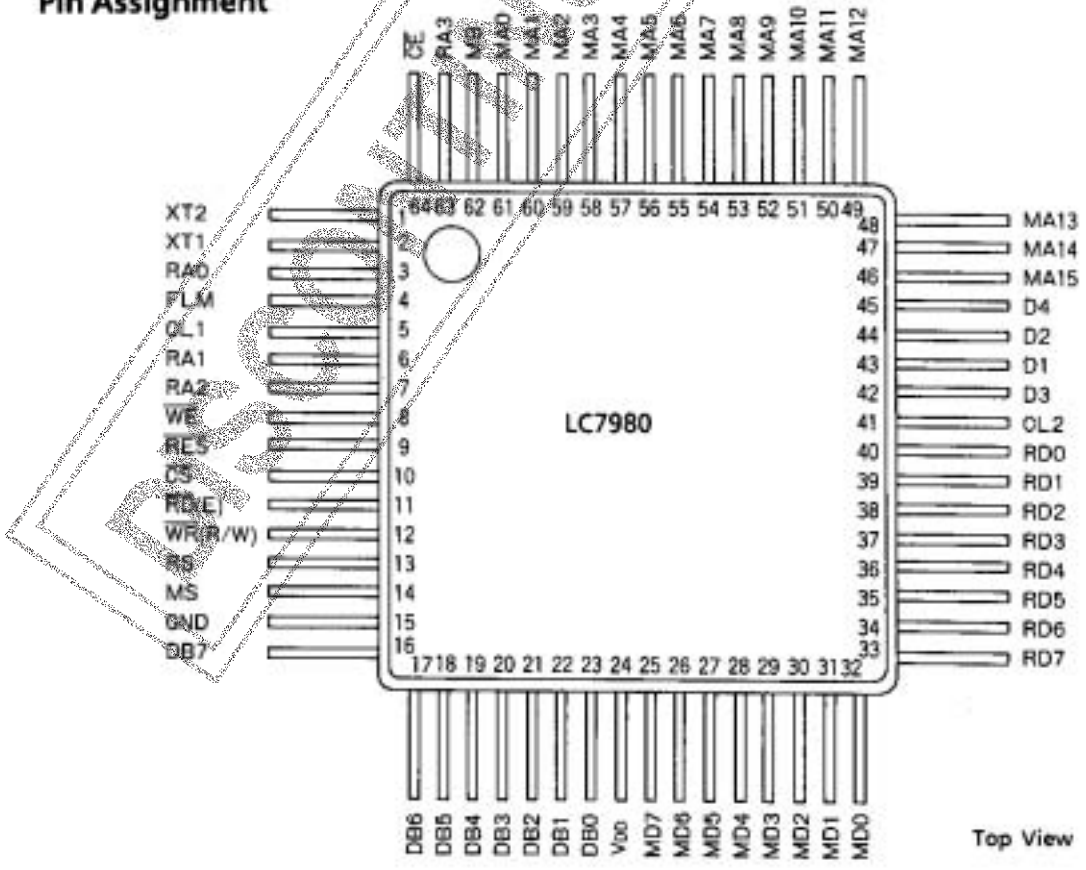
No	Item	Symbol	min	typ	max	unit	Condition
1	Clock cycle time	tCYC	200			ns	
			400			ns	ODD/EVEN mode
2	Clock phase difference	tDCL			100	ns	
3	Clock rise/fall time	tCRF			30	ns	
4	D1-4 phase difference	tDD			100	ns	
5	MB phase difference	tDMA			100	ns	
6	FLM phase difference	tDFM			100	ns	
7	CL1 clock pulse width (H level)	tWCH1	95			ns	
			195			ns	ODD/EVEN mode
8	CL2 clock pulse width (L level)	tWCL2	95			ns	
			195			ns	ODD/EVEN mode
9	CL2 clock pulse width (H level)	tWCH2	95			ns	
			195			ns	ODD/EVEN mode

Notes
(1) All output terminals are under no load.
(2) All measurement points other than those specified are at $0.5V_{DD}$.

Block Diagram



Pin Assignment



Function of each block

- Register

  The LC7980 has 5 types of registers — the instruction register, data input register, data output register, dot register, and mode control register.

  The instruction register stores such instruction codes as the start address, cursor address specification, etc. It consists of 4 bits, and the lower 4 bits of the data bus, DB0 to DB3, are written into it.

  The data input register temporarily stores data to be written into the external RAM, dot register, and mode control register. It consists of 8 bits.

  The data output register temporarily stores data to be read from external RAM, and consists of 8 bits. When the cursor address is written into the cursor address counter via the data input register and the memory read instruction is set in the instruction register, data in external RAM is read into the data output register by internal operation. With the next instruction, the MPU reads the data output register, and completes data transfer to the MPU.

  The dot register stores dot information such as the character pitch, the number of vertical dots, etc. Data sent from the MPU is written into the dot register via the data input register.

  The mode control register stores LCD status information such as display on/off and cursor on/off/blink. It consists of 8 bits. Data sent from the MPU is written into this register via the data input register.

- Busy flag

  When the Busy flag is "1", the LC7980 is operating internally. At this time, the next instruction cannot be accepted. The Busy flag is output to DB7 when RS=1, $\overline{RD}$(E)=0 (MS=0) or RS=1, $\overline{WR}$(R/W), $\overline{RD}$(E)=1 (MS=1). The next instruction must be written after ensuring that the Busy flag is "0".

- Dot counter

  The dot counter generates LC display timing according to the contents of the dot register.

- Refresh address counter

  The refresh address counter controls addresses of the external RAM and is available in two types — refresh address counter (1) and refresh address counter (2). The former is for the upper screen, and the latter for the lower screen.

- Row address counter

  In the character mode, this counter outputs raster addresses RA0 to 3 for the character generator ROM.

- Character generator ROM

  The character generator ROM has a total of 7360 bits and stores data on 192 kinds of characters. Character codes from the external RAM and row codes from the line address counter are added to address signals, and ROM outputs 5-bit dot data.

  There are 192 kinds of character fonts, of which 160 are 5 x 7 and 32 are 5 x 11, With extended ROM, character fonts can be increased to 256 kinds sized 8 x 16.

- Cursor address counter

  The cursor address counter is a 16-bit counter which can be preset by instruction. When data is read from or written into external RAM (i.e., read/write of display dot data or character codes), the counter retains the addresses. The value indicated on the cursor address counter is automatically incremented by 1 when instructions to read/write display data and to perform bit set/clear are issued.

- Cursor signal generator

  In the character mode, the cursor can be displayed by means of instructions. The cursor is generated automatically when the cursor address counter and the row address counter reach the specified value.

- Parallel-serial conversion

  The two parallel-serial conversion circuits simultaneously transfer parallel data from the external RAM, character generator, and extended ROM to the upper and lower LC screen drive circuits as serial data.

- ODD/EVEN

  Data output from the parallel-serial conversion circuit is divided into even-numbered data and odd-numbered data, then output to D1 through D4.

Pin Functions

Pin Name	Pin No.	Function
DB0 to 7	16 to 23	Data bus ----- Three-state I/O common terminal, terminal for transmitting/receiving data to/from the MPU.
$\overline{CS}$	10	Chip select ----- Selection allowed when $\overline{CS}$=0
MS	14	Terminal for selection between the 68- and 80-series MPU, MS=0 ----- 80 series, MS=1 ----- 68 series.
$\overline{RD}$ (E)	11	• MS=0 (when connected to the 80-series MPU) Read ----- MPU ← LC7980 • MS=1 (when connected to the 68-series MPU) Enable ----- Data is written at the negative going edge of $\overline{RD}$(E). Data can be read while $\overline{RD}$(E)=1.
$\overline{WR}$ (R/W)	12	• MS=0 (when connected to the 80-series MPU) Write ----- MPU → LC7980 • MS=1 (when connected to the 68-series MPU) Read/write ----- $\overline{WR}$ (R/W)=1 ----- MPU ← LC7980 $\overline{WR}$ (R/W)=0 ----- MPU → LC7980
RS	13	Register select ----- RS=1 ----- instruction register RS=0 ----- data register
XT1, XT2	1, 2	Terminal for the X'tal oscillator.
$\overline{RES}$	9	Reset ----- Setting $\overline{RES}$ to 0 selects display OFF, 1-bit serial transfer method, 32-frame blink period, and Hp=6.
MA0 to 15	46 to 61	Address output for the display RAM.
RA0 to 3	3, 6, 7, 63	Raster address output for the external character generator ROM.
MD0 to 7	25 to 32	Display data bus ----- Three-state I/O common terminal.
RD0 to 7	33 to 40	ROM data input ----- Dot data from the external character generator is input.
$\overline{WE}$	8	Write enable ----- Display RAM write signal.
$\overline{CE}$	64	Display RAM chip enable signal.
CL2	41	Display data shift clock signal.
CL1	5	Display data latch signal.
FLM	4	Frame signal.
MB	62	LC drive signal ----- AC signal ----- B system
D1, D2 D3, D4	42 to 45	Display data serial output ----- D1, D3 ----- for the upper screen D2, D4 ----- for the lower screen

(Note) When mounting on the PCB, do not dip it in solder.

- **Display control instruction**

Display is controlled by writing data into the instruction register and 13 data registers. The instruction register and the data register are distinguished by the RS signal. First, write 4-bit data in the instruction register when RS=1, then specify the code of the data register. Next, with RS=0, write 8-bit data in the data register, which executes the specified instruction.

A new instruction cannot be accepted while an old instruction is being executed. As the Busy flag is set under this condition, write an instruction only after reading the Busy flag and making sure that it is 0.

However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction. The Busy flag does not change when data is written into the instruction register (RS=1). Therefore, the Busy flag need not be checked immediately after writing data into the instruction register.

1) Mode control

Write code "00H" (in hexadecimal notation) in the instruction register and specify the mode control register.

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	0	0
Mode control Reg	0	0	MODE Data							

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Cursor/blink	CG	Graphic/character display
1/0	1/0	1/0	—	0	0	0	0	Cursor OFF	Built-in CG	Character display
				0	1			Cursor ON		
				1	0			Cursor OFF character blink		
				1	1			Cursor blink		
				0	0		1	Cursor OFF	External CG	
				0	1			Cursor ON		
				1	0			Cursor OFF character blink		
				1	1			Cursor blink		
				0	0	1	0			Graphic mode
Output transfer method	Blink time	Display ON/OFF		Blink	Cursor	Mode	External/built-in CG			

1 : display ON
0 : display OFF

1 : 16 frames
0 : 32 frames

1 : transfer with the ODD/EVEN function
0 : 1-bit serial transfer

2) Setting the character pitch

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	0	1
Character pitch Reg	0	0	(Vp−1) Binary				0	(Hp−1) Binary		

Vp is the number of vertical dots per character. Determine Vp with the pitch between two vertically placed characters taken into consideration. This value is meaningful only in the character display mode. It is invalid in the graphic mode.

In character mode, Hp indicates the number of horizontal dots per character, from the leftmost part of one character to the leftmost part of the next. In the graphic mode, Hp indicates how many bits (or dots) from RAM appear in a 1-byte display.

Hp must take one of the following three values.

Hp	DB2	DB1	DB0	
6	1	0	1	Horizontal character pitch 6
7	1	1	0	" 7
8	1	1	1	" 8

3) Setting the number of characters

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	1	0
Character number Reg	0	0	(HN−1) Binary							

In the character display mode, H_N indicates the number of characters in the horizontal direction. In the graphic mode, it indicates the number of bytes in the horizontal direction. The total number of dots positioned horizontally on the screen n is given by the formula

$$n = Hp \times H_N.$$

Even numbers in the range 2 to 256 (decimal) can be set as H_N.

4) Setting the number of time divisions (display duty)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	0	1	1
Time division Reg	0	0	(Nx−1) Binary							

Nx represents the number of time divisions.

Consequently, 1/Nx is the display duty.

Decimal numbers within the range 1 to 256 can be set as Nx.

5) Setting the cursor position

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	0	1	0	0
Cursor position Reg	0	0	0	0	0	0	(Cp−1) Binary			

In the character display mode, Cp indicates the line at which the cursor is displayed. For example, when Cp=8 (decimal) is specified, the cursor is displayed beneath the character of the 5 x 7 dot-font. The horizontal length of the cursor equals Hp (the horizontal character pitch). Decimal values in the range 1 to 16 can be assigned to Cp. When the value is less than the vertical character pitch Vp ($Cp \leq Vp$), display priority is given to the cursor (provided the cursor display is ON). The cursor is not displayed when $CP > Vp$. The horizontal length of the cursor equals Hp.

6) Setting the display start lower address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	0	0
Display start address Reg (lower byte)	0	0	(start address lower byte) binary							

7) Setting the display start upper address

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	0	1
Display start address Reg (upper byte)	0	0	(start address upper byte) binary							

This instruction writes the display start address value in the display start address register. The display start address is the RAM address at which data to be displayed at the leftmost position of the top line of the screen is stored. The start address consists of 16 bits (upper and lower).

8) Setting the cursor (lower) address (RAM read/write lower address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	1	0
Cursor address counter (lower byte)	0	0	(cursor address lower byte) binary							

9) Setting the cursor (upper) address (RAM read/write upper address)

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	0	1	1
Cursor address counter (upper byte)	0	0	(cursor address upper byte) binary							

This instruction writes the cursor address value in the cursor address counter. The cursor address indicates the address for exchanging display data and character codes with RAM. In other words, data at the address specified by the cursor address is read from or written into RAM. In character display, the cursor is displayed at the position specified by the cursor address.

The cursor address is divided into a lower address (8 bits) and an upper address (8 bits). It should be set in accordance with the following rules.

1	To rewrite (set) both lower and upper addresses:	First set the lower address, then the upper.
2	To rewrite the lower address:	Always reset the upper address after setting the lower address.
3	To rewrite the upper address only:	Set the upper address. It is unnecessary to reset the lower address.

The cursor address counter is a 16-bit up-counter with set/reset functions: when the Nth bit goes from 1 to 0, the count of the (N + 1)th bit increments by one. Accordingly, when the lower address is set so that the lower MSB (8th bit) changes from 1 to 0, the LSB (1st bit) of the upper counter must increment by one. When setting the cursor address, set the lower and upper addresses as a 2-byte continuous instruction.
In character display, the cursor is displayed at the position where the lower 14 bits of the display address and the lower 14 bits of the cursor address agree, and the upper 2 bits are ignored.

10) Writing display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	0	0
RAM	0	0	MSB (pattern data, character code)							LSB

Write code "0DH" in the instruction register. Then, write 8-bit data with RS=0, and the data is written into RAM as display data or character codes at the address specified by the cursor address counter. After writing, the count of the cursor address counter increments by 1.

11) Reading display data

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	0	1
RAM	1	0	MSB (pattern data, character code)							LSB

Write "0CH" in the instruction register. Then, establish the read status with RS=0, and data in the RAM can be read. The procedure for reading data is as follows:

This instruction outputs the contents of the data output register to DB0 to 7, then transfers the RAM data indicated by the cursor address to the data output register. It then increments the cursor address by 1, which means that correct data cannot be read in the first read operation. The specified value is output in the second read operation. Accordingly, a dummy read operation must be performed once when reading data after setting the cursor address.

12) Bit clear

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	1	0
Bit clear	0	0	0	0	0	0	0	(N_B-1) Binary		

13) Bit set

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Instruction Reg	0	1	0	0	0	0	1	1	1	1
Bit set	0	0	0	0	0	0	0	(N_B-1) Binary		

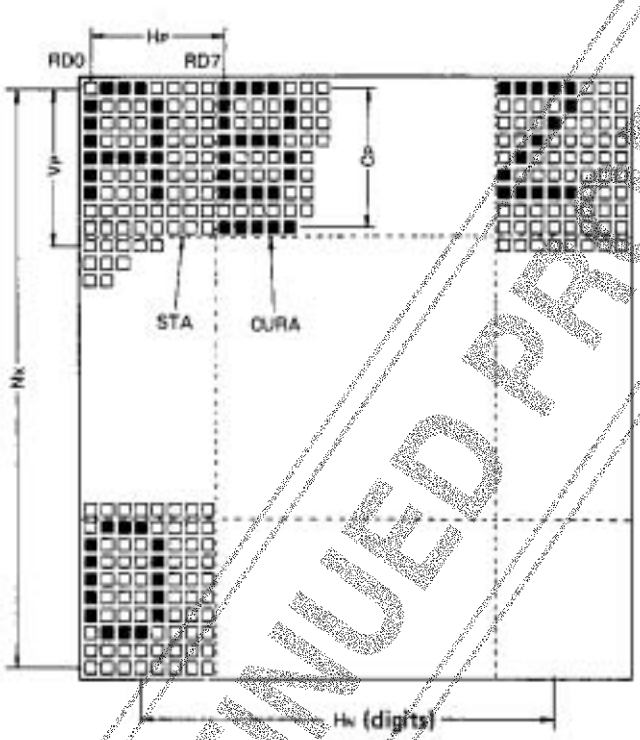
As the bit-clear or bit-set instruction, 1 bit of a 1 byte of data in display RAM is set to 0 or 1. The bit specified by N_B is set to 0 for the bit-clear instruction and 1 for the bit-set instruction. The RAM address is specified by the cursor address, which is automatically incremented by 1 at the completion of the instruction. N_B is a value in the range from 1 to 8. The LSB is indicated by N_B=1, and the MSB by N_B=8.

14) Reading the BUSY flag

Register	R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Busy flag	1	1	I/O	*						

The Busy flag is output to DB7 when read mode is established with RS=1. The Busy flag is set to 1 while any of the instructions 1) through 13) is being executed. It is set to 0 at the completion of the execution, allowing the next instruction to be accepted. No other instruction can be accepted when the Busy flag is 1. Accordingly, before writing an instruction and data, it is necessary to ensure that the Busy flag is 0. However, the next instruction can be executed without checking the Busy flag when the maximum read cycle time or the write cycle time has been exceeded after execution of the previous data read instruction or the data write instruction.
The Busy flag does not change when data is written into the instruction register (RS=1). Therefore, the Busy flag need not be checked immediately after writing data into the instruction register.
Specification of the instruction register is unnecessary to read the Busy flag.

The relation between the LCD panel display and Hp, H_N, Vp, Cp, and Nx.



Symbol	Description	Meaning	Value
Hp	Horizontal character pitch	Character pitch in the horizontal direction	6 to 8 dots
H_N	Number of characters in the horizontal direction	Number of characters (digits) per horizontal line or the number of words per line (graphic)	Even digits in the range 2 to 256
Vp	Vertical character pitch	Character pitch in the vertical direction	1 to 16 dots
Cp	Cursor position	The line number at which the cursor is to be displayed	1 to 16 lines
Nx	Number of lines in the vertical direction	Display duty	1 to 256 lines

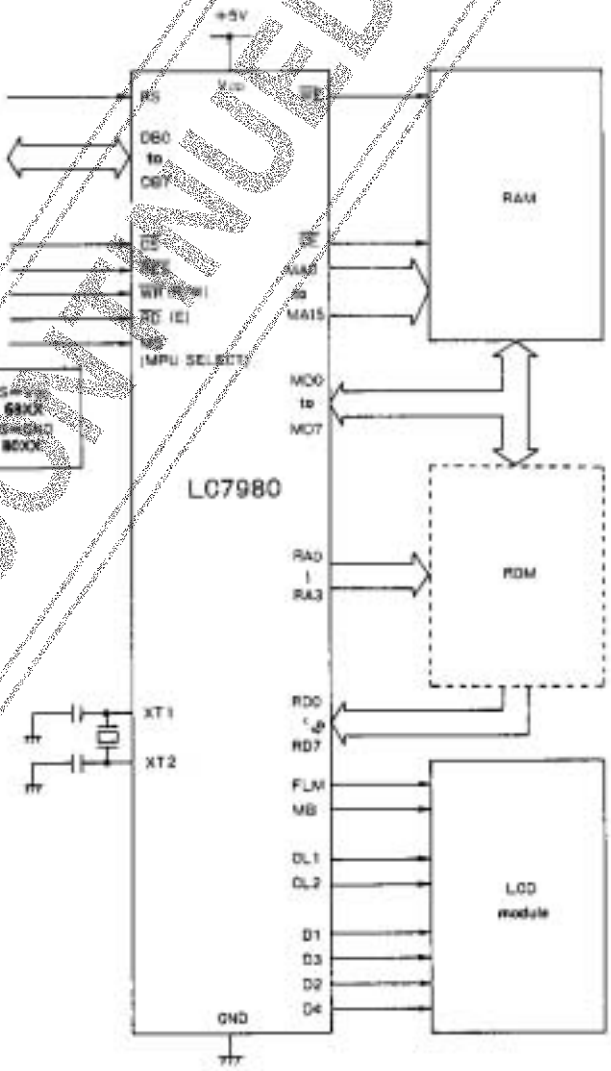
Note)
When the number of vertical dots on the screen is m and that of horizontal dots is n,

$1/m = 1/Nx$ = display duty
$n = Hp \times H_N$
m/Vp = number of display lines
$Cp \leq Vp$

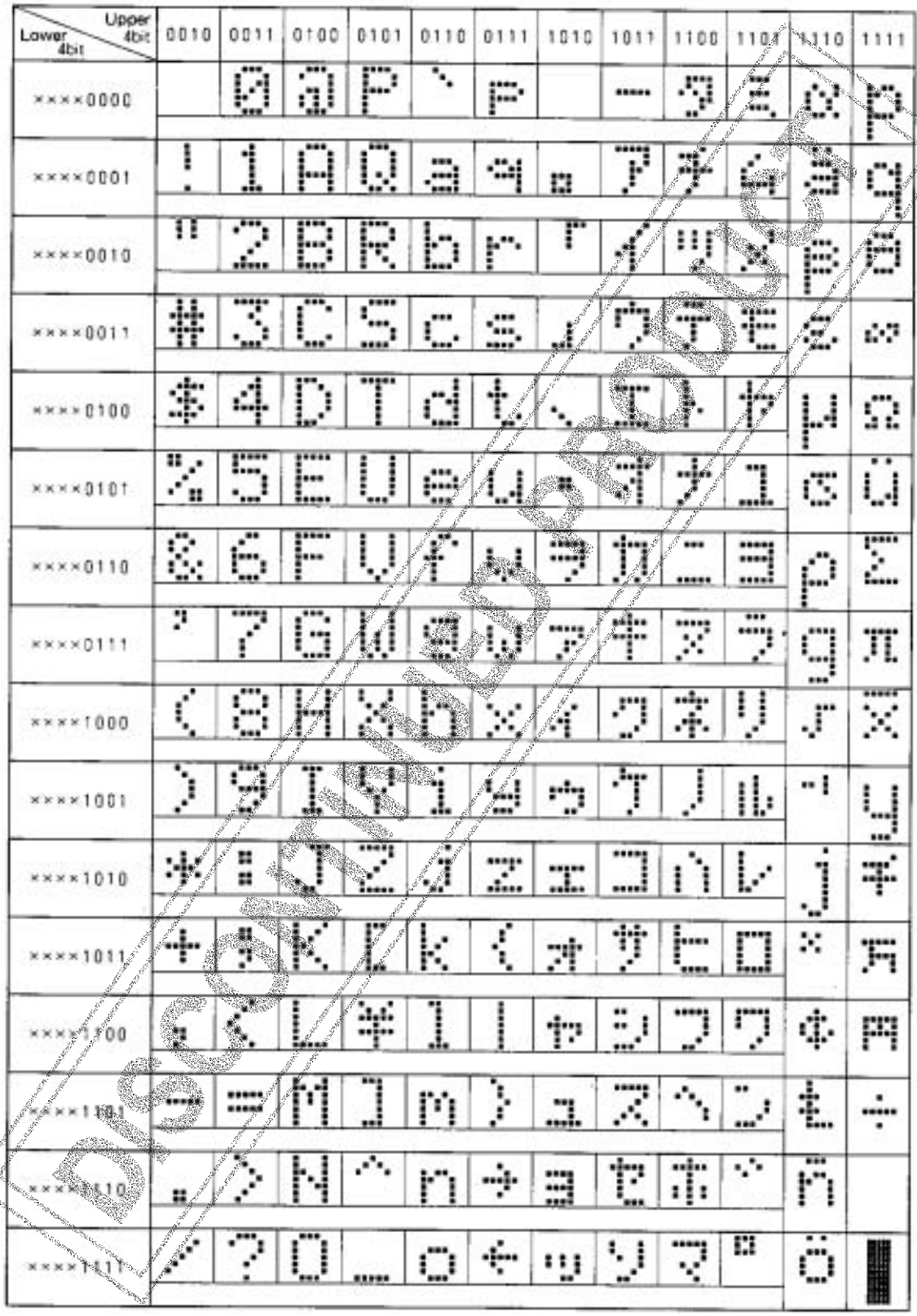
Display mode

Display mode	Display data from the MPU	RAM	LC panel
Character display	Display pattern (8 bits)	Start address	Hp: 6,7 or 8 dots
Graphic	Character code (8 bits)	Start address	8 dots, 8 dots; Hp: 8 dots

Sample application circuit

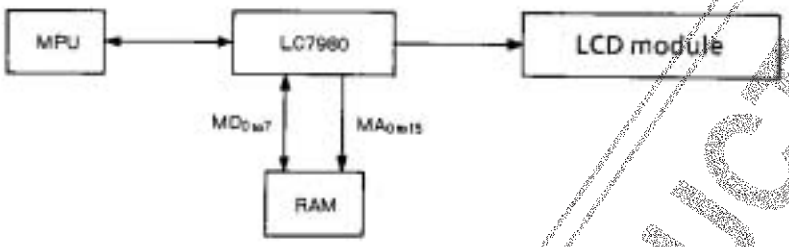


Built-in character generator

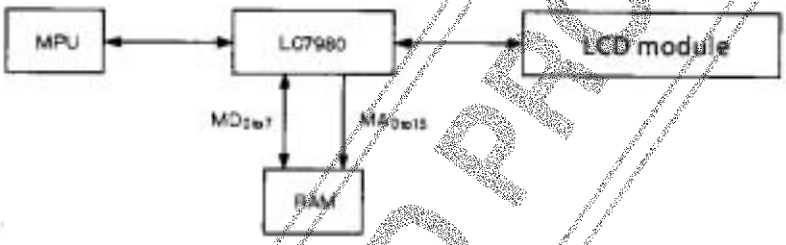


Sample configurations

- Graphic mode



- Character display mode (1) (built-in character generator)



- Character display mode (2) (external character generator)