TEF6635; TEF6638

Highly efficient radio one-chip

Rev. 2 — 19 July 2011 Product data sheet

1. General description

The TEF6635 and TEF6638 devices are radio and audio single-chip ICs. These ICs contain an AM/FM radio tuner, software defined radio signal processing, audio processing and input/output selection.

The TEF6638 is the premium version that provides the full feature set. The TEF6635 is the lite version including a basic feature set.

The AM/FM radio receiver includes the front ends, tuning synthesizer, channel filtering, FM multipath improvement, demodulation, FM stereo decoding, weak signal processing, noise blanking and Radio Data System (RDS) reception. A maximum amount of digital signal processing is used, taking full advantage of the CMOS IC technology.

The audio processing block receives audio signals from the internal AM/FM radio receiver, external digital radio or external analog or digital audio sources. The audio signal processing contains basic functionality as tone-volume control as well as advanced digital audio processing functionality as audio equalization, chimes etc. The output signals of the audio processing block are provided in digital format on the host I^2S outputs and in analog format on the audio DAC outputs.

The TEF6638 supports the digital standards HD Radio and Digital Radio Mondiale (DRM) in combination with NXP terrestrial digital radio coprocessors such as SAF356x.

2. Features and benefits

- All in one digital receiver including tuner, software defined radio and audio processing
- Easy to control with high-level user interface
- FM receiver with a tuning range from 65 MHz to 108 MHz covering OIRT, Japan, Europe and US bands
- AM receiver covering Long Wave (LW), Medium Wave (MW) and full Short Wave (SW) bands
- Fully integrated tuning system combining low phase noise and fast tuning times
- FM Low-Noise Amplifier (LNA) with Automatic Gain Control (AGC)
- FM mixer for frequency conversion to a low Intermediate Frequency (IF) complex signal
- AM front-end LNA and AGC matching active and passive antenna applications
- AM MW RF selectivity with integrated capacitor bank and automatic calibration
- AM mixer for frequency conversion to a low IF complex signal

- High dynamic range Sigma-Delta (SD) IF Analog-to-Digital Converter (ADC)
- Digital IF signal processing including decimation, shift to baseband, AGC control, In-phase/Quadrature-phase (I/Q) correction, Precision Adjacent Channel Suppression (PACS), FM multipath suppression and demodulation
- Baseband I^2S output for support of HD Radio and DRM with external digital radio coprocessor (TEF6638)
- Signal quality detection, FM stereo decoding, noise blanking and weak signal processing
- Advanced RDS and Radio Broadcast Data System (RBDS) demodulation and decoding with versatile output configuration
- One (TEF6635) or two (TEF6638) stereo third-order sigma-delta audio Analog-to-Digital Converters (ADCs) with an anti-aliasing input filter
- Three analog audio inputs with flexible input configuration connected to the analog input selector and audio ADC
- One differential stereo input connected to the second audio ADC (TEF6638)
- Two (TEF6635) or three (TEF6638) asynchronous Inter IC Sound (I^2S) inputs
- One analog Sony Philips Digital InterFace (SPDIF) format input
- One digital SPDIF input, mutually exclusive with one asynchronous I^2S input
- One (TEF6635) or two (TEF6638) synchronous I^2S inputs and outputs in master mode
- Audio sample rate converters
- Digital audio processing with tone and volume control functions
- Four audio Digital-to-Analog Converters (DACs)
- Single 3.3 V supply voltage
- Fast mode I^2C-bus (400 kHz)
- Built-in 1.2 V regulator control circuit
- Qualified in accordance with AEC-Q100

3. Applications

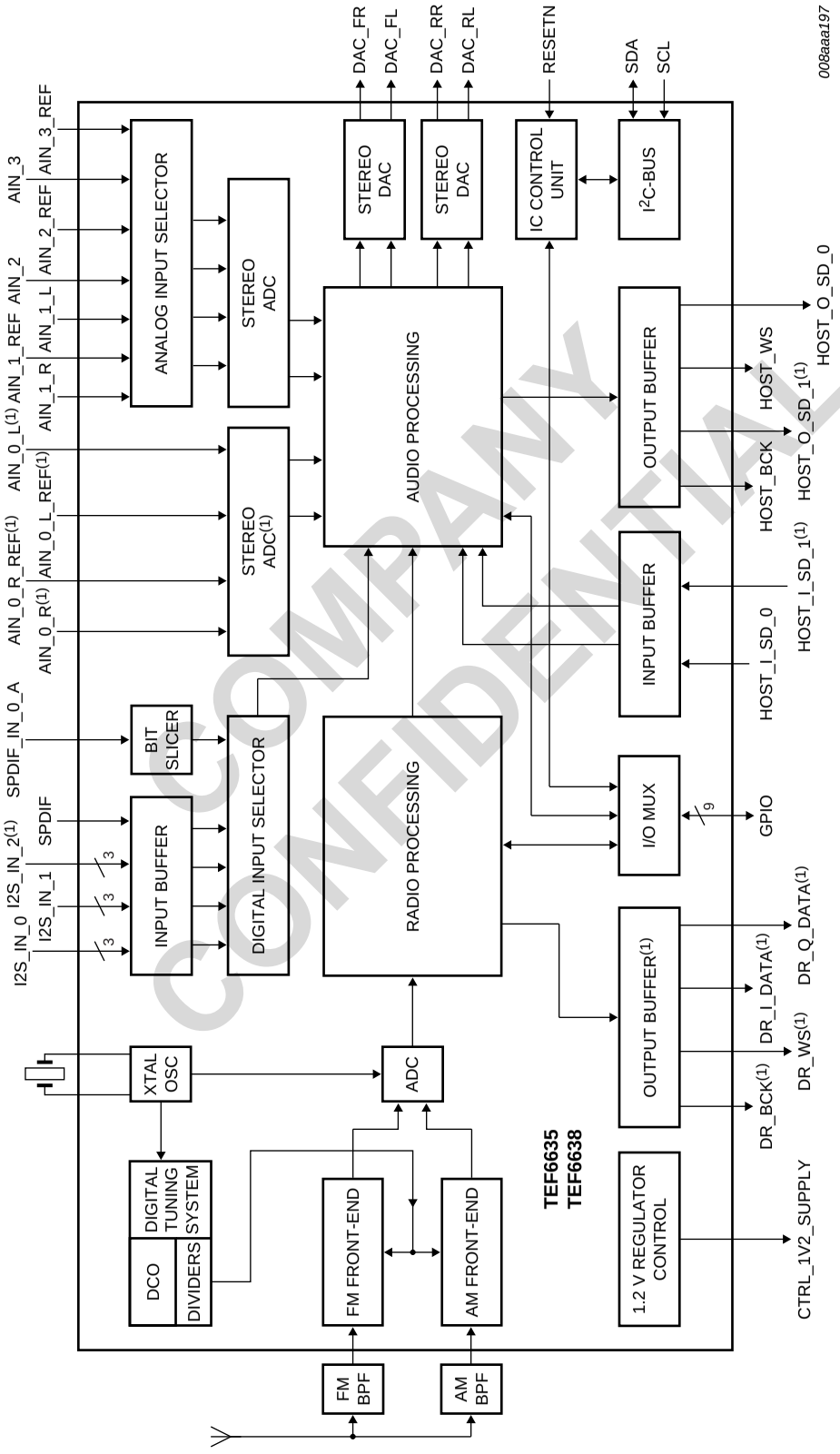
- Single tuner AM/FM receivers addressing aftermarket and entry-level to mainstream OEM in the automotive segment

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEF6635HW	HTQFP100	plastic thermal enhanced thin quad flat package; 100 leads; body 14 × 14 × 1 mm; exposed die pad	SOT638-3
TEF6638HW			

5. Functional diagram



(1) Not available in TEF6635.

Fig 1. Functional diagram

6. Pinning information

6.1 Pinning

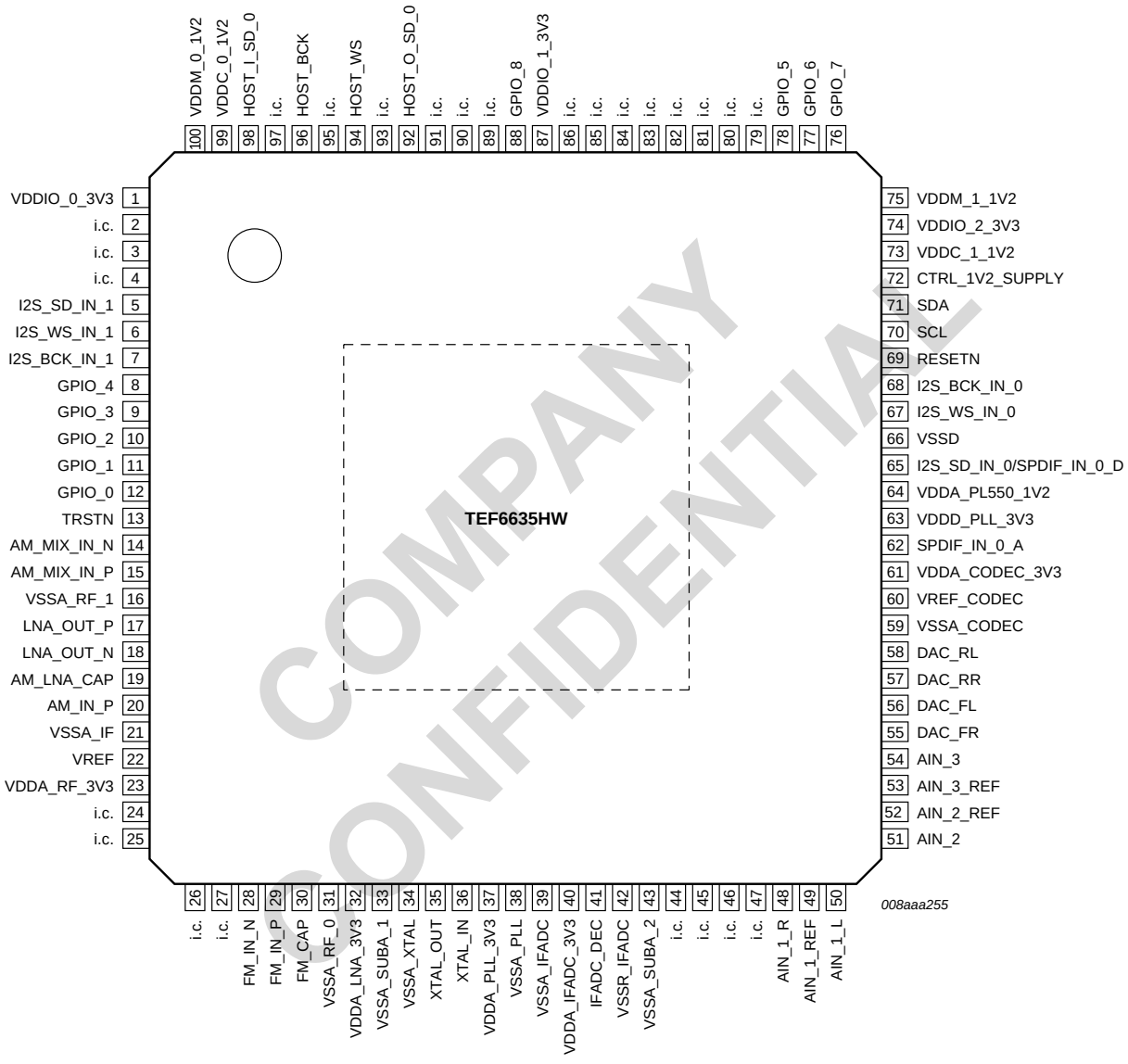


Fig 2. Pin configuration for TEF6635HW

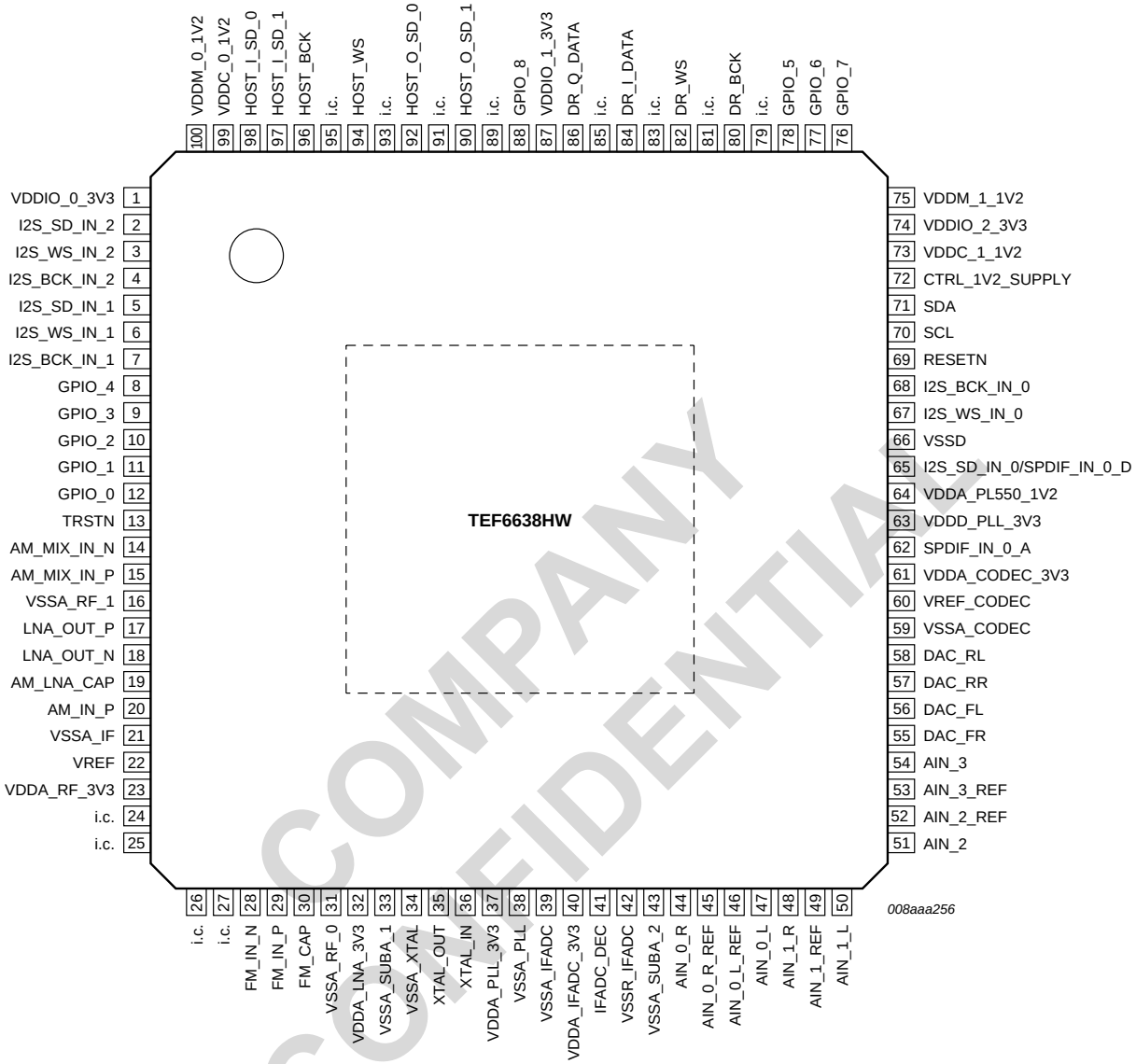


Fig 3. Pin configuration for TEF6638HW

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Pull-up or pull-down[1]	Type[2]	Description
VDDIO_0_3V3	1	-	VDDE	I/O supply voltage 0 (3.3 V)
I2S_SD_IN_2[3]	2	D	I2SRX	I^2S serial data input source 2
I2S_WS_IN_2[3]	3	D	I2SRX	I^2S word select input source 2
I2S_BCK_IN_2[3]	4	D	I2SRX	I^2S bit clock input source 2
I2S_SD_IN_1	5	D	I2SRX	I^2S serial data input source 1
I2S_WS_IN_1	6	D	I2SRX	I^2S word select input source 1
I2S_BCK_IN_1	7	D	I2SRX	I^2S bit clock input source 1
GPIO_4	8	D	SACBSR	General Purpose Input Output (GPIO) 4
GPIO_3	9	D	SACBSR	GPIO 3
GPIO_2	10	D	SACBSR	GPIO 2
GPIO_1	11	D	SACBSR	GPIO 1
GPIO_0	12	U	SACBSR	GPIO 0
TRSTN	13	U	SACBSZ50CMR3H	test reset input (active LOW)
AM_MIX_IN_N	14	-	APIO3V3	negative AM mixer input
AM_MIX_IN_P	15	-	APIO3V3	positive AM mixer input
VSSA_RF_1	16	-	SUPCO3V3	RF 1 analog ground supply voltage
LNA_OUT_P	17	-	APIO3V3	positive AM LNA output
LNA_OUT_N	18	-	APIO3V3	negative AM LNA output
AM_LNA_CAP	19	-	APIO3V3	AM LNA AGC capacitor
AM_IN_P	20	-	APIO3V3	positive AM LNA input
VSSA_IF	21	-	VSSE	IF analog ground supply voltage
VREF	22	-	APIO3V3	reference voltage decoupling
VDDA_RF_3V3	23	-	VDDE	RF analog supply voltage (3.3 V)
i.c.	24	-	APIO3V3	internally connected; leave open
i.c.	25	-	APIO3V3	internally connected; leave open
i.c.	26	-	APIO3V3	internally connected; leave open
i.c.	27	-	APIO3V3	internally connected; leave open
FM_IN_N	28	-	APIO3V3	negative FM RF input
FM_IN_P	29	-	APIO3V3	positive FM RF input
FM_CAP	30	-	APIO3V3	FM AGC capacitor
VSSA_RF_0	31	-	SUPCO3V3	RF 0 analog ground supply voltage
VDDA_LNA_3V3	32	-	SUPCO3V3	LNA analog supply voltage (3.3 V)
VSSA_SUBA_1	33	-	VSSCO2V5	analog ground connection 1
VSSA_XTAL	34	-	VSSCO2V5	crystal analog ground supply voltage
XTAL_OUT	35	-	APIO3V3	crystal oscillator output
XTAL_IN	36	-	APIO3V3	crystal oscillator input
VDDA_PLL_3V3	37	-	SUPCO3V3	synthesizer Phase-Locked Loop (PLL) analog supply voltage (3.3 V)
VSSA_PLL	38	-	VSSCO2V5	synthesizer PLL analog ground supply voltage

Table 2. Pin description *...continued*

Symbol	Pin	Pull-up or pull-down[1]	Type[2]	Description
VSSA_IFADC	39	-	SUPCO3V3	IF ADCs analog ground supply voltage
VDDA_IFADC_3V3	40	-	SUPCO3V3	IF ADCs analog supply voltage (3.3 V)
IFADC_DEC	41	-	APIO3V3	IF ADC decoupling
VSSR_IFADC	42	-	APIO3V3	IF ADC ground supply reference
VSSA_SUBA_2	43	-	APIO3V3	analog ground connection 2
AIN_0_R[3]	44	-	APIO5V6PP	right channel audio input 0
AIN_0_R_REF[3]	45	-	APIO5V6PP	right common-mode reference audio input 0
AIN_0_L_REF[3]	46	-	APIO5V6PP	left common-mode reference audio input 0
AIN_0_L[3]	47	-	APIO5V6PP	left channel audio input 0
AIN_1_R	48	-	APIO5V6PP	right channel audio input 1
AIN_1_REF	49	-	APIO5V6PP	common-mode reference audio input 1
AIN_1_L	50	-	APIO5V6PP	left channel audio input 1
AIN_2	51	-	APIO5V6PP	analog audio input 2
AIN_2_REF	52	-	APIO5V6PP	common-mode reference audio input 2
AIN_3_REF	53	-	APIO5V6PP	common-mode reference audio input 3
AIN_3	54	-	APIO5V6PP	analog audio input 3
DAC_FR	55	-	APIO3V3	audio output for front-right speaker
DAC_FL	56	-	APIO3V3	audio output for front-left speaker
DAC_RR	57	-	APIO3V3	audio output for rear-right speaker
DAC_RL	58	-	APIO3V3	audio output for rear-left speaker
VSSA_CODEC	59	-	VSSE	codec analog ground supply voltage
VREF_CODEC	60	-	APIO3V3	codec reference voltage
VDDA_CODEC_3V3	61	-	VDDEBFX	codec analog supply voltage (3.3 V)
SPDIF_IN_0_A	62	-	APIO3V3	SPDIF analog input source 0
VDDD_PLL_3V3	63	-	SUPCO3V3	synthesizer PLL digital supply voltage (3.3 V)
VDDA_PL550_1V2	64	-	SUPCO2V5	clock PLL analog supply voltage (1.2 V)
I2S_SD_IN_0/SPDIF_IN_0_D	65	D	I2SRX	I^2S serial data input source 0/SPDIF digital input source 0
VSSD	66	-	not applicable	digital ground supply voltage
I2S_WS_IN_0	67	D	I2SRX	I^2S word select input source 0
I2S_BCK_IN_0	68	D	I2SRX	I^2S bit clock input source 0
RESETN	69	U	SACBSZ50CMR3H	system reset input (active LOW)
SCL	70	U	IIC3M4SCL	I^2C-bus serial clock input
SDA	71	U	IIC3M4SCL	I^2C-bus serial data input and output
CTRL_1V2_SUPPLY	72	-	APIO3V3	control output for 1.2 V supply circuit
VDDC_1_1V2	73	-	SUPI	core supply voltage 1 (1.2 V)
VDDIO_2_3V3	74	-	VDDE	I/O supply voltage 2 (3.3 V)
VDDM_1_1V2	75	-	SUPCO2V5	memory supply voltage 1 (1.2 V)
GPIO_7	76	D	SACBSR	GPIO 7
GPIO_6	77	D	SACBSR	GPIO 6

Table 2. Pin description *...continued*

Symbol	Pin	Pull-up or pull-down[1]	Type[2]	Description
GPIO_5	78	D	SACBSR	GPIO 5
i.c.	79	D	SACBSR	internally connected; leave open
DR_BCK[3]	80	D	SACBSR	digital radio bit clock output
i.c.	81	D	SACBSR	internally connected; leave open
DR_WS[3]	82	D	SACBSR	digital radio word select output
i.c.	83	D	SACBSR	internally connected; leave open
DR_I_DATA[3]	84	D	SACBSR	digital radio I-signal serial data output
i.c.	85	D	SACBSR	internally connected; leave open
DR_Q_DATA[3]	86	D	SACBSR	digital radio Q-signal serial data output
VDDIO_1_3V3	87	-	VDDE	I/O supply voltage 1 (3.3 V)
GPIO_8	88	D	SACBSR	GPIO 8
i.c.	89	U	SACBSR	internally connected; leave open
HOST_O_SD_1[3]	90	U	SACBSR	host I^2S output serial data source 1
i.c.	91	U	SACBSR	internally connected; leave open
HOST_O_SD_0	92	D	SACBSR	host I^2S output serial data source 0
i.c.	93	U	SACBSR	internally connected; leave open
HOST_WS	94	U	SACBSR	host I^2S word select output
i.c.	95	U	SACBSR	internally connected; leave open
HOST_BCK	96	U	SACBSR	host I^2S bit clock output
HOST_I_SD_1[3]	97	D	I2SRX	host I^2S input serial data source 1
HOST_I_SD_0	98	D	I2SRX	host I^2S input serial data source 0
VDDC_0_1V2	99	-	SUPI	core supply voltage 0 (1.2 V)
VDDM_0_1V2	100	-	SUPCO2V5	memory supply voltage 0 (1.2 V)

[1] D means internal weak pull-down of 50 kΩ and U means internal weak pull-up of 50 kΩ.

[2] The pin types are defined in Table 3.

[3] This pin is internally connected for the TEF6635 and should be left open. The function is only available in TEF6638.

Table 3. Pin type description

Type	Description
APIO3V3	analog I/O cell; general purpose analog I/O buffer for signals up to 3.6 V
APIO5V6PP	analog I/O cell; maximum input voltage of 2 V (RMS) or 5.6 V (p-p)
I2SRX	virtual ground input to receive I^2S signals through a 10 kΩ external resistor in series
IIC3M4SCL	I^2C-bus cell supporting fast mode (400 kbit/s); compliant with *The I^2C-bus Specification, Version 2.1*; push-pull/open-drain driver; input with hysteresis and pulse filter; fail-safe: when the device is not powered the I/O pins connected to the I^2C-bus are floating and do not disturb the I^2C-bus lines
SACBSR	digital I/O cell with slew rate control; supporting 3.3 V signaling; output driver design for Printed-Circuit Board (PCB) trace impedances in the range of 45 Ω to 80 Ω; indicative maximum frequency 38 MHz
SACBSZ50CMR3H	digital I/O cell; supporting 3.3 V signaling; output driver design for PCB trace impedances in the range of 45 Ω to 80 Ω; indicative maximum frequency 187 MHz
SUPCO2V5	2.5 V analog core supply and ground combination cell
SUPCO3V3	3.3 V analog core supply and ground combination cell
SUPI	I/O and core supply and combination cell for 3.3 V I/O sections
VDDE	core supply cell for 3.3 V I/O sections
VDDEBFX	1.2 V I/O and core internal supply cell for 3.3 V I/O sections
VSSCO2V5	I/O and core external ground cell
VSSE	I/O and core external ground cell

7. Functional description

7.1 FM tuner to IF ADC input

The RF input signal from the antenna is first filtered by an external wideband band-pass RF filter. The RF filter passes the complete FM band of interest and takes care of antenna impedance matching.

After filtering, the RF signal is applied to the high dynamic range FM LNA of TEF663x. The gain of the LNA is reduced by the integrated AGC loop in 7 steps of 6 dB. The input impedance of the LNA, and total receiver application, remains constant for the first 5 AGC steps. The input impedance is reduced for the last 2 AGC steps. Due to the high dynamic range of the FM LNA, and the large integrated AGC range, there is no need for an external LNA or external components as PIN diodes for AGC.

The signal from the LNA is converted to a low IF using a complex mixer. The mixer includes image rejection and Local Oscillator (LO) harmonic rejection for the 3rd and 5th LO harmonics. This reduces the requirements of the RF filter attenuation.

The IF signal from the mixer is amplified and filtered and then digitized by the IF ADC.

7.2 AM tuner to IF ADC input

The RF input signal from the antenna is first filtered by an external high-pass filter and an FM frequency band reject filter. The high-pass filter provides attenuation of 50 Hz/60 Hz signals from power lines. The band reject filter or FM intrusion filter attenuates the FM signals before entering the AM LNA potentially causing intermodulation.

After filtering the RF signal is applied to the AM LNA. The gain of the AM LNA can be reduced by the integrated AGC loop in 10 steps of 6 dB. The input capacitance of the AM LNA is constant over the complete AGC range.

The output signal of the LNA is filtered before being applied to the complex mixer. In AM MW mode the filter is a tuned band-pass filter consisting of two external coils and an integrated tuned capacitor bank. The capacitor bank is automatically calibrated during a tuning action in the AM MW band. The filter between LNA output and mixer input is switched to a high-pass filter characteristic in AM SW and to a low-pass filter characteristic in AM LW. The mixer converts the RF frequency from MW and SW to a low IF, including image rejection and LO harmonic rejection for the 3rd and 5th harmonics of the LO. In LW mode, the mixer is set in bypass mode and passes the LW RF frequency to the IF amplifier.

The IF signal from the mixer is amplified and filtered before the IF signal is digitized by the IF ADC.

7.3 Tuning system

The PLL tuning system provides the LO signal to drive the AM and FM mixer for frequency conversion to low IF. The tuning system is capable of tuning to the US, European, Japanese, and OIRT FM bands and the AM LW, MW and full SW bands. The tuning system is fully integrated and highly digitized, combining low phase noise and fast tuning times.

7.4 IF ADC

The IF signal is digitized by a high dynamic range sigma-delta IF ADC. Due to the high dynamic range, there is no need for narrowband IF filtering which improves FM stereo performance, AM noise blanking and HD Radio reception. The IF ADC provides two bitstreams to the radio signal processing unit.

7.5 Radio processing

The radio processing performs the following functions:

- Decimation of the IF ADC bitstreams
- Shift to baseband
- AGC compensation
- Linear AGC detection and control
- I/Q error correction
- Interface to terrestrial digital radio processor for HD Radio signals or DRM reception
- Channel filtering
- Received Signal Strength Indicator (RSSI) detection
- AM/FM demodulation
- Ignition noise detection and correction
- FM stereo decoding
- Programmable de-emphasis
- Quality detection
- Weak signal handling
- RDS/RBDS demodulation, decoding and error correction

The output of the radio signal processing unit is a left and right digital audio signal.

7.5.1 AM mode features

The AM radio signal processing includes algorithms to improve the signal quality in difficult reception conditions.

Adjacent channels are rejected by the channel filter. The bandwidth of the channel filter can be programmed.

The TEF6638 contains optional automatic bandwidth control of the channel filter (AM PACS).

Ignition noise pulses are suppressed by the AM noise blanker, consisting of a noise blanker at IF in front of the channel filter and at audio after AM demodulation.

The quality of the signal reception is measured by the following quality detectors:

- RSSI or field strength detection (LEVEL)
- Frequency offset detection
- AM modulation detection
- Adjacent channel detection (TEF6638)

The signal quality in weak reception conditions is improved by the AM weak signal handling:

- Soft mute controlled by LEVEL
- High-cut controlled by LEVEL and modulation
- Soft mute controlled by modulation (TEF6638)
- Low-cut controlled by the high-cut signal (TEF6638)

7.5.2 FM mode features

The FM radio signal processing includes algorithms to improve the signal quality in difficult reception conditions.

Channels which are adjacent to the desired signal are rejected by the channel filter. The bandwidth of the channel filter is dynamically controlled (FM PACS). It depends on the adjacent channel conditions and the properties of the desired signal such as modulation and signal strength.

Ignition noise pulses are suppressed by the noise blanker. The noise blanker detects the noise pulses and blanks the pulses in the MultiPleX (MPX) signal.

The quality of the signal reception is measured by the following quality detectors:

- RSSI or field strength detection (LEVEL)
- Frequency offset detection
- Multipath and adjacent channel detection by UltraSonic Noise (USN) detection
- Multipath detection by Wideband AM (WAM) detection
- Frequency deviation by modulation detection
- Stereo pilot detection
- Pause detection (TEF6638)

The signal quality in weak reception and multipath conditions is improved by the weak signal handling function containing:

- Soft mute controlled by LEVEL, USN and WAM
- High-cut controlled by LEVEL, USN, WAM and modulation
- Stereo blend controlled by LEVEL, USN, WAM and modulation
- High blend controlled by LEVEL, USN, WAM and modulation (TEF6638)
- Low-cut controlled by the high-cut signal (TEF6638)

The TEF6638 further contains the following features: Click Noise Suppression (CNS), Enhanced Multipath Suppression (EMS) and optionally Channel EQualization (CEQ).

7.5.3 RDS/RBDS

The TEF6635 and the TEF6638 include a demodulator and a newly developed decoder for data reception of RDS and RBDS transmission with improved performance.

7.5.3.1 RDS demodulator

The RDS demodulator includes optimized filtering and linear signal processing that allows very good RDS sensitivity. The MPX signal is filtered for selection of the 57 kHz RDS signal and data shaping. The RDS demodulator data is fed into the RDS decoder for further processing. To support available software stacks, the RDS demodulator data can also be read out directly via I^2C-bus or GPIO pins.

7.5.3.2 RDS decoder

The RDS decoder provides synchronization to the block and group structure of the demodulated RDS data stream. When synchronized, the decoder delivers data in a fixed ABCD group order for easy software handling. A synchronization search continues in the background for fast correction on bit slip or other synchronization errors. When compared to earlier designs, extended error detection and correction allows a 60 % increase of 2-bit corrected blocks, without sacrificing reliability.

An I^2C-bus read bit signals the availability of new group data. When the interrupt signal is active, an interrupt signal 'data available' is provided on one of the GPIO pins.

'Data available' is flagged whenever a new group is received (i.e. at reception of block D). However, for fastest information, 'data available' is already flagged at synchronization start after the reception of the first Programme Identification (PI) code (i.e. block A or block C').

7.5.4 Baseband I^2S output

For HD Radio and DRM reception with the TEF6638, the baseband signal is provided to an external digital radio coprocessor, such as the NXP SAF356x. The baseband I^2S output includes a Bit Clock (BCK), Word Select (WS), I-data and Q-data signals. The BCK and WS frequencies are defined by the TEF6638. The digital radio coprocessor will slave to the baseband I^2S signal.

7.6 Audio input

Several types of analog and digital audio sources can be connected to the audio DSP. The analog inputs support:

- one stereo input with ground input for common-mode rejection (AUX), that can also be configured as a single-ended stereo input
- two mono inputs each with ground input for common-mode rejection (navigation, phone). The inputs can also be configured as differential or single-ended mono inputs. Alternatively, they can be used as one differential stereo input, that can also be configured as a stereo input with ground input for common-mode rejection or as single-ended stereo input

A source selector connects the analog inputs to a stereo ADC.

TEF6638 provides one additional differential stereo input (audio bus). This input can be configured either as a stereo input with ground input for common-mode rejection or as a single-ended stereo input. It is connected to a second stereo ADC.

In addition, two (TEF6635) or three (TEF6638) digital audio input ports are available using the I^2S format. Each I^2S input can have a different sample rate and a different clock phase to the others (asynchronous). Alternatively input port IN0 (pin 65) can be configured as an input of the digital SPDIF signal. A separate analog SPDIF input is also available.

All independent digital audio input streams pass the audio Sample Rate Converter (SRC) to convert the incoming data streams to the system output sample rate.

In addition to the asynchronous inputs, either one (TEF6635) or two (TEF6638) synchronous digital audio input ports can be used (pins HOST_I_SD_0 and HOST_I_SD_1).

The I^2S input and output interfaces are compliant with the *I^2S specification, Revision June 5, 1996*. The I^2S specification allows data to be written with the falling or rising edge of the bit clock (BCK). For the safest timing, it is recommended to use the falling edge on BCK to write data (SD) and word select (WS).

7.7 Digital audio processing

The audio processing provides the following features:

Input source specific processing:

- Compact Disc (CD) de-emphasis
- HD Radio blending (TEF6638)

Primary channel functions:

- Source scaling
- DC filter
- Sound adjustment (treble, mid, bass, volume, balance and fader)
- Soft audio mute
- Individual channel mute
- Individual channel gain
- Limiter
- Bass boost or loudness
- Dynamic range compressor and expander
- Parametric equalizer - front and rear: modules of 2 times 7 bands, center and subwoofer are configurable up to eighth-order Infinite Impulse Response (IIR) filter
- 5 band graphic equalizer
- Superposition of phone, navigation or chime generator signals
- 6 channel delay line

Secondary channel functions:

- Source scaling
- DC filter
- Sound adjustment (treble, mid, bass, volume, balance and fader)
- Soft audio mute

- Individual channel gain
- Limiter

Special functions:

- Dedicated signal paths for phone and navigation channel containing two second-order filters, smoothed volume control and mute
- Chime generator or double Park Distance Control (PDC) generator
- Optional polyphonic chime generator
- Wave-table based click-clack sound generator
- Noise or sine generator
- Four mono and three stereo second-order general-purpose filters
- Level detector
- Graphical spectrum analyzer

7.8 Audio output

The audio output includes two stereo DACs to generate the front and rear output signals with optional rear seat entertainment. Additional channels, such as subwoofer and center channels, can be output via the HOST_O pins.

7.9 IC control unit

The IC control unit takes control of the internal clock generation, the reset sequence, the power control and the programming interface of the whole system.

7.9.1 Crystal oscillator

The reference clock for the TEF6635 and TEF6638 system is provided by a Pierce crystal oscillator running at 62.4 MHz. The crystal oscillator can be used with a fundamental mode crystal or a third overtone crystal. For the fundamental mode, a crystal and two Pierce load capacitors are required in the application. In applications using a third overtone crystal, an additional series LC circuit is required to suppress oscillation at the fundamental frequency.

7.9.2 Reset

The reset generator controls the start-up sequence of all units and ensures that all processing units will be set to a defined state during and after the reset phase.

7.9.3 Clock generator

The clock generator supplies the various processing units with the correct clocks.

7.9.4 I^2C-bus

The I^2C-bus is the central communication interface between the TEF6635 or the TEF6638 system and the outside world (host microcontroller). All system access and control is handled by the I^2C-bus interface. The TEF6635 and the TEF6638 offer straight forward control and support of tuning actions. Switching between the different operational modes is handled internally.

The I²C-bus interface supports 400 kbit/s (fast mode) according to *The I²C-bus Specification, Version 2.1* and *User Manual Rev. 03, 19 June 2007.*

Exception to the I²C-bus specification:

- The host generates start, repeated start and stop conditions only, immediately after a full transmission of a complete byte including acknowledge (ACK).
- The data hold time ($t_{HD;DAT}$) must be at least 30 ns.
- The input levels of the receiver are with respect to $V_{DDD(3V3)}$ and not related to the I²C-bus voltage.

The I²C-bus device address is determined by reading the voltage levels at pins HOST_BCK (DA1) and HOST_WS (DA2) during startup (see Figure 4).

A logic 0 requires a 10 kΩ pull-down resistor to ground, whereas for a logic 1, the pins can be left open (internal pull-up) or connected to the 3.3 V supply voltage using a 10 kΩ pull-up resistor.

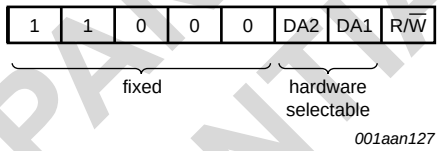


Fig 4. Slave address

7.9.5 Voltage regulator

The voltage regulator generates a 1.2 V supply for TEF6635 and TEF6638 and consists of an internal control loop and an external NPN transistor to handle the power. This voltage regulator allows the TEF6635 and TEF6638 to use a single 3.3 V power supply.

7.10 Default pin assignment for GPIO functions

Table 4. GPIO pin assignment

Description	Direction	GPIO	IC pin
HD Radio signal/FM blend[1]	input	5	78
Baseband frequency selection[1]	output	6	77
RDS data RDDA[2]	output	0	12
RDS clock RDCL[2]	output	1	11
RDS data available[2]	output	0	12
Amplifier clip 0	input	7	76
Amplifier clip 1 and 2	input	8	88
Fast RF quality change[2]	output	0	12
Click-clack control	input	4	8
Fast mute	input	2	10

[1] Function only available for TEF6638.

[2] RDS demodulator outputs RDDA and RDCL are mutually exclusive with interrupt output RDS data available.

8. I²C-bus protocol

8.1 Write mode

Table 5. Device address

7	6	5	4	3	2	1	0
1	1	0	0	0	DA2	DA1	0 (write)

Table 6. Device address description

Bit	Symbol	Description
2 and 1	DA[2:1]	The device address is defined by the application of pins HOST_WS (= DA2) and HOST_BCK (= DA1); pull down to ground = '0', floating pin = '1'. The device address is determined when power is applied to the device.

Table 7. Subaddress

7	6	5	4	3	2	1	0
SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0

Table 8. Subaddress description

Bit	Symbol	Description
7 to 0	SA[7:0]	00h = allows tuning action mode definition and may be combined with I²C write of subaddress 03h and higher
		03h or higher = standard I²C write without tuning action
		01h to 1Fh = direct FM/AM radio control range[1]
		20h to 3Fh = direct audio control range
		40h to 9Fh = reserved
		A0h to BFh = audio special feature range
		C0h to DFh = system and radio special feature range
		E0h = read back of write data
		E1h = keycode for optional features
		E2h to F1h = reserved
		F2h = LOW level control of audio DSP
		F3h to FFh = reserved

[1] FM and AM settings are stored separately within the device and controlled by BAND (00h).

Remark: Unused data bits are reserved and should be written with the indicated bit value (generally 0) for future compatibility.

Table 9. MODE - data byte 0h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	MODE2	MODE1	MODE0	-	-	BAND1	BAND0
Reset	0	0	0	0	0	0	0	0

Table 10. MODE - data byte 0h bit description

Bit	Symbol	Description
6 to 4	MODE[2:0]	tuning action
		000 = Standby: reduced power mode, disabled radio and audio functionality
		001 = Preset mode: tune to new program with short mute time
		010 = Search mode: tune to new program and stay muted (allowing for stop quality check)
		011 = FM AF Update mode: tune to AF program, store quality and tune back including inaudible mute
		100 = FM Jump mode: tune to AF program with inaudible short mute time
		101 = FM Check mode: tune to AF program and stay muted (allowing quality and RDS PI check)
		110 = reserved
		111 = End mode: release mute of Search or Check mode action
1 to 0	BAND[1:0]	tuning band selection
		00 = FM world
		01 = AM LW
		10 = AM MW
		11 = AM SW

Remark: The device is in power-down mode (idle mode) after the supply power is applied and it is powered-up by transmitting a Preset or Search tuning action (MODE = 1 or 2). MODE = 0 puts the device in power saving standby mode (radio and audio function disabled, settings remain). Default MODE controls all power setting, however APWR (data byte 3Fh) allows independent control of audio power.

Remark: Audio use-case (USE, data byte 3Fh) can be changed only during initialization, i.e. before first power-up. Audio special feature control (A6h, A9h) and audio low-level control (F2h) have to be transmitted after power-up. I^2C data bytes 00h to 3Dh and radio configuration (C9h) may be transmitted at any time. FM and AM settings are controlled depending on the BAND setting and are available during initialization or standby.

Table 11. FREQ_M - data byte 01h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	FREQ14	FREQ13	FREQ12	FREQ11	FREQ10	FREQ9	FREQ8
Reset	0	0	1	0	0	0	1	0

Table 12. FREQ_L - data byte 02h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FREQ7	FREQ6	FREQ5	FREQ4	FREQ3	FREQ2	FREQ1	FREQ0
Reset	1	1	1	0	0	0	1	0

Table 13. FREQ - data byte 01h and 02h bit description

Bit	Symbol	Description
14 to 0	FREQ[14:0]	tuning frequency
		6500 to 10800 = 65 MHz to 108 MHz = FM reception frequency in 10 kHz steps
		144 to 288 = 144 kHz to 288 kHz = AM LW reception frequency in 1 kHz steps
		522 to 1710 = 522 kHz to 1710 kHz = AM MW reception frequency in 1 kHz steps
		2300 to 27000 = 2300 kHz to 27000 kHz = AM SW reception frequency in 1 kHz steps

Remark: For a proper tuning result, a change in BAND or FREQ should always be combined with a tuning action of MODE = 1 to 5. Also a tuning action with mode = 1 to 5 (data byte 00h) should include data bytes 01h and 02h (FREQ) within the same transition. Changing BAND is as easy as changing frequency; a tuning action (Preset) with the desired BAND and FREQ setting.

Table 14. TUNER - data byte 03h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RFAGC1	RFAGC0	-	-	BW3	BW2	BW1	BW0
Reset	0	0	0	0	0	0	0	0

Table 15. TUNER - data byte 03h bit description

Bit	Symbol	Description
7 and 6	RFAGC[1:0]	RFAGC wideband threshold
		00 = start of RFAGC: FM: 92 dBμV AM: 97 dBμV
		01 = start of RFAGC: FM: 89 dBμV AM: 94 dBμV
		10 = start of RFAGC: FM: 86 dBμV AM: 91 dBμV
		11 = start of RFAGC: FM: 83 dBμV AM: 88 dBμV
3 to 0	BW[3:0]	bandwidth control
		0000 = dynamic mode (best bandwidth is selected depending on the reception condition)
		0001 to 1111 = narrow to wide bandwidth FM: 72 kHz to 300 kHz (double sided BW) FM default: BW = 0; for AFU tuning BW = 8 AM: 2.4 kHz to 14.0 kHz (double sided BW); AM default BW = 9

Remark: When controlled together with an FM, AFU tuning (MODE = 3) bandwidth is active for the AFU sampling only. AFU bandwidth may be set equal to standard BW or it may be fixed (1 to 15) whereas standard BW is dynamic (0). AM dynamic bandwidth mode (BW = 0) is an optional key-coded feature available in TEF6638.

Table 16. TUNER_OPT - data byte 04h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	ANT	ATT2	ATT1	ATT0	-	-	-	-
Reset	0	0	0	0	0	0	0	0

Table 17. TUNER_OPT - data byte 04h bit description

Bit	Symbol	Description
7	ANT	AM antenna type: ANT may be selected during initialization or standby (otherwise change is only active after a band change from FM to AM)
		0 = AM passive antenna (high-impedance)
		1 = AM active antenna (low impedance allowed)
6 to 4	ATT[2:0]	AM antenna attenuation: ATT may be selected during initialization or standby (otherwise change is only active after a tuning action). Attenuation may be desired for an active antenna to avoid unnecessary AGC control during normal signal conditions
		000 to 111 = AM 0 dB attenuation (full AGC range) to 42 dB attenuation (restricted AGC range)

Table 18. RADIO - data byte 05h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	EMS	CNS	CE	-	NBSA1	NBSA0	NBSB1	NBSB0
Reset	0	1	0	0	1	0	1	0

Table 19. RADIO - data byte 05h bit description

Bit	Symbol	Description
7	EMS	enhanced multipath suppression[1]
		0 = FM no enhanced multipath suppression
		1 = FM enhanced multipath suppression system
6	CNS	click noise suppression[1]
		0 = no click noise suppression
		1 = click noise suppression enabled
5	CE	channel equalizer[1][2]
		0 = FM no channel equalizer
		1 = FM channel equalizer; adaptive reception filter
3 and 2	NBSA[1:0]	noise blanker sensitivity A
		00 = noise blanker off (FM or AM IF)
		01 to 11 = noise blanker sensitivity low to high (FM or AM IF)
1 and 0	NBSB[1:0]	noise blanker sensitivity B
		00 = AM audio noise blanker off
		01 to 11 = AM audio noise blanker sensitivity low to high

[1] Feature is not available in TEF6635.

[2] For exceptions in concurrent use of the FM features CNS, EMS and CEQ together, please refer to the radio user manual.

Table 20. SIGNAL - data byte 06h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MONO	DIRAD	-	-	FLOC1	FLOC0	DEMP1	DEMP0
Reset	0	0	0	0	0	0	0	1

Table 21. SIGNAL - data byte 06h bit description

Bit	Symbol	Description
7	MONO	FM mono
		0 = FM stereo enabled
		1 = FM forced mono
6	DIRAD	digital radio[1]
		baseband I^2S output, HD-blend input and Host I^2S input signals are enabled by DIRAD = 1. In case of direct Host I^2S input control (A9h 14h or A9h 15h), DIRAD control over Host I2S is disabled
		0 = analog radio only
		1 = digital radio I/O and blend (GPIO5) active
3 and 2	FLOC[1:0]	fixed low cut audio filter
		00 = FM high pass: no limit / AM high pass: 20 Hz
		01 = FM high pass: reserved / AM high pass: 50 Hz
		10 = FM high pass: reserved / AM high pass: 100 Hz
		11 = FM high pass: reserved / AM high pass: 200 Hz
1 and 0	DEMP[1:0]	de-emphasis
		00 = FM de-emphasis: off / AM low pass: 5 kHz
		01 = FM de-emphasis: 50 µs / AM low pass: 3 kHz
		10 = FM de-emphasis: 75 µs / AM low pass: 2 kHz
		11 = FM de-emphasis: reserved / AM low pass: 1.5 kHz

[1] Function not available in TEF6635.

Table 22. BWCTRL - data byte 07h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	BWS1	BWS0	BWLEV1	BWLEV0
Reset	0	0	0	0	0	1	0	1

Table 23. BWCTRL - data byte 07h bit description

Bit	Symbol	Description
3 and 2	BWS[1:0]	FM dynamic bandwidth control preference
		00 to 11 = modulation handling (wide bandwidth) to adjacent channel suppression (narrow bandwidth)
1 and 0	BWLEV[1:0]	FM dynamic bandwidth control preference at low level
		00 to 11 = modulation handling (wide bandwidth) to noise reduction (narrow bandwidth)

Table 24. SPECIAL - data byte 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	QSI2	QSI1	QSI0	-	-	-	-	AFUP
Reset	0	0	0	0	0	0	0	0

Table 25. SPECIAL - data byte 08h bit description

Bit	Symbol	Description
7 to 5	QSI[2:0]	quality status interrupt[1]
		000 = no interrupt
		001 to 111 = interrupt signal on QRS state (active low at GPIO_0, until I^2C read)
0	AFUP	AFU on pause[2]
		0 = FM standard
		1 = FM delayed AF-Update (MODE = 3) action until “pause” (low modulation)

[1] Multiple interrupts may be output together at GPIO_0 depending on the setting of QSI and RDO (data byte 09h). The status information of QRS and RDAV (read byte 00h) informs about the available interrupt(s).

[2] Function not available in TEF6635.

Table 26. RDS - data byte 09h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	NWSY	TUSY	RBDS	-	-	RDO1	RDO0	RDSM
Reset	0	1	0	0	0	0	0	1

Table 27. RDS - data byte 09h bit description

Bit	Symbol	Description
7	NWSY	new synchronisation (manual RDS start)
		0 = standard operation
		1 = restart RDS (bit NWSY automatically defaults to 0)
6	TUSY	tuning synchronisation (automatic RDS start)
		0 = no automatic RDS reset
		1 = restart RDS automatically after tuning for fast results
5	RBDS	modified mobile search (MMBS) allowance
		0 = RDS (no E blocks accepted)
		1 = RBDS (E blocks accepted)
2 to 1	RDO[1:0]	RDS pin options[1]
		00 = no RDS pin use
		01 = RDS demodulator continuous data output (RDCL, RDDA at GPIO_1, GPIO_0)
		10 = data available interrupt signal (active Low at GPIO_0); demodulator or decoder
		11 = reserved

Table 27. RDS - data byte 09h bit description *...continued*

Bit	Symbol	Description
0	RDSM	RDS mode
		0 = demodulator data via I^2C read
		1 = decoder RDS group data via I^2C read

[1] Multiple interrupts may be output together at GPIO_0 depending on the setting of QSI (data byte 08h) and RDO. The status information of QRS and RDAV (read byte 00h) indicates the available interrupt(s).

Table 28. RESERVED0 data byte 0Ah

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

Table 29. RESERVED1 data byte 0Bh

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

Table 30. LEVEL_OFFSET - data byte 0Ch bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	LEVO5	LEVO4	LEVO3	LEVO2	LEVO1	LEVO0
Reset	0	0	1	1	0	0	0	0

Table 31. LEVEL_OFFSET - data byte 0Ch bit description

Bit	Symbol	Description
5 to 0	LEVO[5:0]	level offset can be used to correct for antenna gain and is included in the weak signal handling and the I^2C LEV read
		000000 to 111111 = –48 dB to +15 dB correction of level voltage (LEVO – 48 dB)

8.1.1 Soft mute weak signal handling

Table 32. SOFTMUTE_TIME - data byte 0Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MFT2	MFT1	MFT0	MAT2	MAT1	MAT0	MDT1	MDT0
Reset	0	1	1	0	0	1	0	1

Table 33. SOFTMUTE_TIME - data byte 0Dh bit description

Bit	Symbol	Description
7 to 5	MFT[2:0]	soft mute fast time (FM mode)
		000 = 1 ms fast attack and decay time
		001 = 2 ms fast attack and decay time
		010 = 4 ms fast attack and decay time
		011 = 8 ms fast attack and decay time
		100 = 15 ms fast attack and decay time
		101 = 30 ms fast attack and decay time
		110 = 60 ms fast attack and decay time
		111 = 120 ms fast attack and decay time
4 to 2	MAT[2:0]	soft mute slow attack time
		000 = 60 ms slow attack time
		001 = 120 ms slow attack time
		010 = 250 ms slow attack time
		011 = 500 ms slow attack time
		100 = 1000 ms slow attack time
1 and 0	MDT[1:0]	soft mute slow decay time
		00 = 2 times the soft mute slow attack
		01 = 4 times the soft mute slow attack
		10 = 8 times the soft mute slow attack
		11 = 16 times the soft mute slow attack

Table 34. SOFTMUTE_DET - data byte 0Eh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MMOD1	MMOD0	MFOL	MSOL	MFON	MSON	MFOM	MSOM
Reset	0	0	0	1	0	0	0	0

Table 35. SOFTMUTE_DET - data byte 0Eh bit description

Bit	Symbol	Description
7 and 6	MMOD[1:0]	soft mute on modulation[1]
		00 = off
		01 to 11 = weak to strong control on modulation (AM mode)
5	MFOL	soft mute fast on level
		0 = off
		1 = FM fast control on level
4	MSOL	soft mute slow on level
		0 = off
		1 = slow control on level (AM and FM mode)
3	MFON	soft mute fast on noise
		0 = off
		1 = FM fast control on ultrasonic noise

Table 35. SOFTMUTE_DET - data byte 0Eh bit description *...continued*

Bit	Symbol	Description
2	MSON	soft mute slow on noise
		0 = off
		1 = FM slow control on ultrasonic noise
1	MFOM	soft mute fast on multipath
		0 = off
		1 = FM fast control on multipath
0	MSOM	soft mute slow on multipath
		0 = off
		1 = FM slow control on multipath

[1] Function not available in TEF6635.

Table 36. SOFTMUTE_LEV - data byte 0Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	MST3	MST2	MST1	MST0	MSL2	MSL1	MSL0
Reset	0	0	1	1	1	0	1	0

Table 37. SOFTMUTE_LEV - data byte 0Fh bit description

Bit	Symbol	Description
6 to 3	MST[3:0]	soft mute start on level
		0000 to 1111 = late to early start of soft mute on level
		FM: 0 dBμV to 30 dBμV (2 dB step)
		AM: 16 dBμV to 46 dBμV (2 dB step)
2 to 0	MSL[2:0]	soft mute slope on level
		000 = soft mute range on level 30 dB
		001 = soft mute range on level 26 dB
		010 = soft mute range on level 22 dB
		011 = soft mute range on level 18 dB
		100 = soft mute range on level 15 dB
		101 = soft mute range on level 12 dB
		110 = soft mute range on level 9 dB
		111 = soft mute range on level 6 dB

Table 38. SOFTMUTE_N_M - data byte 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	MNS2	MNS1	MNS0	-	MMS2	MMS1	MMS0
Reset	0	0	1	1	0	0	1	1

Table 39. SOFTMUTE_N_M - data byte 10h bit description

Bit	Symbol	Description
6 to 4	MNS[2:0]	soft mute noise sensitivity
		000 to 111 = FM weak to strong control on ultrasonic noise
2 to 0	MMS[2:0]	soft mute multipath sensitivity
		000 to 111 = FM weak to strong control on multipath (wideband AM)

Table 40. SOFTMUTE_LIM - data byte 11h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	MLIM3	MLIM2	MLIM1	MLIM0
Reset	0	0	0	0	1	1	0	0

Table 41. SOFTMUTE_LIM - data byte 11h bit description

Bit	Symbol	Description
3 to 0	MLIM[3:0]	soft mute limit
		0000 to 1111 = soft mute maximum control limit at −40 dB to −10 dB (2 dB step)

8.1.2 High cut weak signal handling

Table 42. HIGHCUT_TIME - data byte 12h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	HFT2	HFT1	HFT0	HAT2	HAT1	HAT0	HDT1	HDT0
Reset	0	1	1	0	1	1	1	0

Table 43. HIGHCUT_TIME - data byte 12h bit description

Bit	Symbol	Description
7 to 5	HFT[2:0]	high cut fast time
		000 = FM 1 ms fast attack and decay time
		001 = FM 2 ms fast attack and decay time
		010 = FM 4 ms fast attack and decay time
		011 = FM 8 ms fast attack and decay time
		100 = FM 15 ms fast attack and decay time
		101 = FM 30 ms fast attack and decay time
		110 = FM 60 ms fast attack and decay time
		111 = FM 120 ms fast attack and decay time
4 to 2	HAT[2:0]	high cut slow attack time
		000 = 60 ms slow attack time
		001 = 120 ms slow attack time
		010 = 250 ms slow attack time
		011 = 500 ms slow attack time
		100 = 1000 ms slow attack time

Table 43. HIGHCUT_TIME - data byte 12h bit description *...continued*

Bit	Symbol	Description
1 and 0	HDT[1:0]	high cut slow decay time
		00 = 2 times the high cut slow attack
		01 = 4 times the high cut slow attack
		10 = 8 times the high cut slow attack
		11 = 16 times the high cut slow attack

Table 44. HIGHCUT_DET - data byte 13h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	HMOD1	HMOD0	HFOL	HSOL	HFON	HSON	HFOM	HSOM
Reset	0	0	1	1	0	1	0	1

Table 45. HIGHCUT_DET - data byte 13h bit description

Bit	Symbol	Description
7 and 6	HMOD[1:0]	high cut on modulation
		00 = off
		01 to 11 = AM weak to strong control on modulation
5	HFOL	high cut fast on level
		0 = off
		1 = FM fast control on level
4	HSOL	high cut slow on level
		0 = off
		1 = (AM and FM mode) slow control on level
3	HFON	high cut fast on noise
		0 = off
		1 = FM fast control on ultrasonic noise
2	HSON	high cut slow on noise
		0 = off
		1 = FM slow control on ultrasonic noise
1	HFOM	high cut fast on multipath
		0 = off
		1 = FM fast control on multipath
0	HSOM	high cut slow on multipath
		0 = off
		1 = FM slow control on multipath

Table 46. HIGHCUT_LEV - data byte 14h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	HST3	HST2	HST1	HST0	HSL2	HSL1	HSL0
Reset	0	0	1	1	0	0	1	1

Table 47. HIGHCUT_LEV - data byte 14h bit description

Bit	Symbol	Description
6 to 3	HST[3:0]	high cut start on level
		0000 to 1111 = late to early start of high cut on level
		FM: 20 dBμV to 50 dBμV (2 dB step)
		AM: 30 dBμV to 60 dBμV (2 dB step)
2 to 0	HSL[2:0]	high cut slope on level
		000 = high cut range on level 30 dB
		001 = high cut range on level 26 dB
		010 = high cut range on level 22 dB
		011 = high cut range on level 18 dB
		100 = high cut range on level 15 dB
		101 = high cut range on level 12 dB
		110 = high cut range on level 9 dB
		111 = high cut range on level 6 dB

Table 48. HIGHCUT_N_M - data byte 15h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	HNS2	HNS1	HNS0	-	HMS2	HMS1	HMS0
Reset	0	0	1	1	0	0	1	1

Table 49. HIGHCUT_N_M - data byte 15h bit description

Bit	Symbol	Description
6 to 4	HNS[2:0]	high cut noise sensitivity
		000 to 111 = FM weak to strong control on ultrasonic noise
2 to 0	HMS[2:0]	high cut multipath sensitivity
		000 to 111 = FM weak to strong control on multipath (wideband AM)

Table 50. HIGHCUT_LIM - data byte 16h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	HFIL	-	HSLIM1	HSLIM0	-	HLIM2	HLIM1	HLIM0
Reset	0	0	0	0	0	0	1	0

Table 51. HIGHCUT_LIM - data byte 16h bit description

Bit	Symbol	Description
7	HFIL	high cut filter type
		0 = low-pass filter with controlled frequency
		1 = low-pass filter with controlled attenuation limit
5 and 4	HSLIM[1:0]	high cut start limit
		00 = unlimited
		01 = 15 kHz high cut minimum control limit
		10 = 10 kHz high cut minimum control limit
		11 = 7 kHz high cut minimum control limit

Table 51. HIGHCUT_LIM - data byte 16h bit description *...continued*

Bit	Symbol	Description
2 to 0	HLIM[2:0]	high cut limit
		000 = 1 kHz[1] or FM 17 dB attenuation[2]
		001 = 1.5 kHz[1] or FM 14 dB attenuation[2]
		010 = 2 kHz[1] or FM 12 dB attenuation[2]
		011 = 2.5 kHz[1] or FM 10 dB attenuation[2]
		100 = 3 kHz[1] or FM 8 dB attenuation[2]
		101 = 4 kHz[1] or FM 6 dB attenuation[2]
		110 = 5 kHz[1] or FM 4.5 dB attenuation[2]
		111 = 7 kHz[1] or FM 3 dB attenuation[2]

[1] high cut maximum control limit (HFIL = 0).

[2] attenuation + 7 kHz frequency limit (HFIL = 1).

Table 52. HIGHCUT_LOC - data byte 17h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	HLOC2	HLOC1	HLOC0
Reset	0	0	0	0	0	1	0	0

Table 53. HIGHCUT_LOC - data byte 17h bit description

Bit	Symbol	Description
2 to 0	HLOC[2:0]	low cut control[1]
		000 = off
		001 = 30 Hz low cut limit
		010 = 70 Hz low cut limit
		011 = 100 Hz low cut limit
		100 = 140 Hz low cut limit
		101 = 200 Hz low cut limit
		110 = 300 Hz low cut limit
		111 = 500 Hz low cut limit

[1] Function not available in TEF6635.

8.1.3 FM stereo weak signal handling

Table 54. STEREO_TIME - data byte 18h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SFT2	SFT1	SFT0	SAT2	SAT1	SAT0	SDT1	SDT0
Reset	0	1	1	1	0	1	0	1

Table 55. STEREO_TIME - data byte 18h bit description

Bit	Symbol	Description
7 to 5	SFT[2:0]	stereo fast time
		000 = 1 ms fast attack and decay time
		001 = 2 ms fast attack and decay time
		010 = 4 ms fast attack and decay time
		011 = 8 ms fast attack and decay time
		100 = 15 ms fast attack and decay time
		101 = 30 ms fast attack and decay time
		110 = 60 ms fast attack and decay time
		111 = 120 ms fast attack and decay time
4 to 2	SAT[2:0]	stereo slow attack time
		000 = 60 ms slow attack time
		001 = 120 ms slow attack time
		010 = 250 ms slow attack time
		011 = 500 ms slow attack time
		100 = 1000 ms slow attack time
1 and 0	SDT[1:0]	stereo slow decay time
		00 = 2 times the stereo slow attack time
		01 = 4 times the stereo slow attack time
		10 = 8 times the stereo slow attack time
		11 = 16 times the stereo slow attack time

Table 56. STEREO_DET - data byte 19h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	SMOD1	SMOD0	SFOL	SSOL	SFON	SSON	SFOM	SSOM
Reset	0	0	1	1	1	1	1	1

Table 57. STEREO_DET - data byte 19h bit description

Bit	Symbol	Description
7 and 6	SMOD[1:0]	stereo on modulation
		00 = off
		01 to 11 = weak to strong control on modulation
5	SFOL	stereo fast on level
		0 = off
		1 = fast control on level
4	SSOL	stereo slow on level
		0 = off
		1 = slow control on level
3	SFON	stereo fast on noise
		0 = off
		1 = fast control on ultrasonic noise

Table 57. STEREO_DET - data byte 19h bit description *...continued*

Bit	Symbol	Description
2	SSON	stereo slow on noise
		0 = off
		1 = slow control on ultrasonic noise
1	SFOM	stereo fast on multipath
		0 = off
		1 = fast control on multipath
0	SSOM	stereo slow on multipath
		0 = off
		1 = slow control on multipath

Table 58. STEREO_LEV - data byte 1Ah bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	SST3	SST2	SST1	SST0	SSL2	SSL1	SSL0
Reset	0	1	0	0	1	0	1	0

Table 59. STEREO_LEV - data byte 1Ah bit description

Bit	Symbol	Description
6 to 3	SST[3:0]	stereo start on level
		0000 to 1111 = late to early start of stereo on level 30 dBµV to 60 dBµV (2 dB step)
2 to 0	SSL[2:0]	stereo slope on level
		000 = stereo control range on level 30 dB
		001 = stereo control range on level 26 dB
		010 = stereo control range on level 22 dB
		011 = stereo control range on level 18 dB
		100 = stereo control range on level 15 dB
		101 = stereo control range on level 12 dB
		110 = stereo control range on level 9 dB
		111 = stereo control range on level 6 dB

Table 60. STEREO_N_M - data byte 1Bh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	SNS2	SNS1	SNS0	-	SMS2	SMS1	SMS0
Reset	0	0	1	1	0	0	1	1

Table 61. STEREO_N_M - data byte 1Bh bit description

Bit	Symbol	Description
6 to 4	SNS[2:0]	stereo noise sensitivity
		000 to 111 = FM weak to strong control on ultrasonic noise
2 to 0	SMS[2:0]	stereo multipath sensitivity
		000 to 111 = FM weak to strong control on multipath (wideband AM)

Table 62. STEREO_LIM - data byte 1Ch bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	SSLIM2	SSLIM1	SSLIM0	-	-	-	-
Reset	0	0	0	0	0	0	0	0

Table 63. STEREO_LIM - data byte 1Ch bit description

Bit	Symbol	Description
6 to 4	SSLIM[2:0]	stereo start limit
		000 = full stereo
		001 = 40 dB channel separation minimum control limit
		010 = 35 dB channel separation minimum control limit
		011 = 30 dB channel separation minimum control limit
		100 = 27 dB channel separation minimum control limit
		101 = 24 dB channel separation minimum control limit
		110 = 20 dB channel separation minimum control limit
		111 = 16 dB channel separation minimum control limit

Table 64. STEREOHB_DET - data byte 1Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	BMOD1	BMOD0	BFOL	BSOL	BFON	BSON	BFOM	BSOM
Reset	0	0	1	1	1	1	1	1

Table 65. STEREOHB_DET - data byte 1Dh bit description

Bit	Symbol	Description
7 and 6	BMOD[1:0]	high blend on modulation[1]
		00 = off
		01 to 11 = weak to strong control on modulation
5	BFOL	high blend fast on level[1]
		0 = off
		1 = fast control on level
4	BSOL	high blend slow on level[1]
		0 = off
		1 = slow control on level
3	BFON	high blend fast on noise[1]
		0 = off
		1 = fast control on noise
2	BSON	high blend slow on noise[1]
		0 = off
		1 = slow control on noise
1	BFOM	high blend fast on multipath[1]
		0 = off
		1 = fast control on multipath

Table 65. STEREOHB_DET - data byte 1Dh bit description *...continued*

Bit	Symbol	Description
0	BSOM	high blend slow on multipath[1]
		0 = off
		1 = slow control on multipath

[1] Function not available in TEF6635.

Remark: Stereo high blend uses the timing as set for stereo time (data byte 18h).

Table 66. STEREOHB_LNM - data byte 1Eh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	BNMS1	BNMS0	-	BLS2	BLS1	BLS0
Reset	0	0	0	1	0	0	1	1

Table 67. STEREOHB_LNM - data byte 1Eh bit description

Bit	Symbol	Description
5 and 4	BNMS[1:0]	high blend noise/multipath sensitivity[1]
		00 to 11 = late start to early start of control on noise and multipath (relative to stereo)
2 to 0	BLS[2:0]	high blend level sensitivity[1]
		000 to 111 = late to early start of control on level relative to stereo: stereo start to stereo start + slope (approximately 2 dB step for SSL = 15 dB)

[1] Function not available in TEF6635.

Remark: Stereo high blend sensitivity settings are relative to the stereo sensitivity settings of level, noise and multipath (data bytes 1Ah and 1Bh).

Table 68. Reserved - data byte 1Fh

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-
Reset	0	0	0	0	0	0	0	0

8.1.4 Input select and system control

Table 69. P_INPUT - data byte 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	PINP4	PINP3	PINP2	PINP1	PINP0
Reset	0	0	0	0	0	0	0	0

Table 70. P_INPUT - data byte 20h bit description

Bit	Symbol	Description
4 to 0	PINP[4:0]	primary input select
		00000 = radio (analog radio with automatic blend to digital radio from Host I^2S 0 if DIRAD = 1)
		01000 = analog input AIN0[1]
		01001 = analog input AIN1
		01010 = analog input AIN2, AIN3
		10000 = I^2S input source 0
		10001 = I^2S input source 1
		10010 = I^2S input source 2
		10011 = Host I^2S input source 0
		10100 = Host I^2S input source 1
		10101 = SPDIF
		11110 = internal white noise source
		11111 = internal sine source

[1] Function not available for TEF6635.

[2] AIN1 not available if navigation or phone use AIN2 or AIN3.

Data bytes 21h to 27h are reserved and should not be written to avoid disruption of audio settings.

Table 71. S_INPUT - data byte 28h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	SINP4	SINP3	SINP2	SINP1	SINP0
Reset	0	0	0	0	0	0	0	0

Table 72. S_INPUT - data byte 28h bit description

Bit	Symbol	Description
4 to 0	SINP[4:0]	secondary input select
		00000 = radio (analog radio with automatic blend to digital (via Host I^2S 0) if DIRAD = 1)
		01000 = analog input AIN0[1]
		01001 = analog input AIN1[2]
		01010 = analog input AIN2, AIN3[3]
		10000 = I^2S input source 0
		10001 = I^2S input source 1
		10010 = I^2S input source 2
		10011 = Host I^2S input source 0
		10100 = Host I^2S input source 1
		10101 = SPDIF
		11110 = internal white noise source
		11111 = internal sine source

[1] Function not available for TEF6635.

[2] AIN1 not available if primary channel, navigation or phone use AIN2 or AIN3.

[3] AIN2, AIN3 not available if primary channel uses AIN1.

Data bytes 29h to 3Eh are reserved and should not be written to avoid disruption of audio settings.

Table 73. SYSTEM - data byte 3Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	-	USE2	USE1	USE0	APWR1	APWR0	-	ASRF
Reset	0	0	1	0	0	0	0	0

Table 74. SYSTEM - data byte 3Fh bit description

Bit	Symbol	Description
6 to 4	USE[2:0]	use case selection availability of audio features is use case dependent use case can be selected only during initialization, i.e. before first power-up
		000 = reserved
		001 = primary channel, analog phone, analog navigation
		010 = primary channel, secondary channel, analog phone, analog navigation
		011 = primary channel, secondary channel, digital phone, analog navigation
		100 = primary channel, secondary channel, analog phone, digital navigation
		101 = reserved
		110 = primary channel
		111 = primary channel, digital phone, digital navigation
3 and 2	APWR[1:0]	audio power control
		00 = system power; audio power controlled together with radio power control (byte 00h; MODE)
		01 = reserved
		10 = audio power-down
		11 = audio power enable
0	ASRF	audio sample rate frequency
		0 = 44.1 kHz
		1 = 48 kHz

8.1.5 Audio special features

8.1.5.1 Audio limiter gain

The gain settings of the audio limiters can be read via subaddress A6h. Figure 5 shows the I^2C protocol used. Gain is a 12-bit value coded as a 2-byte negative number, using the least significant bits [11:0] for the gain. The most significant bits [15:12] are set to 1111.

A read operation may consist of two separate transmissions or a single transmission with the read and write operations joined using a repeated start condition. Limiter gain read subaddressing is only valid for the first read transmission following the write transmission with SA = A6h.

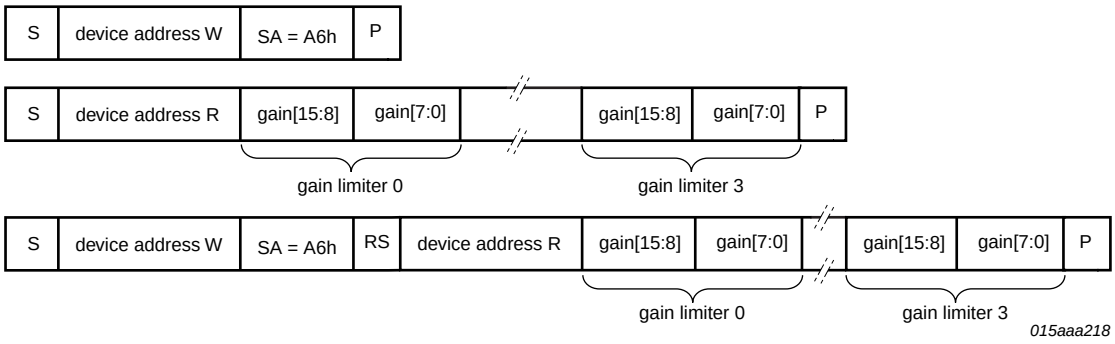


Fig 5. Audio limiter gain subaddressing

Table 75. Legend describing codes used in Figure 5 to Figure 10

Code	Description
S	start address
SA	subaddress
RS	repeated start condition
P	stop condition
PID	peripheral ID
OPT	option selected
MOD	mode

8.1.5.2 Peripheral configuration

Subaddress A9h is used to configure audio ADCs, DACs, I²S inputs, SPDIF inputs and the host I²S-bus interfaces. Figure 6 shows the I²C protocol used. The transmission can contain one or more configurations. Each configuration contains a peripheral ID (PID) along with the option selected (OPT). Table 76 to Table 81 describe these parameters.

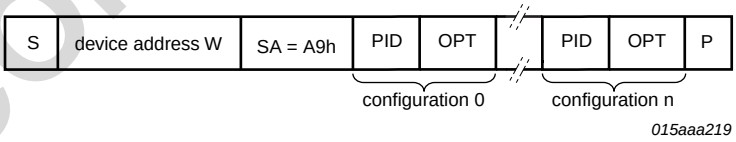


Fig 6. Peripheral configuration

Table 76. Peripheral ID codes

PID	Peripheral
00h	analog audio input AIN0
01h	analog audio input AIN1
02h	analog audio input AIN2
03h	analog audio input AIN3
0Ah	asynchronous I²S input 0 serial format
0Bh	asynchronous I²S input 1 serial format
0Ch	asynchronous I²S input 2 serial format

Table 76. Peripheral ID codes *…continued*

PID	Peripheral
14h	synchronous (host) I^2S input 0 serial format
15h	synchronous (host) I^2S input 1 serial format
16h	synchronous (host) I^2S output 0 serial format
17h	synchronous (host) I^2S output 1 serial format
1Eh	SPDIF input mode
1Fh	SPDIF sample rate range
28h	audio ADCs
32h	rear DAC
33h	front DAC

Table 77. Configuring analog audio inputs (PID = 0h to 3h)

OPT	Configuration
00h	differential 2 V (RMS) (default)
01h	differential 1 V (RMS)
02h	high common mode rejection 2 V (RMS)
03h	high common mode rejection 1 V (RMS)
04h	high common mode rejection 0.5 V (RMS)
05h	high common mode rejection 1.25 V (RMS)

Table 78. Data transmission format for synchronous and asynchronous (host) I^2S inputs and outputs (PID = 0Ah to 0Ch and PID = 14h to 17h)

OPT	Data transmission format
00h	I^2S
01h	LSB aligned 16-bit
02h	LSB aligned 18-bit
03h	LSB aligned 20-bit
04h	LSB aligned 24-bit
05h	off (default)

Table 79. SPDIF format (PID = 1Eh)

OPT	Format
00h	analog (enable bit slicer)
01h	digital (disable bit slicer)
02h	off (default)

Table 80. SPDIF sample rate (PID = 1Fh)

OPT	Sample rate
00h	8 kHz to 23.4 kHz
01h	12.5 kHz to 46.8 kHz
02h	25 kHz to 48 kHz (default)

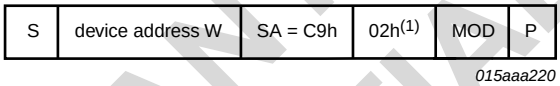
Table 81. ADCs and DACs (PID = 28h, 32h or 33h)

OPT	State
00h	on
01h	off (default)

8.1.6 Radio features

8.1.6.1 Radio configuration - audio sample rate

When this feature is enabled, the audio sample rate is shifted to avoid interference from the spurious signals generated by the host I²S outputs. The sample rate frequency shift is controlled by radio tuning. This function is enabled (MOD = 1) and disabled (MOD = 0) via subaddress C9h. The subaddress must be followed by data byte 02h to select the radio configuration feature (the only radio feature currently supported). Figure 7 shows the I²C protocol used.



(1) Data byte 02h selects the radio configuration feature

Fig 7. Radio configuration - shifting the audio sample rate

Table 82. Audio sample rate

MOD	Sample rate
00h	fixed audio sample rate
01h	audio sample rate frequency shift controlled by radio tuning (default)

8.1.7 Key codes

Optional features are activated by transmitting a 24-bit key code during initialization, before tuning begins. Key codes are set via subaddress E1h. The I²C protocol used is shown in Figure 8.

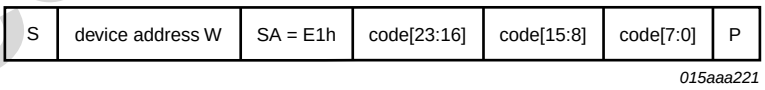


Fig 8. I²C protocol for setting key codes

8.2 Read mode

Upon receiving a read command, clock stretching occurs before the first data byte is sent. During this time TEF6635 andTEF6638 pauses the read transaction by holding the SCL line LOW. The transaction cannot continue until the line is released HIGH again. For details see *Application Note AN11092 "TEF6635/38 single-chip car radio"*.

Table 83. Device address

7	6	5	4	3	2	1	0
1	1	0	0	0	DA2	DA1	1 (read)

Table 84. Device address description

Bit	Symbol	Description
2 and 1	DA[2:1]	the device address is defined by the application of pins HOST_WS (= DA2) and HOST_BCK (= DA1); pull down to ground = '0', floating pin = '1'. The device address is determined after applying supply power to the device

Table 85. STATUS - read byte 00h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	QSR2	QSR1	QRS0	RDAV	STIN	-	-	POR

Table 86. STATUS - read byte 00h bit description

Bit	Symbol	Description
7 to 5	QRS[2:0]	Quality read status - when tuning is ready, the quality detectors (LEVEL, USN, WAM, FOF, IFBW and MOD) are reset for fastest result. The quality result of an AF_update tuning is stored and can be read once at a later time
		000 = no quality data available, tuning is in progress
		001 = no quality data available, tuning ready (settling of quality detectors)
		010 = 1 ms to 2 ms result (FM LEVEL available)
		011 = 2 ms to 8 ms result (FM: first USN, WAM and FOF result, AM: first LEVEL, USN and reliable FOF result)
		100 = 8 ms to 32 ms result
		101 = > 8 ms result (FM: reliable USN, WAM and FOF result, AM: reliable LEVEL and USN result)
		110 = reserved
		111 = AF_update quality data available of FM LEVEL, USN, WAM, FOF and IFBW
4	RDAV	RDS data available
		0 = no new RDS data available
		1 = new RDS data available (decoder or demodulator)
3	STIN	FM stereo indicator
		0 = no stereo pilot found
		1 = stereo pilot detected
0	POR	power-on reset
		0 = standard operation
		1 = internal reset detected. I^2C settings are lost

Remark: POR = 1 standard occurs either after the device is powered up or after a forced reset by means of the reset pin. However, environmental disturbances that may go unnoticed by the controlling microcontroller are also detected this way. Consequently, it is advisable to monitor the POR bit.

Remark: POR = To reset the POR reading back to 0, the STATUS byte must be read at least once and a tuning action must be performed with MODE = 1 or 2.

Table 87. LEVEL - read byte 01h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LEV7	LEV6	LEV5	LEV4	LEV3	LEV2	LEV1	LEV0

Table 88. LEVEL - read byte 01h bit description

Bit	Symbol	Description
7 to 0	LEV[7:0]	signal strength
		0 to 255 = RF input level −8 dBμV to 119.5 dBμV (LEV × 0.5 − 8 dBμV)

Remark: The read value is influenced by the setting of LEV0 (data byte 0Ch). For very low input levels the reading is limited by noise. The attenuation of the RF AGC is only partly compensated and the maximum possible reading is 99.5 dBμV.

Table 89. USN - read byte 02h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	USN7	USN6	USN5	USN4	USN3	USN2	USN1	USN0

Table 90. USN - read byte 02h bit description

Bit	Symbol	Description
7 to 0	USN[7:0]	FM noise detector
		0 to 255 = FM no noise to high noise disturbance detected (adjacent channel or multipath)
		AM adjacent detector[1]

[1] Function not available in TEF6635

Remark: The AM adjacent detector measures the signal level difference between the desired channel and the larger of the two adjacent channels. The signal level difference is positive if the adjacent signal level is larger than the desired signal and negative if the adjacent signal level is smaller than the desired signal. Noise and the influence of the RF AGC, limit the reading to approximately −60 dB to + 60dB whereas the readout range is from −128 dB to +127 dB.

Table 91. WAM - read byte 03h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	WAM7	WAM6	WAM5	WAM4	WAM3	WAM2	WAM1	WAM0

Table 92. WAM (FM function)- read byte 03h bit description

Bit	Symbol	Description
7 to 0	WAM[7:0]	FM multipath detector
		0 to 255 = FM no multipath to high multipath disturbance detected (FM wideband AM)

Table 93. FOF - read byte 04h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	FOFN	FOF6	FOF5	FOF4	FOF3	FOF2	FOF1	FOF0

Table 94. FOF - read byte 04h bit description

Bit	Symbol	Description
7	FOFN	negative frequency offset
		0 = the result indicates a positive RF frequency error
		1 = the result indicates a negative RF frequency error
6 to 0	FOF[6:0]	frequency offset (IF counter)
		0 to 126 =
		FM: 0 kHz to 126 kHz frequency error (1 kHz accuracy)
		AM: 0 kHz to 12.6 kHz frequency error (0.1 kHz accuracy)
		127 = out of range frequency error
		FM ≥ 127 kHz
		AM ≥ 12.7 kHz

Table 95. IFBW - read byte 05h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	IFBW3	IFBW2	IFBW1	IFBW0	-	-	-	-

Table 96. IFBW - read byte 05h bit description

Bit	Symbol	Description
7 to 4	IFBW[3:0]	IF bandwidth
		0 to 15 = narrow to wide IF filter bandwidth

Table 97. MOD - read byte 06h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	MOD7	MOD6	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0

Table 98. MOD - read byte 06h bit description

Bit	Symbol	Description
7 to 0	MOD[7:0]	modulation detector
		0 to 100 =
		FM: 0% to 100% (0 kHz to 75 kHz FM deviation)
		AM: 0% to 100% (AM modulation index)
		100 to 200 =
		FM:100% to 200% (75 kHz to 150 kHz deviation) overmodulation range
		100 to 150 =
		AM:100% to 160% peak modulation range

Remark: The modulation detector reading depends on the modulation type and frequency. It is more an indicative detector rather than a precise instrument. MOD is not part of the AFU sampled quality data (MOD = 0). AM peak modulation is limited to approximately 130%.

8.2.1 RDS demodulator mode data (RDSM = 0): read byte 07h to 11h

Table 99. RDS_STATUS - read byte 07h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RDAV	DOFL	-	-	-	-	-	-

Table 100. RDS_STATUS - read byte 07h bit description

Bit	Symbol	Description
7	RDAV	RDS data available
		0 = no new RDS data available
		1 = new 32 bit RDS demodulator data
6	DOFL	data overflow notification
		0 = no data loss
		1 = previous data was not read, replaced by newer

Table 101. RDS_DAT3 - read byte 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DD31	DD30	DD29	DD28	DD27	DD26	DD25	DD24

Table 102. RDS_DAT2 - read byte 09h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DD23	DD22	DD21	DD20	DD19	DD18	DD17	DD16

Table 103. RDS_DAT1 - read byte 0Ah bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DD15	DD14	DD13	DD12	DD11	DD10	DD9	DD8

Table 104. RDS_DAT0 - read byte 0Bh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0

Table 105. RDS_DAT - read byte 08h to 0Bh bit description

Bit	Symbol	Description
31 to 0	DD[31:0]	demodulator data
		32 bit buffered RDS demodulator data

Table 106. unused for RDSM = 0 - read byte 0Ch to 11h

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

8.2.2 RDS decoder mode data (RDSM = 1): read byte 07h to 11h

Table 107. RDS_STATUS - read byte 07h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RDAV	DOFL	SDATA	TBGRP	EEGRP	-	SYNC	-

Table 108. RDS_STATUS - read byte 07h bit description

Bit	Symbol	Description
7	RDAV	RDS data available
		0 = no new RDS data available
		1 = new RDS group data or first PI data available
6	DOFL	data overflow notification
		0 = no data loss
		1 = previous data was not read it is replaced by new data
5	SDATA	start data flag[1]
		0 = continuous operation; group data
		1 = first PI; data with PI after decoder synchronization
4	TBGRP	RDS group type
		0 = type A; ADCD group (PI code in A)
		1 = type B; ABC'D group (PI code in A and C')
3	EEGRP	special RDS group[2]
		0 = standard RDS group; ABC(')D
		1 = RBDS 'MMBS' group type; EEEE
1	SYNC	decoder status
		0 = decoder not synchronized (no RDS)
		1 = decoder synchronized; RDS data reception active

[1] For SDATA=1 group data may be incomplete; blocks not available are marked as 'non correctable error'; xERR = 3.

[2] EEGRP detection (enabled by RBDS = 1) has become obsolete; E blocks are no longer part of the RBDS system standard and are not found on-air.

Table 109. RDS_A_H - read byte 08h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	A15	A14	A13	A12	A11	A10	A9	A8

Table 110. RDS_A_L - read byte 09h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	A7	A6	A5	A4	A3	A2	A1	A0

Table 111. RDS_A - read byte 08h to 09h bit description

Bit	Symbol	Description
15 to 0	A[15:0]	first block of RDS group
		A block data

Table 112. RDS_B_H - read byte 0Ah bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	B15	B14	B13	B12	B11	B10	B9	B8

Table 113. RDS_B_L - read byte 0Bh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	B7	B6	B5	B4	B3	B2	B1	B0

Table 114. RDS_B - read byte 0Ah to 0Bh bit description

Bit	Symbol	Description
15 to 0	B[15:0]	second block
		B block data

Table 115. RDS_C_H - read byte 0Ch bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C15	C14	C13	C12	C11	C10	C9	C8

Table 116. RDS_C_L - read byte 0Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	C7	C6	C5	C4	C3	C2	C1	C0

Table 117. RDS_C - read byte 0Ch to 0Dh bit description

Bit	Symbol	Description
15 to 0	C[15:0]	third block
		C block data (TBGRP = 0) or C' block data (TBGRP = 1)

Table 118. RDS_D_H - read byte 0Eh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	D15	D14	D13	D12	D11	D10	D9	D8

Table 119. RDS_D_L - read byte 0Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	D7	D6	D5	D4	D3	D2	D1	D0

Table 120. RDS_D - read byte 0Eh to 0Fh bit description

Bit	Symbol	Description
15 to 0	D[15:0]	fourth block
		D block data

Table 121. RDS_ERR - read byte 10h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	AERR1	AERR0	BERR1	BERR0	CERR1	CERR0	DERR1	DERR0

Table 122. RDS_ERR - read byte 10h bit description

Bit	Symbol	Description
7 and 6	AERR[1:0]	data error status of A block data (determined by decoder checking)
		0 = no error; block data was detected without errors
		1 = small error; possible 1 bit reception error detected; data is corrected (max 2 bit burst error)
		2 = large error; theoretically correctable error detected; data is corrected (max 5 bit burst error)
		3 = non correctable error detected
5 and 4	BERR[1:0]	data error status of B block data (determined by decoder checking)
		0 = no error; block data was detected without errors
		1 = small error; possible 1 bit reception error detected; data is corrected (max 2 bit burst error)
		2 = large error; theoretically correctable error detected; data is corrected (max 5 bit burst error)
		3 = non correctable error detected
3 and 2	CERR[1:0]	data error status of C block data (determined by decoder checking)
		0 = no error; block data was detected without errors
		1 = small error; possible 1 bit reception error detected; data is corrected (max 2 bit burst error)
		2 = large error; theoretically correctable error detected; data is corrected (max 5 bit burst error)
		3 = non correctable error detected
1 and 0	DERR[1:0]	data error status of D block data (determined by decoder checking)
		0 = no error; block data was detected without errors
		1 = small error; possible 1 bit reception error detected; data is corrected (max 2 bit burst error)
		2 = large error; theoretically correctable error detected; data is corrected (max 5 bit burst error)
		3 = non correctable error detected

Table 123. unused for RDSM = 1 - read byte 11h

Bit	7	6	5	4	3	2	1	0
Symbol	-	-	-	-	-	-	-	-

Table 124. AGCATT - read byte 12h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	INATT2	INATT1	INATT0	0	FBATT1	FBATT0

Table 125. AGCATT - read byte 12h bit description

Bit	Symbol	Description
5 to 3	INATT[2:0]	RF AGC input attenuation in steps of 6 dB
		AM: 0 to 7: 0 dB to 42 dB of input attenuation
		FM: 0 to 6: 0 dB to 36 dB of input attenuation
1 and 0	FBATT[1:0]	RF AGC feedback attenuation
		AM: 0 to 3: 0 dB to 18 dB of feedback attenuation
		FM: 0 to 1: 0 dB to 6 dB of feedback attenuation

Remark: Total RF AGC attenuation is (INATT + FBATT) * 6 dB.

Table 126. IDENT0 - read byte 13h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	HWTYP4	HWTYP3	HWTYP2	HWTYP1	HWTYP0	HWSID2	HWSID1	HWSID0

Table 127. IDENT0 - read byte 13h bit description

Bit	Symbol	Description
7 to 3	HWTYP[4:0]	hardware type
		00000 = TEF663x
2 to 0	HWSID[2:0]	hardware sub identifier
		010 = C

Table 128. IDENT1 - read byte 14h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	TYPE	VAR2	VAR1	VAR0	HWID3	HWID2	HWID1	HWID0

Table 129. IDENT1 - read byte 14h bit description

Bit	Symbol	Description
7	TYPE	device type
		0 = radio and audio
		1 = radio only
6 to 4	VAR[2:0]	device variant
		101 = lite
		111 = premium
3 to 0	HWID[3:0]	hardware identifier
		0000 = V1

Table 130. IDENT2 - read byte 15h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	0	0	SWID5	SWID4	SWID3	SWID2	SWID1	SWID0

Table 131. IDENT2 - read byte 15h bit description

Bit	Symbol	Description
5 to 0	SWID[5:0]	software identifier
		000011 = 03

8.2.3 Audio read

Table 132. VU_L_H - read byte 16h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LVU15	LVU14	LVU13	LVU12	LVU11	LVU10	LVU9	LVU8

Table 133. VU_L_L - read byte 17h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	LVU7	LVU6	LVU5	LVU4	LVU3	LVU2	LVU1	LVU0

Table 134. LVU - read byte 16h to 17h bit description

Bit	Symbol	Description
15 to 0	LVU[15:0]	left channel audio level (linear scale)

Table 135. VU_R_H - read byte 18h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RVU15	RVU14	RVU13	RVU12	RVU11	RVU10	RVU9	RVU8

Table 136. VU_R_L - read byte 19h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	RVU7	RVU6	RVU5	RVU4	RVU3	RVU2	RVU1	RVU0

Table 137. RVU - read byte 18h to 19h bit description

Bit	Symbol	Description
15 to 0	RVU[15:0]	right channel audio level (linear scale)

Table 138. GRAPHIC1 - read byte 1Ah bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAA7	GSAA6	GSAA5	GSAA4	GSAA3	GSAA2	GSAA1	GSAA0

Table 139. GRAPHIC2 - read byte 1Bh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAB7	GSAB6	GSAB5	GSAB4	GSAB3	GSAB2	GSAB1	GSAB0

Table 140. GRAPHIC3 - read byte 1Ch bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAC7	GSAC6	GSAC5	GSAC4	GSAC3	GSAC2	GSAC1	GSAC0

Table 141. GRAPHIC4 - read byte 1Dh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAD7	GSAD6	GSAD5	GSAD4	GSAD3	GSAD2	GSAD1	GSAD0

Table 142. GRAPHIC5 - read byte 1Eh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAE7	GSAE6	GSAE5	GSAE4	GSAE3	GSAE2	GSAE1	GSAE0

Table 143. GRAPHIC6 - read byte 1Fh bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAF7	GSAF6	GSAF5	GSAF4	GSAF3	GSAF2	GSAF1	GSAF0

Table 144. GRAPHIC7 - read byte 20h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAG7	GSAG6	GSAG5	GSAG4	GSAG3	GSAG2	GSAG1	GSAG0

Table 145. GRAPHIC8 - read byte 21h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAH7	GSAH6	GSAH5	GSAH4	GSAH3	GSAH2	GSAH1	GSAH0

Table 146. GRAPHIC9 - read byte 22h bit allocation

Bit	7	6	5	4	3	2	1	0
Symbol	GSAI7	GSAI6	GSAI5	GSAI4	GSAI3	GSAI2	GSAI1	GSAI0

Table 147. GRAPHIC - read byte 1Ah to 22h bit description

Bit	Symbol	Description
7 to 0	GSAA[7:0]	graphic spectrum analyzer 63 Hz (bar graph)
7 to 0	GSAB[7:0]	graphic spectrum analyzer 125 Hz
7 to 0	GSAC[7:0]	graphic spectrum analyzer 250 Hz
7 to 0	GSAD[7:0]	graphic spectrum analyzer 500 Hz
7 to 0	GSAE[7:0]	graphic spectrum analyzer 1 kHz
7 to 0	GSAF[7:0]	graphic spectrum analyzer 2 kHz
7 to 0	GSAG[7:0]	graphic spectrum analyzer 4 kHz
7 to 0	GSAH[7:0]	graphic spectrum analyzer 8 kHz
7 to 0	GSAI[7:0]	graphic spectrum analyzer 16 kHz

8.2.4 Read subaddressing

To reduce the I^{2}C-bus load, it is possible to use subaddressing for read transmissions. Figure 9 shows the I^{2}C protocol used for subaddressing. A write transmission without data is used to set the read subaddress for the next read operation. Subaddressed read operations can consist of either two separate transmissions or a single transmission with the read and write operations joined using a repeated start condition. Read subaddressing is only valid for the read transmission immediately following the write operation. Without subaddressing, a read transmission will always start at read byte 00h.

Reading byte 01h (LEVEL) resets AFU status bits QRS and frees read data bytes 01h to 06h. Reading byte 08h (RDS_A_H) resets RDS status bit RDAV and frees read data bytes 08h to 11h.

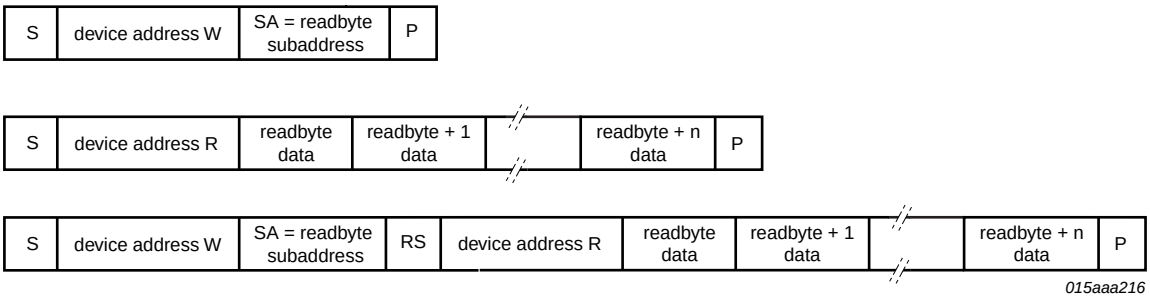


Fig 9. Read subaddressing

Table 148. Legend describing codes used in Figure 9 to Figure 8

Code	Description
S	start address
SA	subaddress
RS	repeated start condition
P	stop condition
PID	peripheral ID
OPT	option selected
MOD	mode

8.2.5 Reading back written data

A write transmission to subaddress E0h sets the subaddress for the next read operation. Read back subaddressing can consist of either two separate transmissions or a single transmission with the read and write operations joined using a repeated start condition.

Read back subaddressing is only valid for the read transmission immediately following the write operation. Read back is supported for subaddress range 00h to 3Fh only.

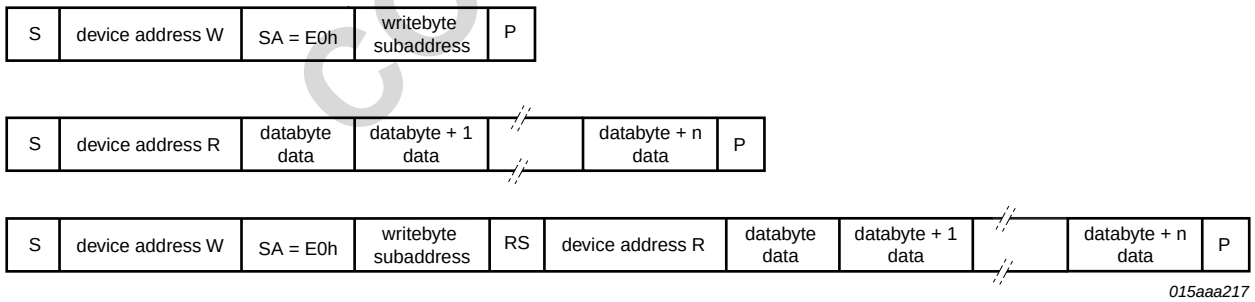


Fig 10. Read back subaddressing

9. Limiting values

Table 149. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pins VDDA_RF_3V3, VDDA_LNA_3V3, VDDA_PLL_3V3, VDDA_IFADC_3V3 and VDDA_CODEC_3V3		−0.5	+3.9	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	on pins VDDIO_0_3V3, VDDIO_1_3V3, VDDIO_2_3V3 and VDDD_PLL_3V3		−0.5	+3.9	V
$V_{DDD(1V2)}$	digital supply voltage (1.2 V)	on pins VDDA_PL550_1V2, VDDC_0_1V2, VDDC_1_1V2, VDDM_0_1V2 and VDDM_1_1V2		−0.5	+1.6	V
$\Delta V_{DD(3V3-3V3)}$	supply voltage difference between two 3.3 V supplies			−0.3	+0.3	V
$\Delta V_{DD(1V2-1V2)}$	supply voltage difference between two 1.2 V supplies			−0.05	+0.05	V
V_n	voltage on any other pin		[1]	−0.5	$+V_{DDD(3V3)}$ + 0.3	V
		on pins 44, 47, 48, 50, 51 and 54		−1.7	+4.2	V
		on pins 45, 46, 49, 52 and 53		−0.6	+3.1	V
$I_{o(sink)}$	output sink current	on pin IFADC_DEC		−5	+5	mA
$I_{o(source)}$	output source current	on pin IFADC_DEC		−5	+5	mA
I_{lu}	latch-up current	all supply voltages below the maximum value	[2]	−100	+100	mA
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
T_j	junction temperature			-	125	°C
V_{ESD}	electrostatic discharge voltage	human body model	[3]	−2000	+2000	V
		charged-device model				
		corner pins	[4]	−750	+750	V
		corner pins	[5]	−650	+650	V
		other pins	[4]	−400	+400	V
		other pins	[5]	−250	+250	V

[1] The maximum voltage shall be less than 3.9 V.

[2] In accordance with AEC - Q100-004.

[3] In accordance with AEC - Q100-002 H2 and JESD22-A114 Class 2.

[4] In accordance with JESD22-C101 Class II.

[5] In accordance with AEC - Q100-011 C2.

10. Thermal characteristics

Table 150. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	dual layer board	[1]	39	K/W

[1] Simulation result assuming a dual layer board with a copper thickness of 35 μm; size: 50 × 50 mm; exposed die pad soldered to thermal landing pattern; thermal landing pattern connected to a large ground plane on the bottom layer by multiple thermal vias; copper coverages 25 % (top layer) and 90 % (bottom layer).

11. Static characteristics

Table 151. Voltages and currents characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	on pins VDDA_RF_3V3, VDDA_LNA_3V3, VDDA_PLL_3V3, VDDA_IFADC_3V3 and VDDA_CODEC_3V3	3.0	3.3	3.5	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	on pins VDDIO_0_3V3, VDDIO_1_3V3, VDDIO_2_3V3 and VDDD_PLL_3V3	3.0	3.3	3.5	V
$V_{DDD(1V2)}$	digital supply voltage (1.2 V)	on pins VDDA_PL550_1V2, VDDC_0_1V2, VDDC_1_1V2, VDDM_0_1V2 and VDDM_1_1V2	1.14	1.2	1.3	V
Current in FM mode						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF_3V3	28	33	39	mA
$I_{DDA(LNA)}$	LNA analog supply current	on pin VDDA_LNA_3V3	36	51	65	mA
$I_{DDA(PLL)}$	PLL analog supply current	on pin VDDA_PLL_3V3	27	34	41	mA
$I_{DDD(PLL)}$	PLL digital supply current	on pin VDDD_PLL_3V3	3.6	5.4	7.2	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC_3V3	22	26	30	mA
$I_{DDA(CODEC)}$	codec analog supply current	on pin VDDA_CODEC_3V3	26	31	35	mA
$I_{DD(IO)}$	input/output supply current	on pins VDDIO_0_3V3, VDDIO_1_3V3 and VDDIO_2_3V3	9	13	17	mA
$I_{DDA(PLL550)}$	PLL 550 MHz analog supply current	on pin VDDA_PL550_1V2	1.2	2.2	3.3	mA
$I_{DDD(C)}$	core digital supply current	on pins VDDC_0_1V2 and VDDC_1_1V2	45	59	65	mA
$I_{DDD(MEM)}$	memory digital supply current	on pins VDDM_0_1V2 and VDDM_1_1V2	14	16	18	mA
Current in AM mode						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF_3V3	52	73	93	mA
$I_{DDA(LNA)}$	LNA analog supply current	on pin VDDA_LNA_3V3	1.0	2.6	3.2	mA

Table 151. Voltages and currents characteristics *…continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DDA(PLL)}$	PLL analog supply current	on pin VDDA_PLL_3V3	29	37	45	mA
$I_{DDD(PLL)}$	PLL digital supply current	on pin VDDD_PLL_3V3	3.6	5.4	7.2	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC_3V3	22	26	30	mA
$I_{DDA(CODEC)}$	codec analog supply current	on pin VDDA_CODEC_3V3	26	31	35	mA
$I_{DD(IO)}$	input/output supply current	on pins VDDIO_0_3V3, VDDIO_1_3V3 and VDDIO_2_3V3	9	13	17	mA
$I_{DDA(PLL550)}$	PLL 550 MHz analog supply current	on pin VDDA_PL550_1V2	1.2	2.2	3.3	mA
$I_{DDD(C)}$	core digital supply current	on pins VDDC_0_1V2 and VDDC_1_1V2	45	57	62	mA
$I_{DDD(MEM)}$	memory digital supply current	on pins VDDM_0_1V2 and VDDM_1_1V2	14	15	18	mA
Current in Standby mode						
$I_{DDA(RF)}$	RF analog supply current	on pin VDDA_RF_3V3	2.3	2.8	3.3	mA
$I_{DDA(LNA)}$	LNA analog supply current	on pin VDDA_LNA_3V3	1.0	1.9	2.4	mA
$I_{DDA(PLL)}$	PLL analog supply current	on pin VDDA_PLL_3V3	3	5.5	9	mA
$I_{DDD(PLL)}$	PLL digital supply current	on pin VDDD_PLL_3V3	0.6	1.2	2.4	mA
$I_{DDA(IFADC)}$	IF ADC analog supply current	on pin VDDA_IFADC_3V3	25	45	56	mA
$I_{DDA(CODEC)}$	codec analog supply current	on pin VDDA_CODEC_3V3	0.15	0.2	0.25	mA
$I_{DD(IO)}$	input/output supply current	on pins VDDIO_0_3V3, VDDIO_1_3V3 and VDDIO_2_3V3	9.5	13	17	mA
$I_{DDA(PLL550)}$	PLL 550 MHz analog supply current	on pin VDDA_PL550_1V2	0.75	1.3	2.5	mA
$I_{DDD(C)}$	core digital supply current	on pins VDDC_0_1V2 and VDDC_1_1V2	4	9	15	mA
$I_{DDD(MEM)}$	memory digital supply current	on pins VDDM_0_1V2 and VDDM_1_1V2	0.4	0.8	1.5	mA
Reference voltage						
V_{ref}	reference voltage		2.375	2.5	2.65	V
V_{IFADC_DEC}	voltage on pin IFADC_DEC		2.35	2.5	2.65	V
Voltage regulator						
$I_{o(source)}$	output source current	on pin CTRL_1V2_SUPPLY	0	-	5	mA

Table 152. Pin characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input characteristics						
V_{IH}	HIGH-level input voltage		2.0	-	$V_{DDD(3V3)}$ + 0.5	V
V_{IL}	LOW-level input voltage		−0.5	-	0.8	V
$V_{hys(i)}$	input hysteresis voltage		0.1 × $V_{DDD(3V3)}$	-	-	V

Table 152. Pin characteristics *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Weak input pull-up/pull-down characteristics							
$R_{pu(weak)}$	weak pull-up resistance	IO = 0 V	[1]	40	50	57	kΩ
$R_{pd(weak)}$	weak pull-down resistance	IO = $V_{DDD(3V3)}$	[1]	40	50	57	kΩ
Output characteristics							
Z_o	output impedance	NMOS driver					
		V_{OL} = 1.2 V		40	-	-	Ω
		V_{OL} = 2.0 V		-	-	67.5	Ω
		PMOS driver					
		V_{OH} = $V_{DDD(3V3)}$ −1.2 V		40	-	-	Ω
		V_{OH} = $V_{DDD(3V3)}$ −2.0 V		-	-	67.5	Ω
I_{OSH}	HIGH-level short-circuit output current	drive high; output connected to ground		-	-	90	mA
I_{OSL}	LOW-level short-circuit output current	output connected to $V_{DDD(3V3)}$		-	-	87	mA
I_{OH}	HIGH-level output current	V_{OH} = $V_{DDD(3V3)}$ − 0.4 V	[2]	7.3	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[2]	7.1	-	-	mA
Power-on reset							
3.3 V supply voltage on pin VDDIO_2_3V3							
$V_{th(det)POR}$	power-on reset detection threshold voltage			2.3	2.5	2.7	V
$V_{th(rec)POR}$	power-on reset recovery threshold voltage			-	2.67	-	V
$V_{hys(POR)}$	power-on reset hysteresis voltage			70	-	220	mV

[1] See Table 3 for an overview of cell types and configuration of pull-up/pull-down.

[2] The output driver is designed on impedance matching at given pad voltages. For test purposes, I_{OH} and I_{OL} values at low V_{OH}/V_{OL} levels are shown. Note that these values are based on simulation only.

12. Dynamic characteristics

Table 153. Dynamic characteristics for audio codec

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; f_s = 44.1 kHz; T_{amb} = 25 °C; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PSRR	power supply rejection ratio	pin VDDA_CODEC_3V3; V_{ripple} = 100 mV (p-p)				
		$f_{ripple} \leq$ 50 kHz	60	65	-	dB
		f_{ripple} = 217 Hz or 433 Hz; differential mode	-	85	-	dB
Audio ADC						
R_i	input resistance	single-ended	15	21	27	kΩ
V_i	input voltage	2 V RMS differential mode; (THD+N)/S < 1 %	-	-	2.2	V
		2 V RMS single-ended or pseudo differential mode	-	-	2.0	V
$N_{O(ADC)}$	ADC output value	V_i = 0 dB; all modes	−4	−3	−2	dBFS
$V_{i(unb)(ch-ch)}$	input voltage unbalance between channels		−0.2	-	0.2	dB
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	f_i = 1 kHz at 0 dB differential mode; 2 V RMS or 1 V RMS; differential mode; single-ended or pseudo differential mode; 2 V RMS or 1.25 V RMS; DAC level < −3 dBFS		−80	−75	dB
		f_i = 1 kHz at −60 dB differential mode 2 V RMS or 1 V RMS; high common mode rejection or single-ended 2 V RMS or 1.25 V RMS; A-weighted	-	−31	−25	dB(A)
$\alpha_{ct(ch)}$	channel crosstalk	f_i = 1 kHz				
		between inputs	85	90	-	dB
		between left and right channel of AIN_0	85	90	-	dB
		between left and right channel of AIN_1 with a coupling capacitor (C36 in Figure 12) of				
		C = 47 µF	65	-	-	dB
		C = 10 µF	55	-	-	dB
CMRR	common-mode rejection ratio	V_i =100 mV (p-p); $R_s \leq$ 20 Ω				
		f_i = 1 kHz	55	-	-	dB
		f_i = 20 kHz	40	-	-	dB
Audio DAC						
R_o	output resistance		-	-	1	kΩ
V_o	output voltage	single-ended; at 0 dBFS digital input; R_L = 20 kΩ	975	1000	1025	mV

Table 153. Dynamic characteristics for audio codec *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; f_s = 44.1 kHz; T_{amb} = 25 °C; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{o(unb)(ch-ch)}$	output voltage unbalance between channels	Full-scale output; deviation in output level of one of the four DAC outputs with respect to the average of the four outputs	−0.2	-	0.2	dB
(THD+N)/S	total harmonic distortion plus noise-to-signal ratio	R_L > 20 kΩ	-	−85	−78	dB
		A-weighted at −60 dBFS	-	−46	−40	dB(A)
$V_{n(o)(RMS)}$	RMS output noise voltage	idle channel; A-weighted	-	5	10	μV
		out of band noise; measured with a brick-wall high-pass filter with $f_{-3dB} = f_s / 2$; C_L = 6.8 nF	-	-	2	mV
α_{cs}	channel separation		74	82	-	dB

Table 154. Dynamic characteristics for tuning system

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Crystal oscillator						
f_{xtal}	crystal frequency		-	62.4	-	MHz
Tuning oscillator						
f_{osc}	oscillator frequency		5.3	-	6.2	GHz
$\varphi_{n(RF\_LO)}$	RF LO phase noise	f_{LO} = 100 MHz; Δf = 10 kHz	106	111	-	dBc/Hz
t_{tune}	tuning time		-	80	100	μs

Table 155. Dynamic characteristics for FM path

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; all RF voltages refer to an unterminated RMS voltage with a source impedance of 75 Ω; 22.5 kHz deviation; 1 kHz audio frequency; de-emphasis of 50 μs; RF frequency of 97.1 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM system						
f_{RF}	RF frequency	FM tuning range	65	-	108	MHz
$f_{tune(step)}$	step of tuning frequency		-	10	-	kHz
f_{IF}	IF frequency	f_{xtal} = 62.4 MHz	-	300	-	kHz

Table 155. Dynamic characteristics for FM path *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; all RF voltages refer to an unterminated RMS voltage with a source impedance of 75 Ω; 22.5 kHz deviation; 1 kHz audio frequency; de-emphasis of 50 μs; RF frequency of 97.1 MHz; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{i(sens)}$	input sensitivity voltage	(S+N)/N = 26 dB; Δf = 22.5 kHz; f_{AF} = 1 kHz					
		weak signal handling off		-	5	-	dBμV
		weak signal handling set to default, CEQ disabled	[1]	-	2	-	dBμV
		weak signal handling set to default, CEQ enabled	[1]	-	−4	-	dBμV
		Δf_{RDS} = 2 kHz; Δf = 22.5 kHz; f_{AF} = 1 kHz; stereo					
		for 50 % block quality RDS reception		-	17	19	dBμV
		for 95 % block quality RDS reception		-	20	22	dBμV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 80 dBμV; Δf = 22.5 kHz; f_{AF} = 1 kHz					
		mono		70	75	-	dB
		stereo		60	65	-	dB
$\alpha_{sup(AM)}$	AM suppression	$V_{i(RF)}$ = 60 dBμV; m = 30 %; f_{AF} = 1 kHz		67	70	-	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 60 dBμV; Δf = 75 kHz; f_{AF} = 1 kHz					
		mono		-	0.03	0.1	%
		stereo L-only		-	0.1	0.2	%
Δf_{max}	maximum frequency deviation	$V_{i(RF)}$ = 80 dBμV; f_{AF} = 1 kHz; THD = 3 %		150	-	-	kHz
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$		90	-	-	dB
S	selectivity	static selectivity					
		Δf_{RF} = ±100 kHz		60	65	-	dB
		Δf_{RF} = ±200 kHz		65	70	-	dB
		Δf_{RF} = ±300 kHz		70	-	-	dB
IP3	third-order intercept point	f_{RF} = 97.1 MHz; $f_{RF(unw)1}$ = 97.5 MHz; $f_{RF(unw)2}$ = 97.9 MHz; balun application; see Figure 13		114	117	-	dBμV

Table 155. Dynamic characteristics for FM path *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; all RF voltages refer to an unterminated RMS voltage with a source impedance of 75 Ω; 22.5 kHz deviation; 1 kHz audio frequency; de-emphasis of 50 μs; RF frequency of 97.1 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(RF)AGC(start)}$	start AGC RF input voltage	wideband threshold; data byte 0 bits BAND[1:0] = 00 (FM world)				
		data byte 3h bits RFAGC[1:0] = 00	89	92	95	dBμV
		data byte 3h bits RFAGC[1:0] = 01	86	89	92	dBμV
		data byte 3h bits RFAGC[1:0] = 10	83	86	89	dBμV
		data byte 3h bits RFAGC[1:0] = 11	80	83	86	dBμV
$\alpha_{cr(AGC)}$	AGC control range		38	42	46	dB
α_{cs}	channel separation	$V_{i(RF)}$ = 60 dBμV; Δf = 67.5 kHz; f_{AF} = 1 kHz; stereo L-only	40	-	-	dB
N_{LEV}	LEV value	V_{RF} = 60 dBμV; f_{RF} = 97.2 MHz; Δf = 0 kHz; data byte 0Ch; LEVO[5:0] = 11 0000 (level offset = 0 dB) [2]	130	136	142	

Table 155. Dynamic characteristics for FM path *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; all RF voltages refer to an unterminated RMS voltage with a source impedance of 75 Ω; 22.5 kHz deviation; 1 kHz audio frequency; de-emphasis of 50 μs; RF frequency of 97.1 MHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
FM LNA (input pins FM_IN_P and FM_IN_N)						
$V_{FM\_IN\_P}$	voltage on pin FM_IN_P	data byte 12h bits INATT[2:0] = 000	1.15	-	1.45	V
$V_{FM\_IN\_N}$	voltage on pin FM_IN_N	data byte 12h bits INATT[2:0] = 000	1.15	-	1.45	V
R_i	input resistance	differential on pin FM_IN_P to pin FM_IN_N; f_{RF} = 100 MHz				
		data byte 12h bits INATT[2:0] = 000	-	261	-	Ω
		data byte 12h bits INATT[2:0] = 001	-	241	-	Ω
		data byte 12h bits INATT[2:0] = 010	-	206	-	Ω
		data byte 12h bits INATT[2:0] = 011	-	203	-	Ω
		data byte 12h bits INATT[2:0] = 100	-	202	-	Ω
		data byte 12h bits INATT[2:0] = 101	-	202	-	Ω
		data byte 12h bits INATT[2:0] = 110	-	76	-	Ω
		data byte 12h bits INATT[2:0] = 111	-	32	-	Ω
C_i	input capacitance	differential on pin FM_IN_P to pin FM_IN_N	-	7	-	pF
$G_{FM(step)}$	step of FM gain	$G_{FM(stepN)} - G_{FM(stepN-1)}$ with N = 1 to 7 (read data byte 12h bits INATT[2:0])	4	6	7.5	dB

[1] Default weak signal handling settings as described in the radio user manual.

[2] Signal strength register readout.

Table 156. Dynamic characteristics for AM path

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; tests on RF level are done with a capacitive dummy antenna aerial 15 pF/60 pF; levels refer to dummy input; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM system						
f_{RF}	RF frequency	AM (LW) tuning range	144	-	288	kHz
		AM (MW) tuning range	522	-	1710	kHz
		AM (SW) tuning range	2.3	-	27.0	MHz
$f_{tune(step)}$	step of tuning frequency	AM tuning step size	-	1	-	kHz
f_{IF}	IF frequency	f_{xtal} = 62.4 MHz; AM MW and SW bands	-	57	-	kHz

Table 156. Dynamic characteristics for AM path *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; tests on RF level are done with a capacitive dummy antenna aerial 15 pF/60 pF; levels refer to dummy input; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(sens)}$	input sensitivity voltage	(S+N)/N = 26 dB; B_{aud} = 2 kHz; f_{RF} = 990 kHz; m = 30 %; f_{AF} = 400 Hz				
		weak signal handling off	-	34	-	dBµV
		weak signal handling on; default settings	-	30	-	dBµV
(S+N)/N	signal plus noise-to-noise ratio	$V_{i(RF)}$ = 74 dBµV; m = 30 %	-	68	-	dB
THD	total harmonic distortion	$V_{i(RF)}$ = 74 dBµV				
		f_{AF} = 1 kHz; m = 30 %	-	0.02	0.1	%
		f_{AF} = 100 Hz; m = 30 %	-	0.03	0.1	%
		f_{AF} = 1 kHz; m = 80 %	-	0.07	0.2	%
		f_{AF} = 100 Hz; m = 80 %	-	0.15	0.3	%
α_{image}	image rejection	$f_{RF(image)} = f_{RF(wanted)} \pm 2 \times f_{IF}$	100	-	-	dB
$\alpha_{rej(IF)}$	IF rejection		80	92	-	dB
S_{stat}	static selectivity	single signal; Δf_{RF} = 10 kHz; $f_{tune} \pm 10$ kHz	70	80	-	dB
		single signal; Δf_{RF} = 20 kHz; $f_{tune} \pm 20$ kHz	80	-	-	dB
IP3	third-order intercept point	f_{RF} = 990 kHz; $f_{RF(unw)1}$ = 1030 kHz; $f_{RF(unw)2}$ = 1070 kHz	130	133	-	dBµV
		f_{RF} = 990 kHz; $f_{RF(unw)1}$ = 1290 kHz; $f_{RF(unw)2}$ = 1590 kHz	140	145	-	dBµV
IP2	second-order intercept point	f_{RF} = 1400 kHz; $f_{RF(unw)1}$ = 600 kHz; $f_{RF(unw)2}$ = 800 kHz	160	170	-	dBµV
AM LNA and AGC (input pin AM_IN_P; output pins LNA_OUT_P and LNA_OUT_N; AGC capacitor pin AM_LNA_CAP)						
$V_{AM\_LNA\_CAP}$	voltage on pin AM_LNA_CAP		0.4	0.6	0.8	V
$V_{LNA\_OUT\_P}$	voltage on pin LNA_OUT_P		1.3	1.4	1.5	V
$V_{LNA\_OUT\_N}$	voltage on pin LNA_OUT_N		1.3	1.4	1.5	V
G_{LNA}	LNA gain	gain from input of passive antenna dummy to differential LNA output (pins LNA_OUT_P and LNA_OUT_N)	5.0	6.5	8.0	dB
C_i	input capacitance	data byte 4h bit ANT = 0	-	274	-	pF
$V_{i(max)}$	maximum input voltage	THD < 3 %; m = 80 %; f_{AF} = 400 Hz				
		capacitive antenna 15 pF/60 pF	136	139	-	dBµV
		active antenna 50 Ω	124	-	-	dBµV

Table 156. Dynamic characteristics for AM path *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; tests on RF level are done with a capacitive dummy antenna aerial 15 pF/60 pF; levels refer to dummy input; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(RF)AGC(start)}$	start AGC RF input voltage	in-band threshold; data byte 0 bits BAND[1:0] = 10 (AM MW); f_{RF} = 990 kHz; f_{tune} = 990 kHz; m = 0 %				
		data byte 3h bits RFAGC[1:0] = 00	92	96	100	dBµV
		data byte 3h bits RFAGC[1:0] = 01	89	93	97	dBµV
		data byte 3h bits RFAGC[1:0] = 10	86	90	94	dBµV
		data byte 3h bits RFAGC[1:0] = 11	83	87	91	dBµV
		wideband threshold; data byte 0 bits BAND[1:0] = 10 (AM MW); f_{RF} = 1500 kHz; f_{tune} = 990 kHz; m = 0 %	104	107	110	dBµV
$\alpha_{cr(AGC)}$	AGC control range		57	60	63	dB
$G_{AM(step)}$	step of AM gain	$G_{AM(stepN)} - G_{AM(stepN-1)}$ with N = 1 to 10 (read data byte 12h bits INATT[2:0] plus FBATT[1:0]	5	6	7	dB
N_{LEV}	LEV value	V_{RF} = 60 dBµV; f_{RF} = 1 MHz; m = 0; data byte 0Ch; LEVO[5:0] = 10 1110 (level offset = −2 dB) [1]	130	136	142	
AM RF filter						
AM LW low-pass filter						
f_{-3dB}	cut-off frequency	data byte 0 bits BAND[1:0] = 01 (AM LW); f_{RF} = 100 kHz for 0 dB reference; L = 560 µH (external inductor)	360	415	470	kHz
AM MW band-pass filter						
B_i	input bandwidth	data byte 0 bits BAND[1:0] = 10 (AM MW); f_{RF} = 990 kHz; L = 560 µH (external inductor)	-	215	-	kHz
AM SW high-pass filter						
f_{-3dB}	cut-off frequency	data byte 0 bits BAND[1:0] = 11 (AM SW); f_{RF} = 5 MHz for 0 dB reference	1.5	2	2.3	MHz
AM mixer (input pins AM_MIX_IN_P and AM_MIX_IN_N)						
$V_{AM\_MIX\_IN\_P}$	voltage on pin AM_MIX_IN_P		0.65	0.75	0.85	V
$V_{AM\_MIX\_IN\_N}$	voltage on pin AM_MIX_IN_N		0.65	0.75	0.85	V
R_i	input resistance	data byte 0 bits BAND[1:0] = 01 (AM LW)	-	1.3	-	kΩ
		data byte 0 bits BAND[1:0] = 10 (AM MW)	-	33.8	-	kΩ

Table 156. Dynamic characteristics for AM path *...continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; all AC values are given in RMS; tests on RF level are done with a capacitive dummy antenna aerial 15 pF/60 pF; levels refer to dummy input; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_i	input capacitance	data byte 0 bits BAND[1:0] = 01 (AM LW)	190	235	280	pF
		data byte 0 bits BAND[1:0] = 10 (AM MW)				
		minimum capacitance	-	10	-	pF
		maximum capacitance	190	235	280	pF

[1] Signal strength register readout.

Table 157. I²S-bus interface characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	sampling frequency	asynchronous I²S inputs	8	-	48	kHz
T_{cy}	clock cycle time	[1]	320	-	-	ns
t_r	rise time		-	-	$0.15 \times T_{cy}$	ns
t_f	fall time		-	-	$0.15 \times T_{cy}$	ns
$t_{BCK(H)}$	bit clock time HIGH		$0.35 \times T_{cy}$	-	-	ns
$t_{BCK(L)}$	bit clock time LOW		$0.35 \times T_{cy}$	-	-	ns
$t_{s;DAT}$	data set-up time		$0.2 \times T_{cy}$	-	-	ns
$t_{h;DAT}$	data hold time		$0.2 \times T_{cy}$	-	-	ns
$t_{d;DAT}$	data delay time		-	-	$0.15 \times T_{cy}$	ns
$t_{s;WS}$	word select set-up time		$0.2 \times T_{cy}$	-	-	ns
$t_{h;WS}$	word select hold time		$0.2 \times T_{cy}$	-	-	ns

[1] The bit clock frequency is: $f_{clk} = 64 \times f_s$ and the clock cycle time: $T_{cy} = 1/f_{clk}$.

Table 158. HD Radio interface characteristics

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; $V_{DDD(1V2)}$ = 1.2 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	sampling frequency		-	650	675	kHz
T_{cy}	clock cycle time	[1]	92.5	96.15	-	ns
t_r	rise time		-	-	14	ns
t_f	fall time		-	-	14	ns
$t_{BCK(H)}$	bit clock time HIGH		34	-	-	ns
$t_{BCK(L)}$	bit clock time LOW		34	-	-	ns
$t_{d;DAT}$	data delay time		-	-	14	ns

[1] The bit clock frequency is: $f_{clk} = 16 \times f_s$ and the clock cycle time: $T_{cy} = 1/f_{clk}$ and the word select frequency is: $f_{ws} = f_s/2$.

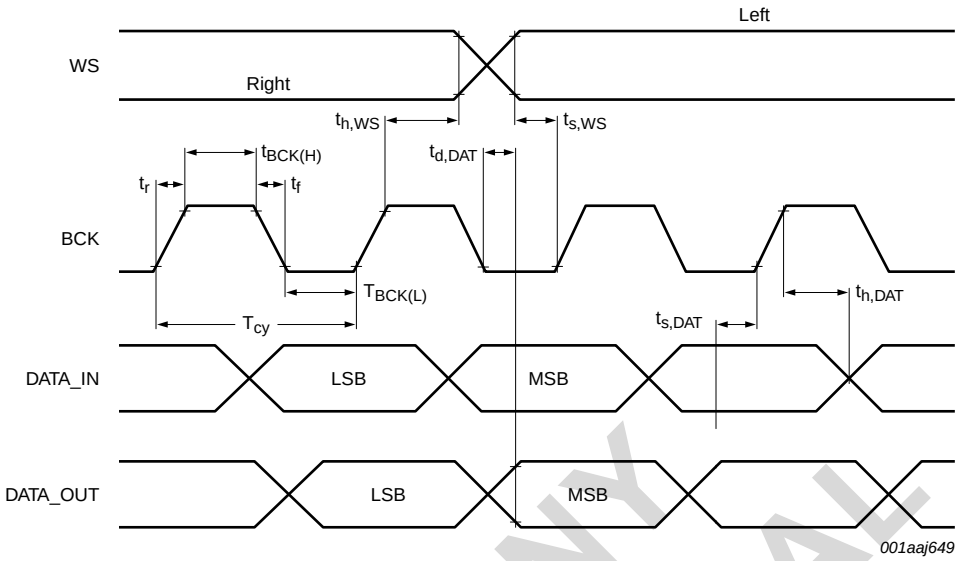


Fig 11. Input timing of digital audio data inputs and outputs

Table 159. Dynamic characteristics for RESETN

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{w(rst)}$	reset pulse width	LOW input level on pin RESETN	1	-	-	µs

Table 160. Analog S/PDIF characteristics

Recommended operating conditions; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{i(a)(p-p)}$	peak-to-peak analog input voltage		0.2	-	1	V
R_i	input resistance	V_i = 3.3 V	5.5	8.5	14	kΩ
$V_{hys(i)}$	input hysteresis voltage		30	38	46	mV

13. Application information

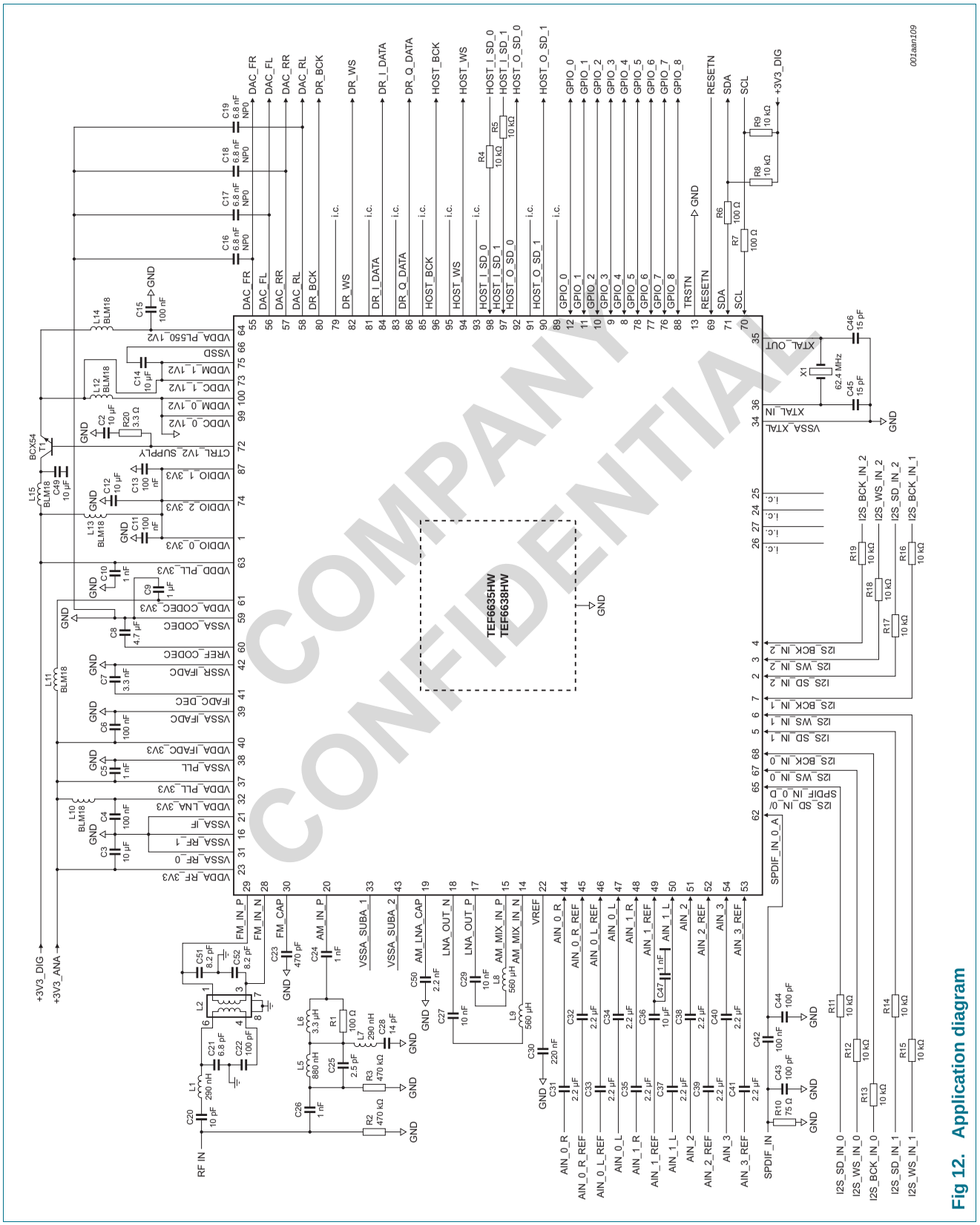


Fig 12. Application diagram

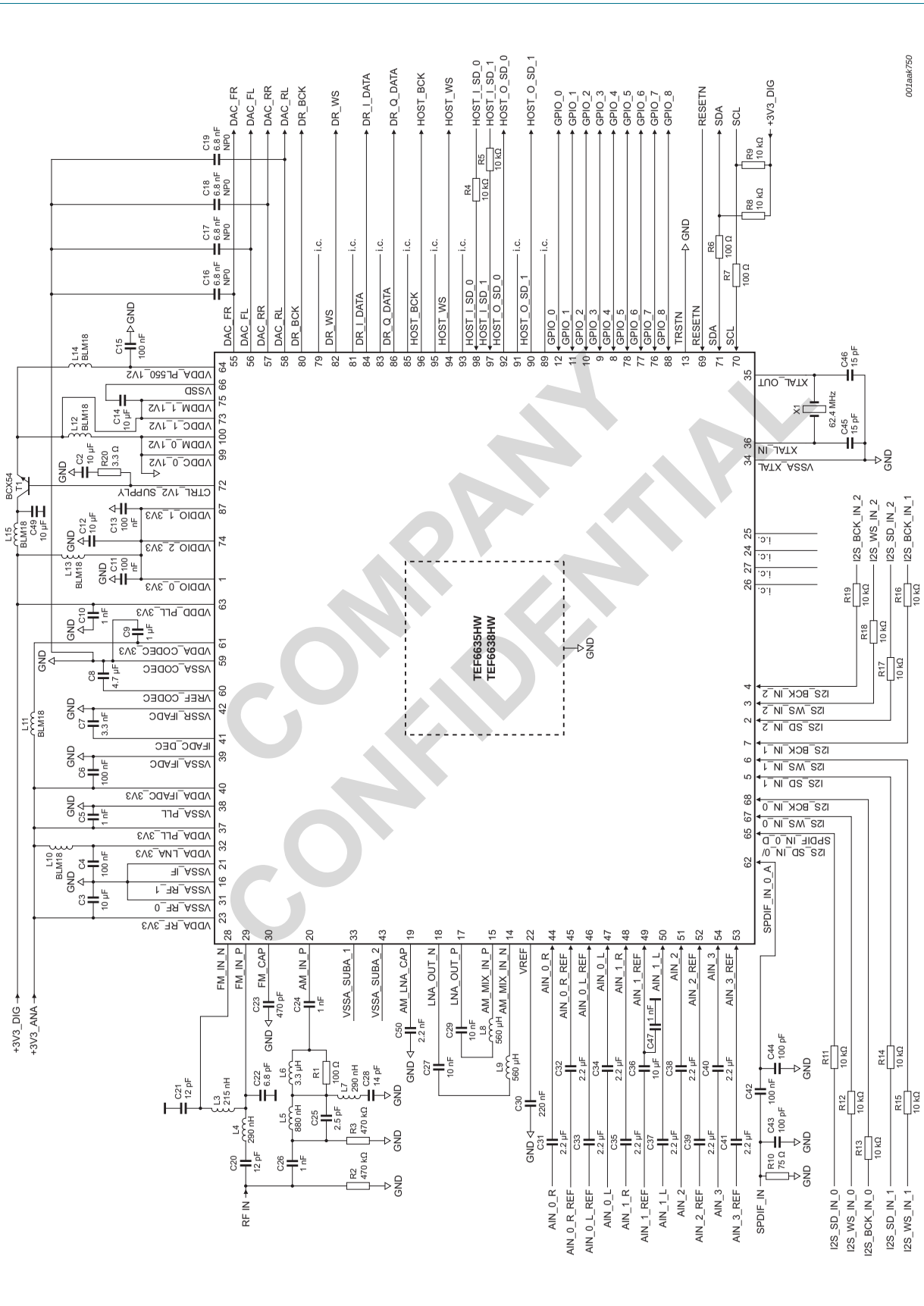


Fig 13. Low cost application diagram (no transformer at FM input)

Table 161. List of components for Figure 12 and Figure 13

Symbol	Type	Series	Manufacturer
L1	LQH31HNR29J03L	LQH31	Murata
L2	#A638AN-A163YXO	5CCE	Toko
L3	LQH31HNR21K01L	LQH31	Murata
L4	LQH31HNR29J03L	LQH31	Murata
L5	LQH31HNR88K03	LQH31	Murata
L6	LLM2520-3R3K	LLM2520	Toko
L7	LQH31HNR29J03L	LQH31	Murata
L8 and L9	LQH43MN561K03L	LQH43	Murata
L10 to L15	BLM18EG601SN1	BLM18	Murata
X1	1C262400CCOA	DSX321G	KDS
	EXSOOA-CGO1288	NX3225GA	NDK

Table 162. DC operating points

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
VDDIO_0_3V3	1	external 3.3 V			external 3.3 V		
I2S_SD_IN_2[1]	2	-	1.1	-	-	1.1	-
I2S_WS_IN_2[1]	3	-	1.1	-	-	1.1	-
I2S_BCK_IN_2[1]	4	-	1.1	-	-	1.1	-
I2S_SD_IN_1	5	-	1.1	-	-	1.1	-
I2S_WS_IN_1	6	-	1.1	-	-	1.1	-
I2S_BCK_IN_1	7	-	1.1	-	-	1.1	-
GPIO_4	8	-	0/3.3	-	-	0/3.3	-
GPIO_3	9	-	0/3.3	-	-	0/3.3	-
GPIO_2	10	-	0/3.3	-	-	0/3.3	-
GPIO_1	11	-	0/3.3	-	-	0/3.3	-
GPIO_0	12	-	0/3.3	-	-	0/3.3	-
TRSTN	13	external GND			external GND		
AM_MIX_IN_N	14	-	0	-	0.65	0.75	0.85
AM_MIX_IN_P	15	-	0	-	0.65	0.75	0.85
VSSA_RF_1	16	external GND			external GND		
LNA_OUT_P	17	-	0	-	1.3	1.4	1.5
LNA_OUT_N	18	-	0	-	1.3	1.4	1.5
AM_LNA_CAP	19	-	0	-	0.4	0.6	0.8
AM_IN_P	20	-	0	-	-	0.63	-
VSSA_IF	21	external GND			external GND		
VREF	22	2.375	2.5	2.65	2.375	2.5	2.65
VDDA_RF_3V3	23	external 3.3 V			external 3.3 V		
i.c.	24	-	0	-	-	0	-

Table 162. DC operating points *…continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
i.c.	25	-	0	-	-	0	-
i.c.	26	-	0	-	-	0	-
i.c.	27	-	0	-	-	0	-
FM_IN_N	28	1.15	1.27	1.45	-	1.54	-
FM_IN_P	29	1.15	1.27	1.45	-	1.54	-
FM_CAP	30	-	1.27	-	-	1.54	-
VSSA_RF_0	31	external GND			external GND		
VDDA_LNA_3V3	32	external 3.3 V			external 3.3 V		
VSSA_SUBA_1	33	external GND			external GND		
VSSA_XTAL	34	external GND			external GND		
XTAL_OUT	35	-	0.58	-	-	0.58	-
XTAL_IN	36	-	0.58	-	-	0.58	-
VDDA_PLL_3V3	37	external 3.3 V			external 3.3 V		
VSSA_PLL	38	external GND			external GND		
VSSA_IFADC	39	external GND			external GND		
VDDA_IFADC_3V3	40	external 3.3 V			external 3.3 V		
IFADC_DEC	41	2.35	2.5	2.65	2.35	2.5	2.65
VSSR_IFADC	42	-	0	-	-	0	-
VSSA_SUBA_2	43	external GND			external GND		
AIN_0_R[1]	44	-	1.24	-	-	1.24	-
AIN_0_R_REF[1]	45	-	1.24	-	-	1.24	-
AIN_0_L_REF[1]	46	-	1.24	-	-	1.24	-
AIN_0_L[1]	47	-	1.24	-	-	1.24	-
AIN_1_R	48	-	1.24	-	-	1.24	-
AIN_1_REF	49	-	1.24	-	-	1.24	-
AIN_1_L	50	-	1.24	-	-	1.24	-
AIN_2	51	-	1.24	-	-	1.24	-
AIN_2_REF	52	-	1.24	-	-	1.24	-
AIN_3_REF	53	-	1.24	-	-	1.24	-
AIN_3	54	-	1.24	-	-	1.24	-
DAC_FR	55	-	1.61	-	-	1.61	-
DAC_FL	56	-	1.61	-	-	1.61	-
DAC_RR	57	-	1.61	-	-	1.61	-
DAC_RL	58	-	1.61	-	-	1.61	-
VSSA_CODEC	59	external GND			external GND		
VREF_CODEC	60	-	1.24 (high-ohmic)	-	-	1.24 (high-ohmic)	-
VDDA_CODEC_3V3	61	external 3.3 V			external 3.3 V		

Table 162. DC operating points *…continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
SPDIF_IN_0_A	62	-	0.15	-	-	0.15	-
VDDD_PLL_3V3	63	external 3.3 V			external 3.3 V		
VDDA_PL550_1V2	64	external 1.2 V			external 1.2 V		
I2S_SD_IN_0/SPDIF_IN_0_D	65	-	1.1	-	-	1.1	-
VSSD	66	external GND			external GND		
I2S_WS_IN_0	67	-	1.1	-	-	1.1	-
I2S_BCK_IN_0	68	-	1.1	-	-	1.1	-
RESETN	69	-	3.3	-	-	3.3	-
SCL	70	external I^2C-bus voltage			external I^2C-bus voltage		
SDA	71	external I^2C-bus voltage			external I^2C-bus voltage		
CTRL_1V2_SUPPLY	72	-	1.85	-	-	1.85	-
VDDC_1_1V2	73	external 1.2 V			external 1.2 V		
VDDIO_2_3V3	74	external 3.3 V			external 3.3 V		
VDDM_1_1V2	75	external 1.2 V			external 1.2 V		
GPIO_7	76	-	0/3.3	-	-	0/3.3	-
GPIO_6	77	-	0/3.3	-	-	0/3.3	-
GPIO_5	78	-	0/3.3	-	-	0/3.3	-
i.c.	79	-	0/3.3	-	-	0/3.3	-
DR_BCK[1]	80	-	0/3.3	-	-	0/3.3	-
i.c.	81	-	0/3.3	-	-	0/3.3	-
DR_WS[1]	82	-	0/3.3	-	-	0/3.3	-
i.c.	83	-	0/3.3	-	-	0/3.3	-
DR_I_DATA[1]	84	-	0/3.3	-	-	0/3.3	-
i.c.	85	-	0/3.3	-	-	0/3.3	-
DR_Q_DATA[1]	86	-	0/3.3	-	-	0/3.3	-
VDDIO_1_3V3	87	external 3.3 V			external 3.3 V		
GPIO_8	88	-	0/3.3	-	-	0/3.3	-
i.c.	89	-	0/3.3	-	-	0/3.3	-
HOST_O_SD_1[1]	90	-	0/3.3	-	-	0/3.3	-
i.c.	91	-	0/3.3	-	-	0/3.3	-
HOST_O_SD_0	92	-	0/3.3	-	-	0/3.3	-
i.c.	93	-	0/3.3	-	-	0/3.3	-
HOST_WS	94	-	0/3.3	-	-	0/3.3	-
i.c.	95	-	0/3.3	-	-	0/3.3	-
HOST_BCK	96	-	0/3.3	-	-	0/3.3	-
HOST_I_SD_1[1]	97	-	1.1	-	-	1.1	-

Table 162. DC operating points *…continued*

$V_{DDA(3V3)}$ = 3.3 V; $V_{DDD(3V3)}$ = 3.3 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Pin	Unloaded DC voltage (V)					
		FM mode			AM mode		
		Min	Typ	Max	Min	Typ	Max
HOST_I_SD_0	98	-	1.1	-	-	1.1	-
VDDC_0_1V2	99	external 1.2 V			external 1.2 V		
VDDM_0_1V2	100	external 1.2 V			external 1.2 V		

[1] This pin is internally connected for the TEF6635. The function is only available in TEF6638.

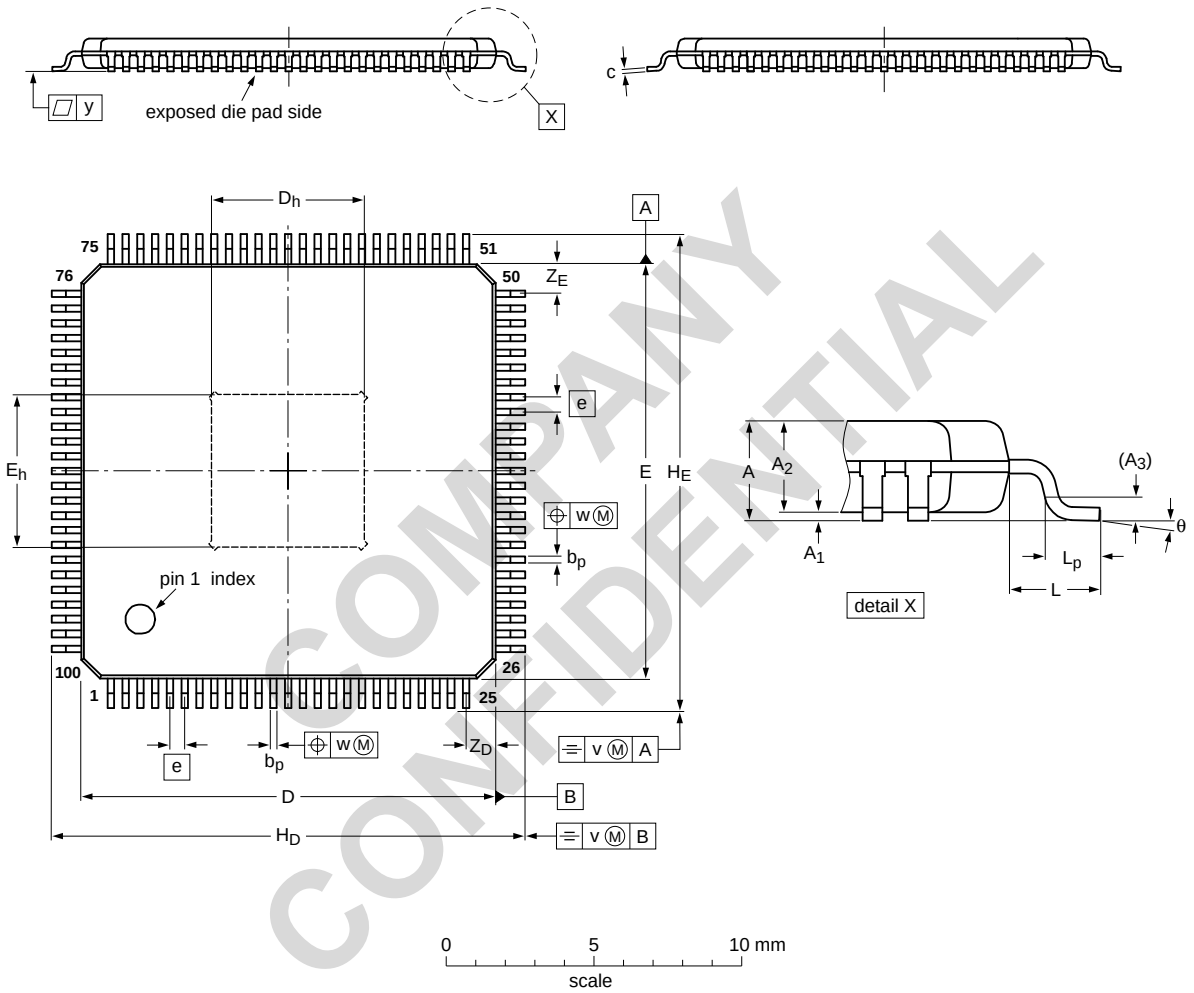
14. Test information

14.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

15. Package outline

HTQFP100: plastic thermal enhanced thin quad flat package; 100 leads; body 14 x 14 x 1 mm; exposed diepad **SOT638-3**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	max	1.20	0.15	1.05		0.27	0.20	14.1	5.7	14.1	5.7		16.15	16.15		0.75				1.15	1.15	7°
	nom	1.00	0.10	1.00	0.25	0.22	0.15	14.0	5.2	14.0	5.2	0.5	16.00	16.00	1	0.60	0.2	0.08	0.08	1.00	1.00	
	min	0.95	0.05	0.95		0.17	0.09	13.9	4.7	13.9	4.7		15.85	15.85		0.45				0.85	0.85	0°

Note

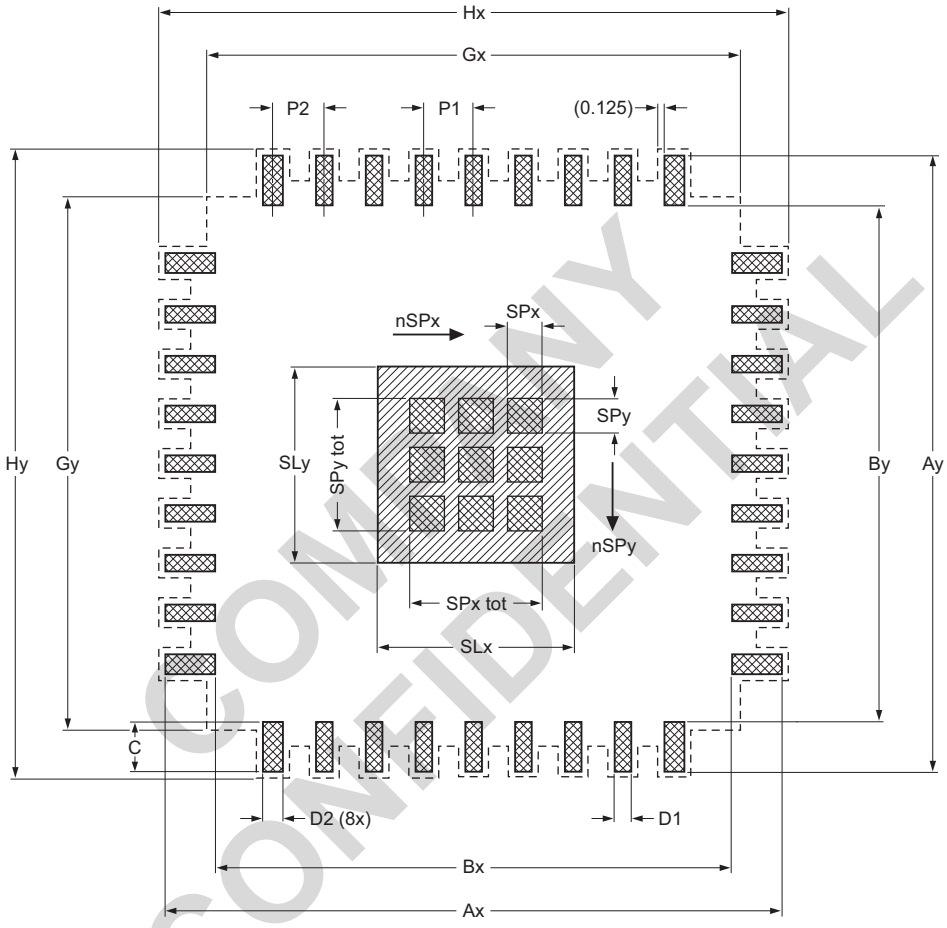
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT638-3		MS-026				~~08-03-06~~ 08-04-08

Fig 14. Package outline SOT638-3 (HTQFP100)

16. Soldering

Footprint information for reflow soldering of HTQFP100 package **SOT638-3**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

solder paste

occupied area

nSPx	nSPy
4	4

DIMENSIONS in mm

P1	P2	Ax	Ay	Bx	By	C	D1	D2	Gx	Gy	Hx	Hy	SLx	SLy	SPx tot	SPy tot	SPx	SPy
0.500	0.560	17.300	17.300	14.300	14.300	1.500	0.280	0.400	14.500	14.500	17.550	17.550	5.500	5.500	3.100	3.100	0.900	0.900

Fig 15. Soldering footprint SOT638-3 (HTQFP100)

17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 16) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 163 and 164

Table 163. SnPb eutectic process (from J-STD-020C)

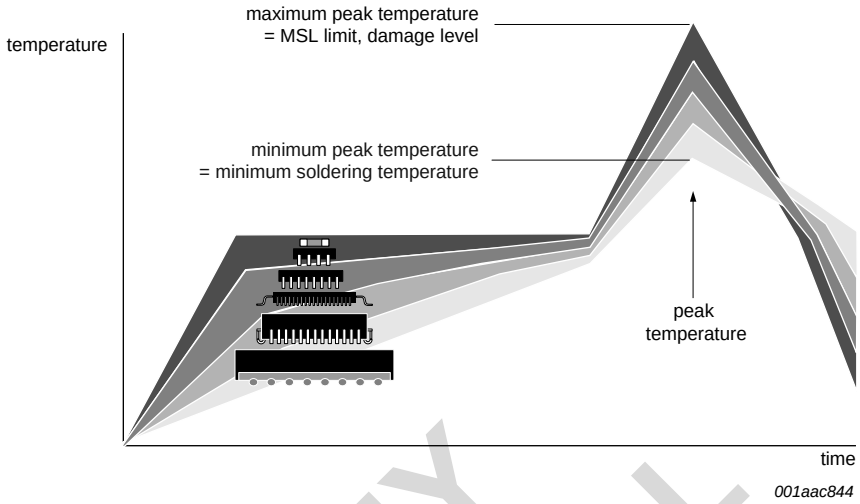
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 164. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 16.



MSL: Moisture Sensitivity Level

Fig 16. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

18. Abbreviations

Table 165. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AFU	Alternative Frequency Update
AGC	Automatic Gain Control
API	Application Programming Interface
AUX	AUXiliary
BCK	Bit ClocK
BPF	Band-Pass Filter
CD	Compact Disc
CEQ	Channel EQualization
CMOS	Complementary Metal-Oxide Semiconductor
CNS	Click Noise Suppression
DAC	Digital-to-Analog Converter
DCO	Digital Controlled Oscillator
DRM	Digital Radio Mondiale
DSP	Digital Signal Processor
EMS	Enhanced Multipath Suppression
GPIO	General Purpose Input Output
I/Q	In-phase/Quadrature-phase
I^2C-bus	Inter IC bus
I^2S	Inter IC Sound
IC	Integrated Circuit
IF	Intermediate Frequency
IIR	Infinite Impulse Response
LNA	Low-Noise Amplifier
LO	Local Oscillator
LW	Long Wave
MPX	MultiPleX
MUX	MUltipleXer
MW	Medium Wave
OEM	Original Equipment Manufacturer
OSC	OSCillator
PACS	Precision Adjacent Channel Suppression
PCB	Printed-Circuit Board
PDC	Park Distance Control
PI	Programme Identification
PLL	Phase-Locked Loop
RBDS	Radio Broadcast Data System
RDCL	RDS Demodulator CLock
RDDA	RDS Demodulator DAta

Table 165. Abbreviations *...continued*

Acronym	Description
RDS	Radio Data System
RF	Radio Frequency
RMS	Root Mean Square
RSSI	Received Signal Strength Indicator
SD	Sigma-Delta
SPDIF	Sony Philips Digital InterFace
SRC	Sample Rate Converter
SW	Short Wave
USN	UltraSonic Noise
WAM	Wideband AM
WB	Weather Band
WS	Word Select
XTAL	CrysTAL

19. References

[1] **User Manual 10204 Rev. 03, 19 June 2007 —** Technical information

[2] **The I²C-bus Specification, Version 2.1 —** Official I²S Standard Document (available from NXP Semiconductors, International Marketing and Sales

[3] **IEC 60134 —** Absolute Maximum Rating System

[4] **AEC - Q100-004 —** Automotive Electronics Council - IC Latch Up Test

[5] **AEC - Q100-002 —** Automotive Electronics Council - Human Body Model (HBM) Electrostatic Discharge (ESD) Test

[6] **AEC - Q100-011 —** Automotive Electronics Council - Charged Device Model (CDM) Electrostatic Discharge (ESD) Test

[7] **JESD22-A114 —** JEDEC Standard - Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[8] **JESD22-C101 —** JEDEC Standard - Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[9] **Application Note AN10365 —** “Surface mount reflow soldering description”

[10] **Application Note AN11092 —** “TEF6635/38 single-chip car radio”

20. Revision history

Table 166. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEF6635_TEF6638 v.2	20110719	Product data sheet	-	TEF6635_TEF6638 v.1
TEF6635_TEF6638 v.1	20110715	Preliminary data sheet	not published	-

21. Legal information

21.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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23. Tables

24. Figures

25. Contents

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