STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • FAX: 516-231-6004

COM92C451

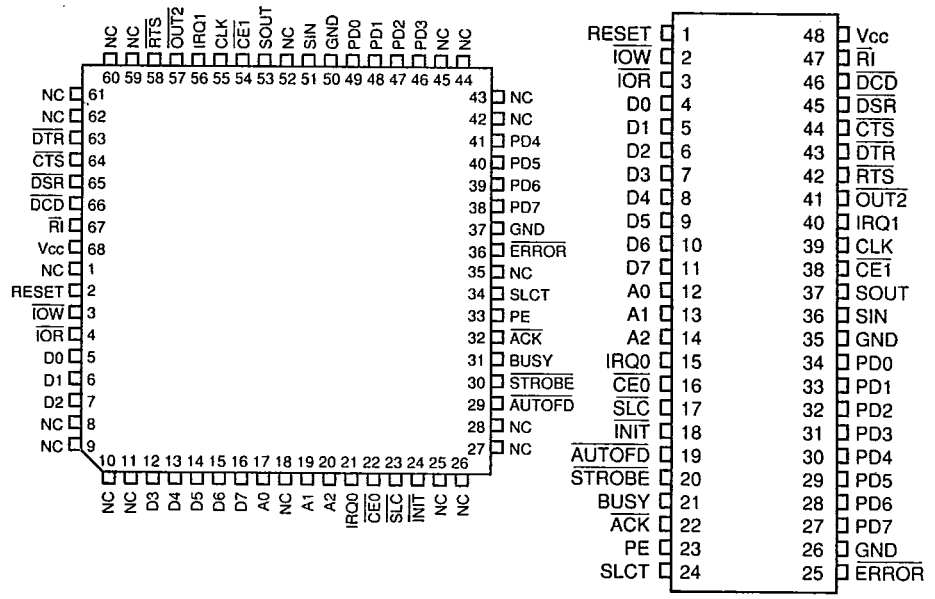
T-75-37-05

Combination UART/Printer Interface

FEATURES

- ☐ Fully IBM PC®, PC XT®, PC AT® Compatible
- ☐ Easily Interfaces to Most Popular Microprocessors
- ☐ Replaces Both the 16C450 and Parallel Port to Reduce Cost and Space
- ☐ Compatible with Industry Standards 16C450 and 82C50A
- ☐ Fully Programmable UART Characteristics:
  - 5-, 6-, 7-, or 8-Bit Characters
  - 1, 1.5, or 2 Stop Bit Generation
  - Even, Odd, or No Parity Bit Generation and Detection
  - Baud Rate Generator (DC to 625 KBaud)
- ☐ Internal Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to 65,535 to Generate 16x Clock of up to 10 MHz
- ☐ Provides Full Individual Modem Control Functions
- ☐ Independent and Prioritized Transmit, Receive, Line Status, and Modem Interrupts
- ☐ False Start Bit Detection
- ☐ Complete Status Reporting Capabilities
- ☐ Line Break Generation and Detection
- ☐ Internal Diagnostics Capabilities Include:
  - Loopback Controls for Communications Link Fault Isolation and
  - Break, Parity Overrun, Framing Error Simulation
- ☐ Full Double Buffering to Eliminate Need for Precise Synchronization Between CPU and Serial Data
- ☐ Independent Receiver Clock Input
- ☐ High Impedance TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- ☐ Fully Compatible with Centronics Parallel Port
- ☐ Provides Latched Data and Control Signals to Printer
- ☐ Provides Printer Status Port
- ☐ Low Power CMOS, +5V Supply

PIN CONFIGURATION



Packages: 68-Pin PLCC or 48-Pin DIP

Ordering Information: COM92C451 LJP for PLCC
COM92C451 P for DIP

GENERAL DESCRIPTION

The COM92C451 is a CMOS device which is fully compatible with the IBM PC/AT and may reside on the motherboard to replace both a serial data input/output interface and a parallel port. The serial port is a UART with special modem control signals. The system software configures the UART via the 8-bit bidirectional data bus.

The UART performs serial-to-parallel conversions on data characters received from peripheral devices or modems, and parallel-to-serial conversions on data characters from the microprocessor. The UART includes a programmable baud rate generator capable of dividing the input clock by 1 to 65,535, generating a 16x clock of up to 10 MHz, giving a maximum baud rate of 625 KBaud. Individual, prioritized interrupts can be programmed to the requirements of the user, providing utmost flexibility.

The Parallel Port contains a bidirectional parallel data port which may store information from the UART en route to the printer. The parallel port also contains a control register and a status register, allowing the microprocessor to fully communicate with the printer.

The registers of the COM92C451 are addressable via the A0-A2 bus and the microprocessor may communicate with the registers at any time by reading or writing the information on the D0-D7 lines.

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DESCRIPTION OF PIN FUNCTIONS

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PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
PROCESSOR INTERFACE				
17, 19-20	12-14	Address 0-2	A0-A2	Input. These signals are used to decode the registers of the Asynchronous Communications Element (ACE) or printer Interface Adapter (PIA).
5-7, 12-16	4-11	Data 0-7	D0-D7	Input/Output. These signals are used to transfer data, status, and control words between the COM92C451 and the microprocessor. These signals are in the high impedance state when not active.
4	3	$\overline{\text{I/O Read}}$	$\overline{\text{IOR}}$	Input. This active low signal is used by the microprocessor to read data from the COM92C451. A low level on this pin outputs data onto the D0-D7 pins.
3	2	$\overline{\text{I/O Write}}$	$\overline{\text{IOW}}$	Input. This active low signal is used by the microprocessor to write data to the COM92C451. The data is latched onto the D0-D7 pins on the rising edge of this signal. A low level on this pin and on $\overline{\text{CE0}}$ and $\overline{\text{CE1}}$ simultaneously puts the COM92C451 into an ACE Baud Rate Test Mode.
22	16	$\overline{\text{Chip Enable 0}}$	$\overline{\text{CE0}}$	Input. This active low signal is used to enable the PIA. Whenever access to the Printer Interface is required, this signal must be held stable at a logic "0". A low level on this pin and on $\overline{\text{IOW}}$ and $\overline{\text{CE1}}$ simultaneously will put the COM92C451 into the ACE Baud Rate Test Mode. A low level on $\overline{\text{CE0}}$ and $\overline{\text{CE1}}$ without $\overline{\text{IOW}}$ held low is an illegal condition.
54	38	$\overline{\text{Chip Enable 1}}$	$\overline{\text{CE1}}$	Input. This active low signal is used to enable the ACE. Whenever access to the ACE is required, this signal must be held stable at a logic "0". A low level on this pin and on $\overline{\text{IOW}}$ and $\overline{\text{CE0}}$ simultaneously will put the COM92C451 into the ACE Baud Rate Test Mode. A low level on $\overline{\text{CE0}}$ and $\overline{\text{CE1}}$ without $\overline{\text{IOW}}$ held low is an illegal condition.
21	15	Interrupt Request 0	IRQ0	Output. This active high signal is used by the PIA to interrupt the processor. This signal is enabled by setting bit 4 of the Printer Interface Control Register to a logic "1", and is otherwise in the high impedance state.
56	40	Interrupt Request 1	IRQ1	Output. This active high signal is used by the ACE to interrupt the processor. This signal is enabled by setting the appropriate bits in the Interrupt Enable Register to a logic "1" (see the Internal Registers section of this document).
2	1	Reset	RESET	Input. This active high signal resets the COM92C451 to its initial state. A hard reset clears the Data Register and the Control Register of the PIA and clears all registers of the ACE except for the Receiver Buffer, the Transmitter Holding Register and the Divisor Latches.
PARALLEL INTERFACE				
49-46, 41-38	34-37	Printer Data 0-7	PD0-PD7	Input/Output. These signals carry the data stored in the Printer Interface Data Register to and from the printer via non-inverting buffers.
23	17	$\overline{\text{Printer Select}}$	$\overline{\text{SLC}}$	Output. This active low, open-drain signal is used to select the printer. This signal is the complement of bit 3 of the Printer Control Register and is in the high impedance state when not active.
24	18	$\overline{\text{Initiate}}$	$\overline{\text{INIT}}$	Output. This active low, open-drain signal is used to clear the printer buffer. This signal is bit 2 of the Printer Control Register and is in the high impedance state when not active.
29	19	$\overline{\text{Auto Feed}}$	$\overline{\text{AUTOFD}}$	Output. This active low, open-drain signal is used to feed the printer automatically. This signal is the complement of bit 1 of the Printer Control Register and is in the high impedance state when not active.
30	20	$\overline{\text{Strobe}}$	$\overline{\text{STROBE}}$	Output. This active low, open-drain signal is used to strobe the printer data into the printer. This signal is the complement of bit 0 of the Printer Control Register and is in the high impedance state when not active.

DESCRIPTION OF PIN FUNCTIONS (CONTINUED)

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PLCC PIN NO.	DIP PIN NO.	NAME	SYMBOL	DESCRIPTION
PARALLEL INTERFACE (CONTINUED)				
31	21	Busy	BUSY	Input. This active high signal is used to tell the COM92C451 that the printer is not ready to receive new data. This signal is the complement of bit 7 of the Printer Status Register.
32	22	Acknowledge	$\overline{ACK}$	Input. This active low signal is used to tell the COM92C451 that the printer has received the data and is ready to accept new data. This signal is bit 6 of the Printer Status Register.
33	23	Paper End	PE	Input. This active high signal is used to tell the COM92C451 that the printer is out of paper. This signal is bit 5 of the Printer Status Register.
34	24	Printer Selected Status	SLCT	Input. This active high signal is used to tell the COM92C451 that the printer has power on. This signal is bit 4 of the Printer Status Register.
36	25	Error	$\overline{ERROR}$	Input. This active low signal is used to tell the COM92C451 that there is an error condition at the printer. This signal is bit 3 of the Printer Status Register.
SERIAL INTERFACE				
51	36	Serial Input	SIN	Input. This signal carries the serial data to the receiver of the COM92C451.
53	37	Serial Output	SOUT	Output. This signal carries the serial data from the transmitter of the COM92C451.
55	39	Clock	CLK	Input. This is the clock input for the COM92C451 Baud Rate Generator.
57	41	Output 2	$\overline{OUT2}$	Output. This signal is a user-designated output which may be programmed by bit 3 of the Modem Control Register. The level of this signal is the inverse of the level programmed into the Modem Control Register.
58	42	Request to Send	$\overline{RTS}$	Output. This active low signal is used to tell the modem that the ACE is ready to transmit data.
63	43	Data Terminal Ready	$\overline{DTR}$	Output. This active low signal is used to tell the modem that the ACE is ready to communicate.
64	44	Clear to Send	$\overline{CTS}$	Input. This active low signal is used to tell the COM92C451 that the modem is ready to exchange data. This signal is the complement of bit 4 of the Modem Status Register. Bit 0 of the Modem Status Register may be read to determine whether this signal has changed state since the last reading of the Modem Status Register. $\overline{CTS}$ has no effect on the transmitter.
65	45	Data Set Ready	$\overline{DSR}$	Input. This active low signal is used to tell the COM92C451 that the modem is ready to establish the communication link with it. This signal is the complement of bit 5 of the Modem Status Register. Bit 1 of the Modem Status Register may be read to determine whether this signal has changed stae since the last reading of the Modem Status Register.
66	46	Data Carrier Detect	$\overline{DCD}$	Input. This active low signal is used to tell the COM92C451 that the data carrier has been detected by the modem. This signal is the complement of bit 7 of the Modem Status Register. Bit 3 of the Modem Status Register may be read to determine whether this signal has changed state since the last reading of the Modem Status Register. This signal has no effect on the receiver.
67	47	Ring Indicator	$\overline{RI}$	Input. This active low signal is used to tell the COM92C451 that a telephone ringing signal has been received by the modem. This signal is the complement of bit 6 of the Modem Status Register. Bit 2 of the Modem Status Register may be read to determine whether this signal has changed from a low to a high state since the last reading of the Modem Status Register.
MISCELLANEOUS				
68	48	Power Supply	VCC	+5 Volt Power Supply pin.
37, 50	26, 35	Ground	GND	Ground pins
1, 8-11,18, 25-28, 35, 42-45, 52, 59-62		No Connect	NC	Make no connection to these pins.

SYSTEM DESCRIPTION

The COM92C451 is a CMOS device which interfaces to the microprocessor and contains both a serial and a parallel port. The serial port is compatible to the industry standards 16C450 and 82C50A, providing the functionality of an asynchronous UART with on-chip Baud Rate Generator and full modem controls. The parallel port is Centronics compatible, providing an 8-bit printer data bus with a printer status register and control register.

MICROPROCESSOR INTERFACE

The left half of Figure 1 illustrates a typical COM92C451 interface to the microprocessor. The signals may be directly connected to the corresponding signals on the motherboard. The microprocessor interface consists of a 3-bit address bus, an 8-bit data bus, and a control bus. The address bus is used in accessing the internal registers of the device. During register accesses, these signals must be stable. The data bus is used to transfer data, status and control words between the microprocessor and the device. These lines are capable of driving TTL levels, and are in the high impedance state when not in use. The appropriate Chip Enable pin must be low and stable during register accesses. During a write operation, the data is latched into the appropriate register on the rising edge of $\overline{IOW}$.

PRINTER INTERFACE

The lower right half of Figure 1 illustrates a typical COM92C451 interface to the printer port. The signals may be directly connected to the corresponding signals on the motherboard. The printer interface consists of an 8-bit printer data bus, which carries the information in the data register between the printer and the microprocessor. The status of the eight control signals of the printer interface may be read from the printer status register. Please refer to the descriptions of the Printer Status and Command Registers for further detail.

UART/MODEM INTERFACE

The upper right half of Figure 1 illustrates a typical COM92C451 interface to the serial port. The signals may be directly connected to the corresponding signals on the motherboard. The serial interface consists of the serial input and output signals, as well as the modem control signals. The modem control signals may be accessed via the Modem Control and Modem Status Registers. Please refer to the descriptions of these registers for further detail.

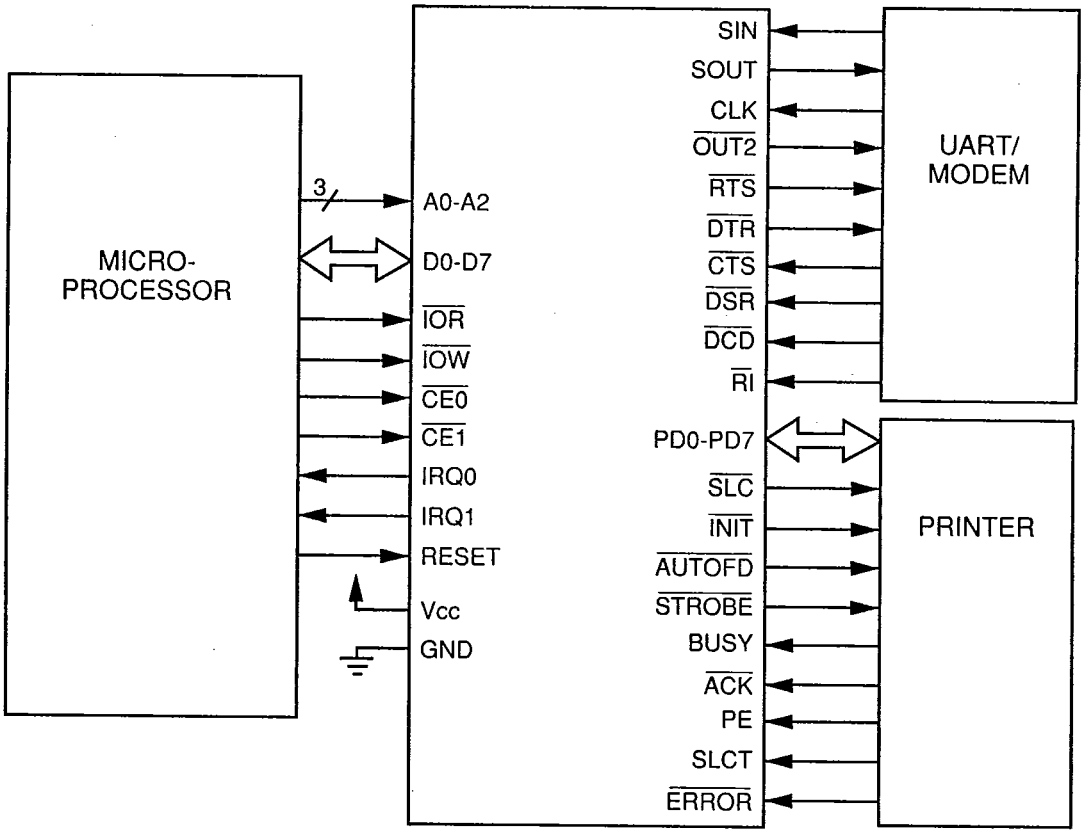

FIGURE 1 - TYPICAL SYSTEM BLOCK DIAGRAM

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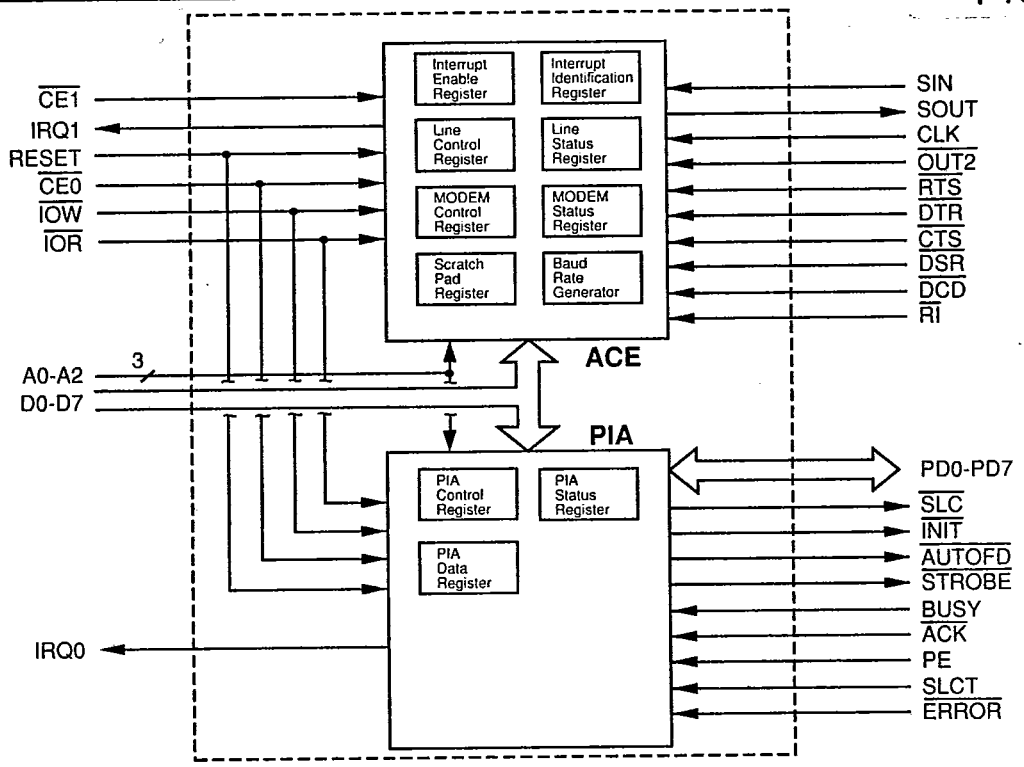

FIGURE 2 - INTERNAL BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

The COM92C451 consists of both a Printer Interface Adapter (PIA) and an Asynchronous Communications Element (ACE). Refer to Figure 2 for the Internal Block Diagram of the COM92C451. Table 1 shows the bit definitions required to access the registers in the PIA and in the ACE. Combinations other than the ones shown are illegal.

Table 1 - Register Accesses

DLAB**	$\overline{CE0}$	$\overline{CE1}$	$\overline{IOR}$	$\overline{IOW}$	A2	A1	A0	FUNCTION
X	0	1	0	1	X	0	0	Read PIA Data Register
X	0	1	1	0	X	0	0	Write PIA Data Register
X	0	1	0	1	X	1	0	Read PIA Control Register
X	0	1	1	0	X	1	0	Write PIA Control Register
X	0	1	0	1	X	0	1	Read PIA Status Register
X	1	0	0	1	0	1	1	Read ACE Line Control Register
X	1	0	1	0	0	1	1	Write ACE Line Control Register
X	1	0	0	1	1	0	1	Read ACE Line Status Register
X	1	0	0	1	1	0	0	Read ACE Modem Control Register
X	1	0	1	0	1	0	0	Write ACE Modem Control Register
X	1	0	0	1	1	1	0	Read ACE Modem Status Register
X	1	0	0	1	1	1	1	Read ACE Scratchpad Register
X	1	0	1	0	1	1	1	Write ACE Scratchpad Register
X	0	0	X	0	X	X	X	ACE Baud Rate Test Mode
0	1	0	0	1	0	0	0	Read Receiver Buffer Register
0	1	0	1	0	0	0	0	Write Transmitter Holding Register
0	1	0	0	1	0	0	1	Read Interrupt Enable Register
0	1	0	1	0	0	0	1	Write Interrupt Enable Register
X	1	0	0	1	0	1	0	Read Interrupt ID Register
1	1	0	0	1	0	0	0	Read LSB of Divisor Latch
1	1	0	1	0	0	0	0	Write LSB of Divisor Latch
1	1	0	0	1	0	0	1	Read MSB of Divisor Latch
1	1	0	1	0	0	0	1	Write MSB of Divisor Latch

**Note: DLAB is software accessable by writing bit 7 of the Line Control Register.

PRINTER INTERFACE ADAPTER

The Printer Interface Adapter provides the functions necessary to interface to an IBM PC bus and a Centronics compatible parallel port. The interfacing is accomplished through the use of the Data Port, Control Port, and Status Port, each consisting of their own registers and control gating. The bit combinations required to access the PIA registers are shown in Table 1.

PIA Data Register

The PIA Data Register is an 8-bit Read/Write register used to hold the contents of the data bus. During a Write operation, the microprocessor data bus contents are latched into the Data Register and are then presented to the PD0-PD7 lines on the rising edge of $\overline{IOW}$. During a Read operation, the PD0-PD7 contents are read and output onto the microprocessor bus D0-D7. The PIA Data Register is cleared at power up by RESET.

PIA Control Register

The PIA Control Register is an 8-bit Read/Write register which holds the control information necessary to implement a Read or Write operation. During a WRITE operation , the microprocessor data bus bit 0-4 are latched into the control register and presented to the control pins on the rising edge of $\overline{IOW}$. The PIA Control Register bits 0-4 are cleared at power up by RESET.

Table 2 - PIA Control Register

BIT	DESCRIPTION
0	During a Write operation, this bit is inverted and output onto the $\overline{STROBE}$ pin. During a Read, the level on the $\overline{STROBE}$ pin is inverted and output onto D0 of the microprocessor data bus.
1	During a Write operation, this bit is inverted and output onto the $\overline{AUTOFD}$ pin. During a Read, the level on the $\overline{AUTOFD}$ pin is inverted and output onto D1 of the microprocessor data bus.
2	During a Write operation, this bit is output onto the $\overline{INIT}$ pin. During a Read, the level on the $\overline{INIT}$ pin is output onto D2 of the microprocessor data bus.
3	During a Write operation, this bit is inverted and output onto the $\overline{SLC}$ pin. During a Read, the level on the $\overline{SLC}$ pin is inverted and output onto D3 of the microprocessor data bus.
4	This but, when set to a logic "1", enables interrupt requests from the PIA to the microprocessor. A PIA interrupt to the microprocessor occurs when the COM92C451 receives the $\overline{ACK}$ signal from the printer, indicating that the printer has received the data and is ready to accept new data.
5-7	These undefined bits are permanently logic "1" and cannot be written.

PIA Status Register

The PIA Status Register is an 8-bit Read-Only register which holds the printer status information to be read by the microprocessor. The levels on these bits are exactly the same as those input to the device from the printer, with the exception of bit 7, BUSY. The PIA Status Register is not cleared by RESET.

Table 3 - PIA Status Register T-75-37-05

BIT	BIT NAME	DESCRIPTION
0-2		These bits are permanently read as logic "0".
3	$\overline{ERROR}$	A logic "0" on this bit indicates that an error condition exists at the printer. This is the $\overline{ERROR}$ input of the COM92C451.
4	SLCT	A logic "1" on this bit indicates that the printer has power on. This is the SLCT input of the COM92C451.
5	PE	A logic "1" on this bit indicates that the printer is out of paper. This is the PE input of the COM92C451.
6	$\overline{ACK}$	A logic "0" on this bit indicates that the printer has received the data and is ready to accept new data. This is the $\overline{ACK}$ input of the COM92C451.
7	BUSY	A logic "0" on this bit indicates that the printer is not ready to receive new data. This is the complement of the BUSY input of the COM92C451.

ASYNCHRONOUS COMMUNICATIONS ELEMENT

The Asynchronous Communications Element is essentially an Asynchronous UART with a Programmable Baud Rate Generator. In addition, the ACE contains extra features such as Full Modem Controls, Modem Status, and Maskable Interrupts with Priority. The functionality of the ACE is achieved through the use of the internal baud rate generator, which can be programmed to provide a 16x baud rate of up to 10 MBaud to the internal UART, and seven internal registers. The seven registers consist of the Line Control, Line Status, Modem Control, Modem Status, Interrupt Identification, Interrupt Enable, and Scratchpad Registers. The bit combinations required to access the ACE registers are shown in Table 1.

Programmable Baud Rate Generator (and Divisor Latches DLH and DLL)

The Baud Rate Generator within the COM92C451 is capable of taking any clock input (DC to 10 MHz) and dividing it by any divisor from 1 to 65,535 to provide a 16x baud rate of up to 10 MBaud, allowing a maximum baud rate of 625 KBaud. The two 8-bit latches which store the divisor in 16-bit binary form must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded to prevent long counts on initial load.

The functionality of the internal baud rate generator is as follows: If a 0 is loaded into the Divisor Latches, then the input clock is divided by 3. If a 1 is loaded then the baud clock is the inverse of the input clock. If a two is loaded than the input clock is divided by 2 and the baud clock has a 50% duty cycle. If a 3 or greater is loaded, then the input clock is divided by that number and the baud clock is not a 50% duty cycle, but rather, low for two counts and high for the remainder of count.

Tables 4 and 5 list some commonly used baud rates.

Table 4 - Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Theoretical 16x Clock (Khz)	Actual Frequency (KHz)	Percent Error
50	2304	0.8000	0.8000	-
75	1536	1.2000	1.2000	-
110	1047	1.7600	1.7605	0.026
134.5	857	2.1520	2.1508	0.058
150	768	2.400	2.4000	-
300	384	4.8000	4.8000	-
600	192	9.6000	9.6000	-
1200	96	19.2000	19.2000	-
1800	64	28.8000	28.8000	-
2000	58	32.000	31.7793	0.69
2400	48	38.4000	38.4000	-
3600	32	57.6000	57.6000	-
4800	24	76.8000	76.8000	-
7200	16	115.2000	115.2000	-
9600	12	153.6000	153.6000	-
19200	6	307.2000	307.2000	-
38400	3	614.4000	614.4000	-
56000	2	896.0000	921.6000	2.86

Table 5 - Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Theoretical Frequency 16x Clock (KHz)	Actual Frequency 16x Clock (KHz)	Percent Error
50	3840	0.8000	0.8000	-
75	2560	1.2000	1.2000	-
110	1745	1.7600	1.7605	0.026
134.5	1428	2.1520	2.1513	0.034
150	1280	2.4000	2.4000	-
300	640	4.8000	4.8000	-
600	320	9.6000	9.6000	-
1200	160	19.2000	19.2000	-
1800	107	28.8000	28.7103	0.312
2000	96	32.0000	32.0000	-
2400	80	38.4000	38.4000	-
3600	53	57.6000	57.9623	0.629
4800	40	76.8000	76.8000	-
7200	27	115.2000	113.7778	1.235
9600	20	153.6000	153.6000	-
19200	10	307.2000	307.2000	-
38400	5	614.4000	614.4000	-
56000	3	896.0000	1024.0000	14.286

Line Control Register (LCR)

This 8-bit Read/Write register controls the configuration of the UART. The Line Control Register is cleared at power up by RESET.

Table 6 - Line Control Register

BIT	BIT NAME	DESCRIPTION
0,1	Word Length	These two bits specify the number of bits in each transmitted or received serial character as per the following table: Bit 1 / Bit 0 / Word length 0 / 0 / 5 bits 0 / 1 / 6 bits 1 / 0 / 7 bits 1 / 1 / 8 bits
2	Stop Bits	This bit specifies the number of stop bits in each transmitted or received character as per the following table: Bit 2 / Word Length (as determined by bits 0 and 1 of LCR) / Number of Stop Bits 0 / X / 1 stop bit 1 / 5 bits / 1.5 stop bits 1 / 6, 7 or 8 bits / 2 stop bits
3	Parity Enable	A logic "1" on bit 3 enables the device to generate/check the parity bit between the last data word bit and the first stop bit. The parity bit is used to generate/check an even or odd number of 1's when the data word bits and the parity bit are summed.
4	Even Parity Select	If parity is enabled, then this bit selects even or odd parity. A logic "0" on this bit generates/checks an odd number of logic "1's". A logic "1" on bit 4 generates/checks an even number of logic "1's". If parity is disabled, then this bit has no effect.
5	Stick Parity	If parity is enabled, then a logic "1" on this bit reverses the polarity of the parity bit. A logic "1" causes the parity bit to be transmitted and then detected by the receiver in the opposite state of that indicated by bit 4. A logic "0" maintains the even or odd parity. If parity is disabled, then this bit has no effect.
6	Set Break Control	A logic "1" on this bit forces the Serial Output pin of the COM92C451 to the spacing (logic "0") state. The spacing state (Break) is maintained until this bit is reset, regardless of other transmitter activity. This feature enables the ACE to alert a terminal in a communications system.
7	Divisor Latch Access	A logic "1" on this bit allows access to the Divisor Latches of the Baud Rate Generator during read or write operations. A logic "0" allows access to the Receiver Buffer Register, the Transmitter Holding Register, and the Interrupt Enable Register.

Line Status Register (LCR)

This 8-bit Read-Only register provides the status information of the conversions that are performed by the UART and provides an Interrupt if the corresponding bits of the Interrupt Enable Register are set. The Line Status Register is cleared at power up by RESET.

Table 7 - Line Status Register

BIT	BIT NAME	DESCRIPTION
0	Data Ready	A logic "1" on this bit indicates that a complete incoming character has been received and transferred into the Receiving Buffer Register. This bit, when set, will cause an interrupt if bit 0 of the Interrupt Enable Register is also set. This bit is reset when the data in the Receiver Buffer Register is read.
1	Overrun Error	A logic "1" on this bit indicates that the Receiver Buffer Register was not read before the next character was transferred into it, in which case the previous character was destroyed. This bit, when set, will cause an interrupt if bit 2 of the Interrupt Enable Register is also set. The Overrun Error bit is reset when the Status Register is read.
2	Parity Error	A logic "1" on this bit indicates that the received data character did not have the correct even or odd parity, as selected by the Even Parity Select bit of the ACE Control Register. This bit, when set, will cause an interrupt if bit 2 of the Interrupt Enable Register is also set. The Parity Error bit is reset when the Status Register is read.
3	Framing Error	A logic "1" on this bit indicates that the received character did not have a valid stop bit. When a Framing Error occurs, the ACE will try to resynchronize itself by assuming that the error was due to the next start bit, in which case it will sample the start bit twice and then proceed to accept the data. The Framing Error bit, when set, will cause an interrupt if bit 2 of the Interrupt Enable Register is also set. This bit is reset when the Status Register is read.
4	Break Interrupt	A logic "1" on this bit indicates that the Serial Input pin of the COM92C451 is held in the spacing state for longer than a full word transmission time (start + data + parity + stop bits). This bit, when set, will cause an interrupt if bit 2 of the Interrupt Enable Register is also set. In order for the ACE to restart after a break is received, the Serial Input pin of the COM92C451 must be a logic "1" for at least 1/2 bit time. The Break Interrupt bit is reset when the Status Register is read.
5	Transmitter Holding Register Empty	A logic "1" on this bit indicates that the ACE is ready to accept a new character for transmission because the previous character has been transferred from this register to the Shift Register. This bit, when set, will cause an interrupt if bit 1 of the Interrupt Enable Register is also set. This bit is reset when the microprocessor loads the Transmitter Holding Register.
6	Transmitter Empty	A logic "1" on this bit indicates that the Transmitter Holding Register and the Transmitter Shift Register are both empty. This bit is reset when either the Holding Register of the Shift Register contains a data character.
7		This undefined bit is permanently a logic "0".

Modem Control Register (MCR)

This 8-bit Read/Write register controls the ACE's interface to the modem. The Modem Control Register is cleared at power up by RESET.

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Table 8 - Modem Control Register

BIT	BIT NAME	DESCRIPTION
0	DTR	A logic "1" on this bit forces the $\overline{DTR}$ output to a logic "0". A logic "0" on this bit forces the $\overline{DTR}$ output to a logic "1".
1	RTS	A logic "1" on this bit forces the $\overline{RTS}$ output to a logic "0". A logic "0" on this bit forces tha $\overline{RTS}$ output to a logic "1".
2	BIT2	This bit is used in loopback mode only (as described in bit 4 definition). This bit is not brought out to a pin.
3	OUT2	A logic "1" on this bit forces the $\overline{OUT2}$ output to a logic "0". A logic "0" on this bit forces the $\overline{OUT2}$ output to a logic "1".
4	LOOPBACK	This bit provides the loopback feature for diagnostic testing of the ACE. In the diagnostic test mode, the data from the transmitter output is internally connected to t the receiver input in order to allow the processor to verify the transmit and receive data paths of the ACE. A logic "1" on this bit does the following: - Sets the Serial Output pin to the marking state. - Effectively disconnects the Serial Input signal. - "Loops back" the output of the Transmitter Shift Register into the input of the Receiver Shift Register . - Effectively disconnects the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$). - Internally connects the three Modem Control outputs ($\overline{RTS}$, $\overline{DTR}$, and $\overline{OUT2}$) and bit 2 to the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$, and $\overline{RI}$) respectively. The three Modem Control output pins are forced to their inactive state (logic "1"). Bit 2 is not brought out to a pin. In the diagnostic mode, the receiver and transmitter interrupts are fully operational and are still controlled by the Interrupt Enable Register. The Modem Control Interrupts are also operational but the sources of these interrupts are now the lower four bits of the Modem Control Register rather than the Modem Control inputs.
5-7		These undefined bits are permanently logic "0".

Modem Status Register (MSR)

This 8-bit Read-Only register provides the current state of the control lines from the modem and provide a Modem Status Interrupt whenever these states change. The Modem Status Register is cleared at power up by RESET.

Table 9 - Modem Status Register

BIT	BIT NAME	DESCRIPTION
0	Delta Clear To Send	A logic "1" on this bit indicates that the $\overline{CTS}$ input of the COM92C451 has changed state since the last time the Modem Status Register was read. This bit, when set, will cause an interrupt if bit 3 of the Interrupt Enable Register is also set. This bit is reset when the Modem Status Register is read.
1	Delta Data Set Ready	A logic "1" on this bit indicates that the $\overline{DSR}$ input of the COM92C451 has changed state since the last time the Modem Status Register was read. This bit, when set, will cause an interrupt if bit 3 of the Interrupt Enable Register is also set. This bit is reset when the Modem Status Register is read.
2	Trailing Edge of Ring Indicator	A logic "1" on this bit indicates that the $\overline{RI}$ input of the COM92C451 has changed from logic "0" to logic "1" since the last time the Modem Status Register was read. This bit, when set, will cause an interrupt if bit 3 of the Interrupt Enable Register is also set. This bit is reset when the Modem Status Register is read.
3	Delta Data Carrier Detect	A logic "1" on this bit indicates that the $\overline{DCD}$ input of the COM92C451 has changed state since the last time the Modem Status Register was read. This bit, when set, will cause an interrupt if bit 3 of the Interrupt Enable Register is also set. This bit is reset when the Modem Status Register is read.
4	CTS	This bit is the complement of the $\overline{CTS}$ input. If the device is in loopback mode (bit 4 of MCR is logic "1") then this bit is equivalent to bit 1 ($\overline{RTS}$) of the MCR.
5	DSR	This bit is the complement of the $\overline{DSR}$ input. If the device is in loopback mode (bit 4 of MCR is logic "1") then this bit is equivalent to bit 0 ($\overline{DTR}$) of the MCR.
6	RI	This bit is the complement of the $\overline{RI}$ input. If the device is in loopback mode (bit 4 of MCR is logic "1") then this bit is equivalent to bit 2 of the MCR, which does not come out to a pin.
7	DCD	This bit is the complement of the $\overline{DCD}$ input. If the device is in loopback mode (bit 4 of MCR is logic "1") then this bit is equivalent to bit 3 ($\overline{OUT 2}$) of the MCR.

Interrupt Identification Register (IIR)

In order to provide minimum software overhead during data character transfers, the ACE prioritizes interrupts into four levels as follows:

Priority 1 - Receiver Line Status
Priority 2 - Received Data Ready
Priority 3 - Transmitter Holding Register Empty
Priority 4 - Modem Status

The IIR is a Read-Only register which stores the information indicating that a prioritized interrupt is pending and the source of that interrupt. When the microprocessor accesses the IIR, the ACE freezes all interrupts and indicates the highest priority pending interrupt to the microprocessor. During the entire microprocessor access, the curent indication of the IIR does not change. Upon completion of the access, any interrupts that may have occured within the time that the access took place now updates the contents of the IIR. The Interrupt Identification Register is cleared at power up by the RESET.

Table 10 - Interrupt Identification Register

BIT	DESCRIPTION
0	A logic "0" on this bit indicates that an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. A logic "1" on this bit indicates that no interrupt is pending. This bit can be used in either a hardwired prioritized or in a polled environment to indicate whether an interrupt is pending.
1,2	These two bits are used to identify the highest priority interrupt pending as indicated in Table 11.
3-7	These undefined bits are permanently logic "0".

Interrupt Enable Register (IER)

This 8-bit Read/Write register allows the user to selectively enable the four interrupt sources of the ACE in order to activate the Interrupt Request 1 pin of the COM92C451. Disabling the entire interrupt system inhibits the Interrupt Identification Register and the Interrupt Request 1 output. All other system functions operate in their normal manner, including the Status and Modem Status Registers. The Interrupt Enable Register is cleared at power up by RESET.

Table 12 - Interrupt Enable Register

BIT	DESCRIPTION
0	A logic "1" on this bit enables the Received Data Available Interrupt.
1	A logic "1" on this bit enables the Transmitter Holding Register Empty Interrupt.
2	A logic "1" on this bit enables the Receiver Line Status Interrupt.
3	A logic "1" on this bit enables the Modem Status Interrupt.
4-7	These undefined bits are permanently logic "0".

Scratchpad Register

This 8-bit Read/Write register is intended for use as a scratchpad register for the programmer to hold temporary data. It has no effect on the operation of the COM92C451. The Scratchpad Register is cleared at power up by RESET.

Table 11 - Interrupt Priority

Bit 2	Bit 1	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
1	1	First	Receiver Line Status	Overrun Error, Parity Error, Framing Error, or Break Interrupt	Reading the Line Ststus Register or RESET
1	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register or RESET
0	1	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmitter Holding Register or RESET
0	0	Fourth	Modem Status	Clear to Send, Data Set Ready, Ring Indicator, or Received Line Signal Detect	Reading the Modem Status Register or RESET

OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive voltage on any pin, with respect to ground ..... V_{cc} +0.3V
Negative voltage on any pin, with respect to ground ..... -0.3V
Maximum V_{CC} ..... +7.0V

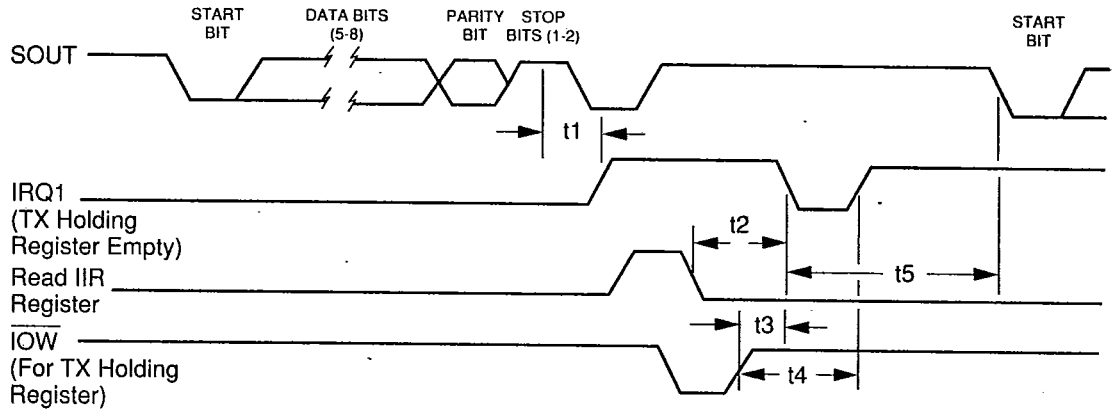
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

PRELIMINARY
Notice: This is not a final specification.
Some parametric limits are subject to change.

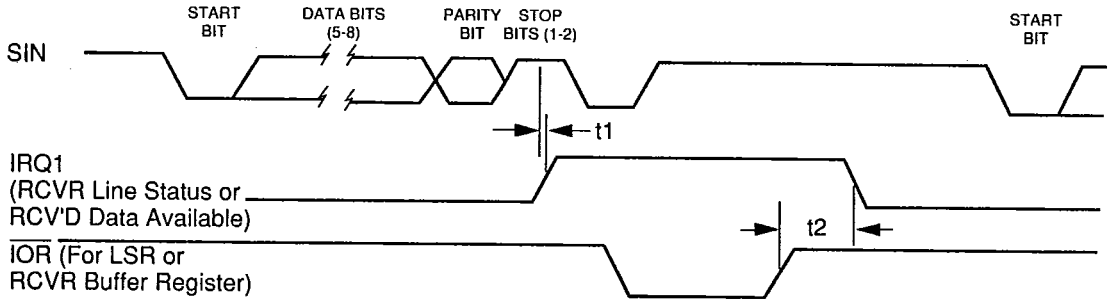
DC ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V+5%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	COMMENTS
Low Input Voltage	V_{IL}			0.8	V	
High Input Voltage	V_{IH}	2.0			V	
Input Leakage Current	I_{IZ}	-10.0		+10.0	µA	V_{IN} = 0 to V_{CC}
Low Output Voltage 1 (All outputs except data buses and printer control bus)	V_{OL1}			0.4	V	I_{SINK} = 4.0mA
High Output Voltage 1 (All outputs except data buses and printer control bus)	V_{OH1}	2.4			V	I_{SOURCE} = 4.0mA
Low Output Voltage 2 (CPU Data Bus)	V_{OL2}			0.4	V	I_{SINK} = 4.0mA
High Output Voltage 2 (CPU Data Bus)	V_{OH2}	2.4			V	I_{SOURCE} = 4.0mA
High Impedance Leakage	I_{OZ1}	-10.0		+10.0	µA	V_{IN} = 0 to V_{CC}
Low Output Voltage 3 (Printer Data Bus)	V_{OL3}			0.4	V	I_{SINK} = 24.0mA
High Output Voltage 3 (Printer Data Bus)	V_{OH3}	2.4			V	I_{SOURCE} = 3.0mA
Low Output Voltage 4 (Printer Control Bus; Open Drain Pins)	V_{OL4}			0.4	V	I_{SINK} = 24.0mA
High Impedance Leakage	I_{OZ2}	-10.0		+10.0	µA	V_{IN} = 0 to V_{CC}
V_{CC} Supply Current 1	I_{CC1}			20.0	mA	No output loads. All inputs at 0V or V_{CC}, at a Baud Rate of 4 MHz.
Input Capacitance	C_{IN}			0.5	pF	T_A = 25°C;
Output Capacitance	C_{OUT}			0.5	pF	f_C = 1MHz;
High Impedance Capacitance	C_Z			5.0	pF	V_{CC} = 0V



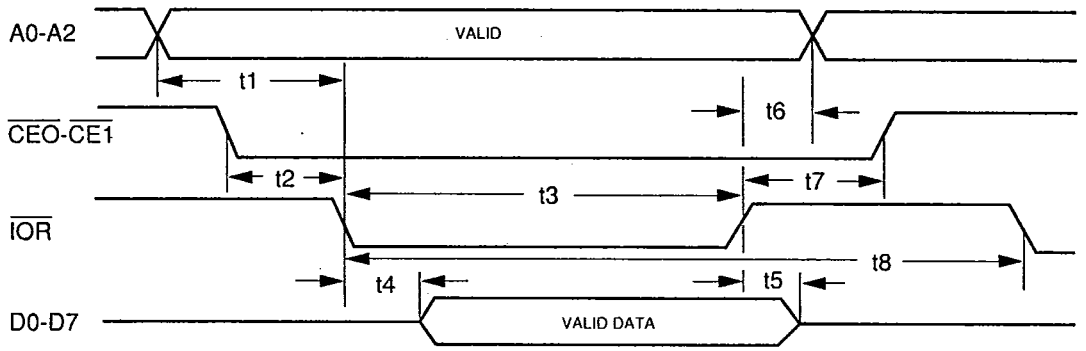
	Parameter	min	typ	max	units
t1	Stop Bit to Interrupt	8		8	Transmit Baud Clocks
t2	Read IIR to Reset Interrupt			150	nS
t3	Write TX Holding Register to Reset Interrupt			150	nS
t4	Initial Write to Interrupt	16		32	Transmit Baud Clocks
t5	Initial Interrupt Reset to TX Start	8		24	Transmit Baud Clocks

FIGURE 3 - TRANSMITTER TIMING



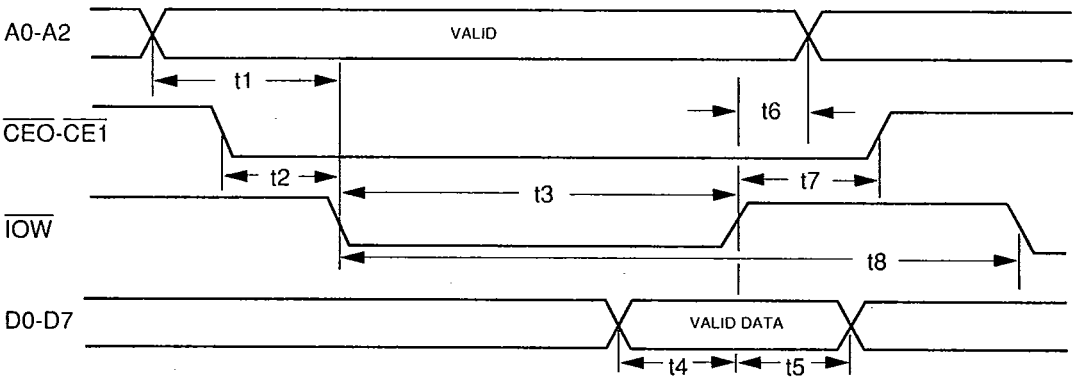
	Parameter	min	typ	max	units
t1	Stop Bit to Interrupt			1	Receive Baud Clocks
t2	Read LSR, RCVR Buffer Register to Reset Interrupt			150	nS

FIGURE 4 - RECEIVER TIMING



	Parameter	min	typ	max	units
t1	Address Set Up	30			nS
t2	Chip Enable Set Up	20			nS
t3	IOR Width	100			nS
t4	IOR to Data Valid			70	nS
t5	IOR to Floating Data	0		70	nS
t6	Address Hold	20			nS
t7	Chip Enable Hold	20			nS
t8	Read Cycle	140			nS

FIGURE 5 - READ CYCLE TIMING



	Parameter	min	typ	max	units
t1	Address Set Up	30			nS
t2	Chip Enable Set Up	20			nS
t3	IOW Width	100			nS
t4	Data Set Up Time	50			nS
t5	Data Hold Time	20			nS
t6	Address Hold Time	20			nS
t7	Chip Select Hold	20			nS
t8	Write Cycle	140			nS

FIGURE 6 - WRITE CYCLE TIMING

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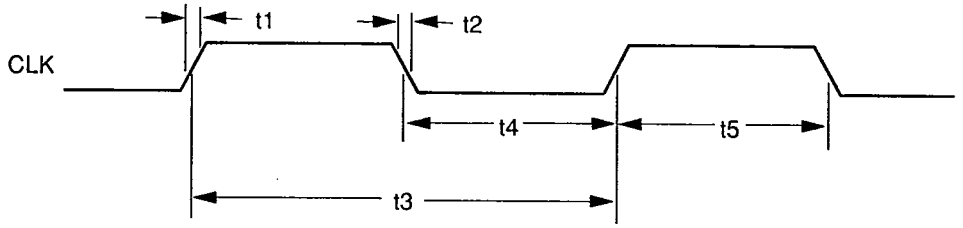
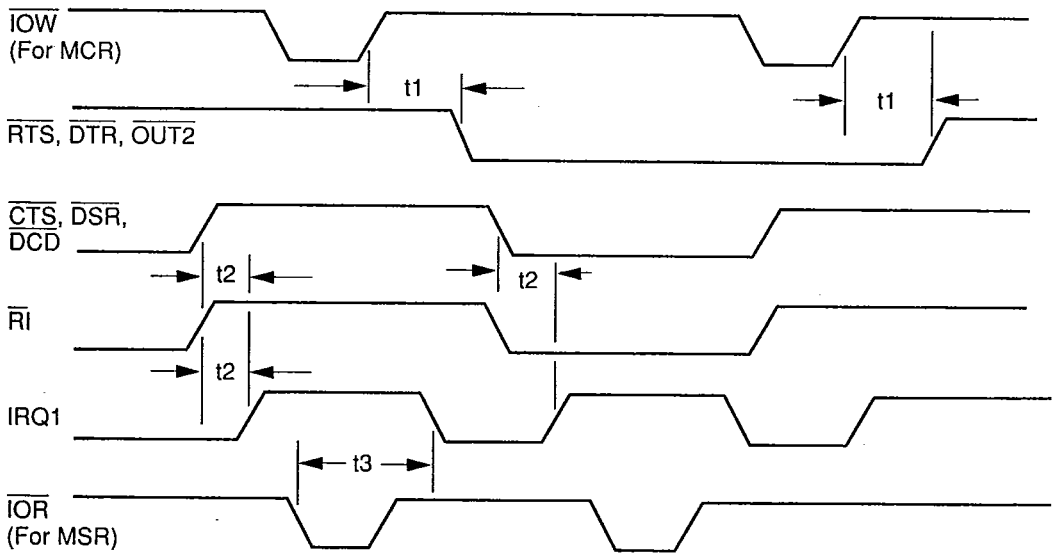


	Parameter	min	typ	max	units
t1	Clock Rise Time			5	nS
t2	Clock Fall Time			5	nS
t3	Clock Period	100			nS
t4	Clock Low Time	40			nS
t5	Clock High Time	60			nS

FIGURE 7 - CLOCK TIMING



	Parameter	min	typ	max	units
t1	Write MCR to MODEM Output Toggle			100	nS
t2	CTS, DSR, DCD, RI High or CTS, DSR DCD Low to IRQ1			100	nS
t3	Read MSR to Reset Interrupt			100	nS

FIGURE 8 - MODEM TIMING

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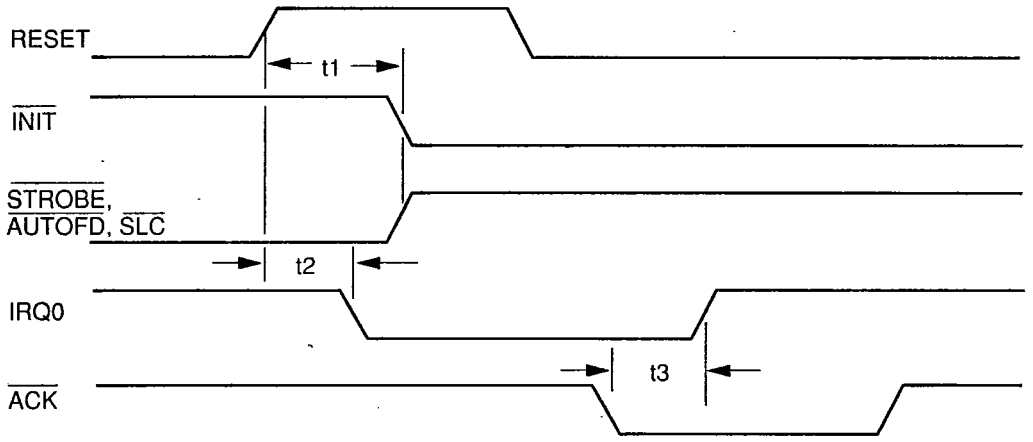

	Parameter	min	typ	max	units
t1	RESET to STROBE, AUTOFD, INIT, SLC			65	nS
t2	RESET to Interrupt Float			55	nS
t3	ACK to Interrupt			35	nS

FIGURE 9 - PRINTER TIMING

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 • FAX 516-231-6004