

Description

RClamp® TVS diodes are designed to protect sensitive electronics from damage or latch-up due to ESD, EFT and EOS events. This device offers desirable characteristics for board level protection including fast response time, low operating and clamping voltage.

RClamp3351ZA features extremely good ESD and EOS protection characteristics highlighted by low dynamic resistance and high surge capability. Data (I/O) lines are protected from EOS surge events as high as 10A ($t_p = 8/20\mu s$). It has low peak ESD clamping voltage, and high ESD withstand voltage ($\pm 22kV$ contact per IEC 61000-4-2). Each device will protect one data line operating up to ± 3.3 volts.

RClamp3351ZA is in a 2-pin SLP0603P2X3F package measuring 0.600×0.300 mm with a nominal height of only 0.250 mm. Leads are finished with NiAu. The small package gives the designer the flexibility to protect single lines in applications where arrays are not practical.

Features

- High ESD withstand voltage
 - ♦ $\pm 25kV$ (air), $\pm 22kV$ (contact) per IEC 61000-4-2
- High surge (EOS) capability : 10A ($t_p = 8/20\mu s$)
- Ultra-Low capacitance: 0.6 pF Max
- Working voltage: $\pm 3.3V$
- Low reverse leakage current: 50nA max at $V_R = 3.3V$
- Solid-state silicon-avalanche technology

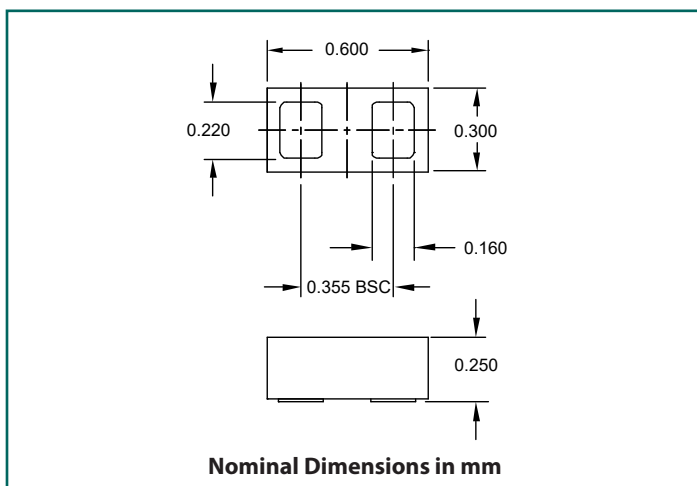
Mechanical Characteristics

- SLP0603P2X3F Package
- Pb-Free, Halogen Free, RoHS/WEEE Compliant
- Nominal Dimensions: $0.60 \times 0.30 \times 0.25$ mm
- Lead Finish: NiAu
- Marking : Marking Code
- Packaging : Tape and Reel

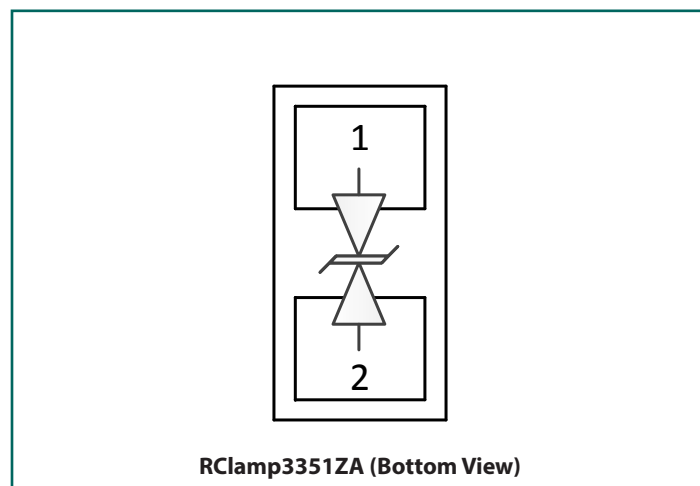
Applications

- SD card
- GbE
- USB 2.0
- LVDS

Nominal Dimensions



Schematic and Pin Configuration



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Peak Pulse Power (tp = 8/20μs)	P _{PK}	65	W
Peak Pulse Current (tp = 8/20μs)	I _{PP}	10	A
ESD per IEC 61000-4-2 (Air) ⁽¹⁾ ESD per IEC 61000-4-2 (Contact) ⁽¹⁾	V _{ESD}	±25 ±22	kV
Operating Temperature	T _J	-40 to +85	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Electrical Characteristics (T=25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Reverse Stand-Off Voltage	V _{RWM}	-40°C to 85°C, Pin 1 to 2 or 2 to 1				3.3	V
Reverse Breakdown Voltage	V _{BR}	I _{BR} = 1mA Pin 1 to 2 or 2 to 1	-40°C to 85°C	5.5	7.5	9	V
Reverse Leakage Current	I _R	V _{RWM} = 3.3V Pin 1 to 2 or 2 to 1	T = 25°C		<5	50	nA
Clamping Voltage ²	V _C	I _{pp} = 10A, tp = 1.2/50μs (Voltage), 8/20μs (Current) Combination Waveform, R _s = 2Ω				6.5	V
ESD Clamping Voltage ³	V _C	I _{pp} = 4A, tp = 0.2/100ns (TLP)			3.2		V
ESD Clamping Voltage ³	V _C	I _{pp} = 16A, tp = 0.2/100ns (TLP)			4.9		V
Dynamic Resistance ^{3, 4}	R _{DYN}	tp = 0.2/100ns (TLP)			0.15		Ohms
Junction Capacitance	C _J	V _R = 0V, f = 1MHz	T = 25°C		0.47	0.6	pF

Notes:

(1): ESD gun return path connected to Ground Reference Plane (GRP).

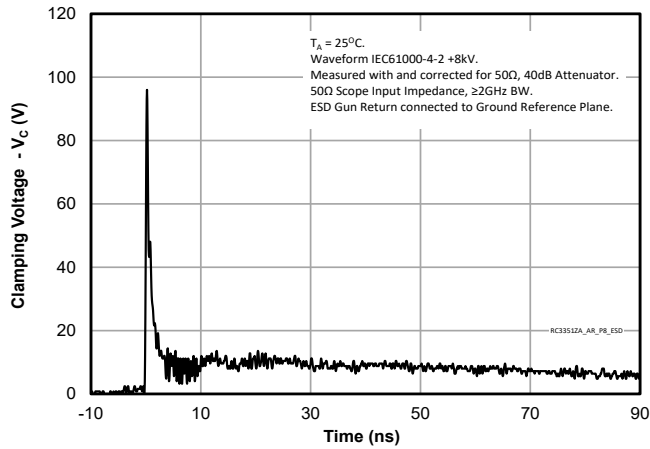
(2): Measured using a 1.2/50μs voltage, 8/20μs current combination waveform, R_S = 2 Ohms. Clamping is defined as the voltage across the device after the device snaps back to a conducting state.

(3): Transmission Line Pulse Test (TLP) Settings: tp = 100ns, tr = 0.2ns, I_{TLP} and V_{TLP} averaging window: t₁ = 70ns to t₂ = 90ns.

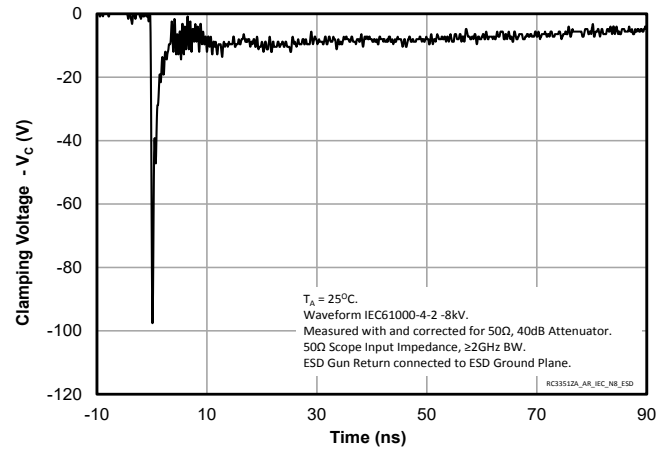
(4): Dynamic resistance calculated from I_{TLP} = 4A to I_{TLP} = 16A.

Typical Characteristics

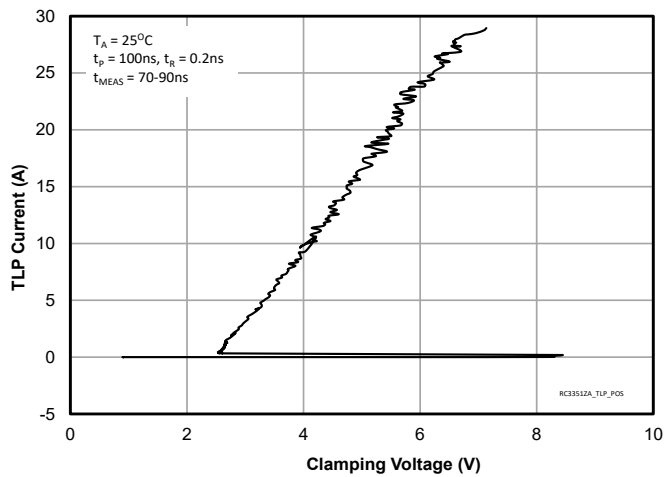
ESD Clamping (+8kV Contact per IEC 61000-4-2)



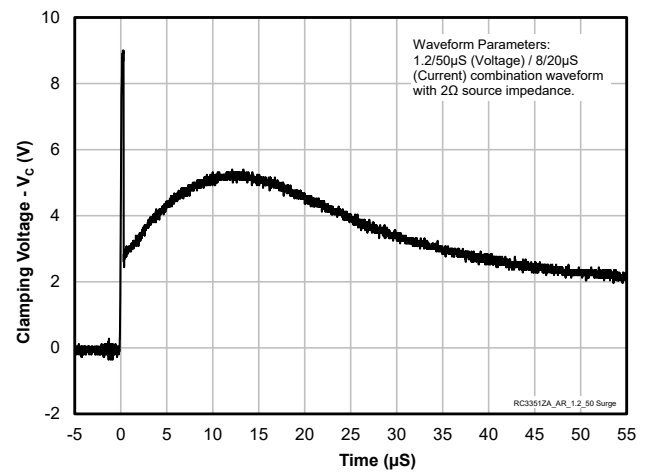
ESD Clamping (-8kV Contact per IEC 61000-4-2)



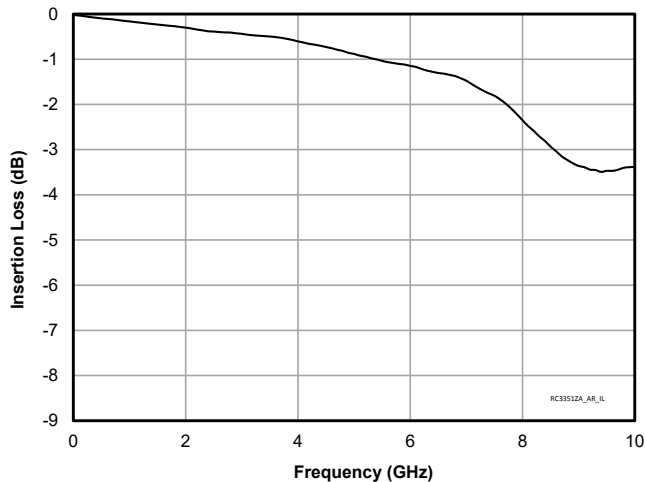
TLP IV Curve



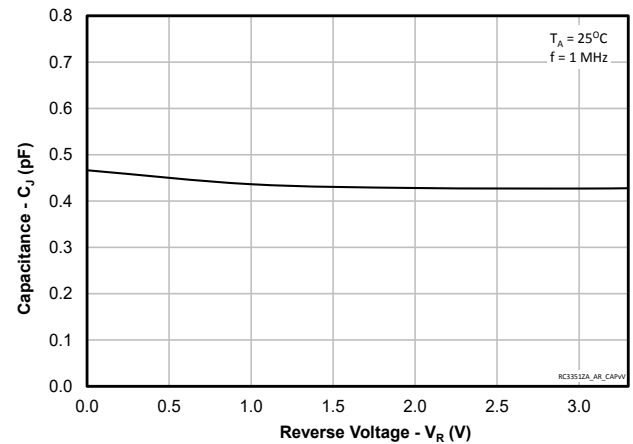
Clamping Characteristic (1.2/50μs Waveform, $V_{IN} = 27\text{V}$)



Insertion Loss (S21)



Capacitance vs. Reverse Voltage



Application Information

Assembly Guidelines

The small size of this device means that some care must be taken during the mounting process to insure reliable solder joints. The figure at the right details Semtech's recommended mounting pattern. Recommended assembly guidelines are shown in Table 1. Note that these are only recommendations and should serve only as a starting point for design since there are many factors that affect the assembly process. Exact manufacturing parameters will require some experimentation to get the desired solder application.

Solder Stencil

Stencil design is one of the key factors which will determine the volume of solder paste which is deposited onto the land pad. The area ratio of the stencil aperture will determine how well the stencil will print. The area ratio takes into account the aperture shape, aperture size, and stencil thickness. A minimum area ratio of 0.66 is preferred for the subject package. The area ratio of a rectangular aperture is given as:

Area Ratio = (L * W) / (2 * (L + W) * T)

Where:

- L = Aperture Length
- W = Aperture Width
- T = Stencil Thickness

Semtech recommends a stencil with square aperture and rounded corners for consistent solder release. The stencil should be laser cut with electropolished finish. A stencil thickness of 0.075mm (0.003") is recommended. A 0.100mm (0.004") stencil may be used, however the stencil opening may need to be increased slightly to achieve the desired area ratio to ensure proper solder coverage on the pad.

Recommended Mounting Pattern

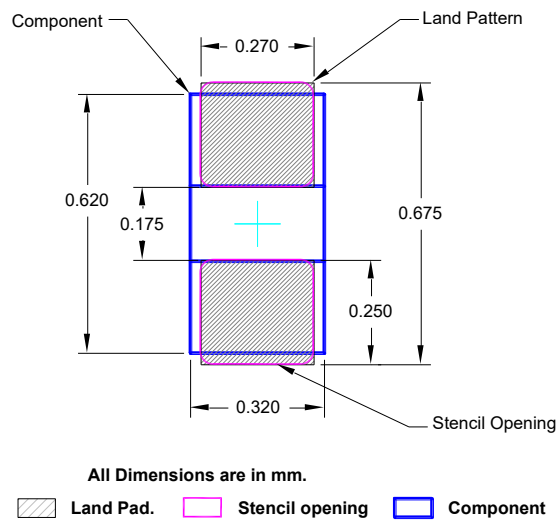
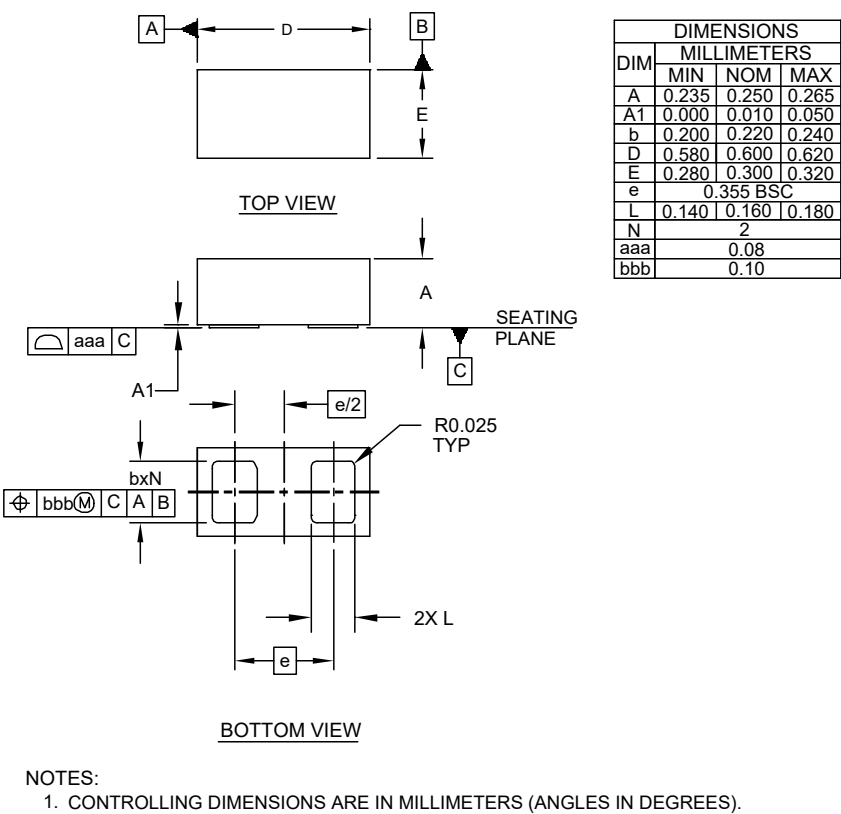


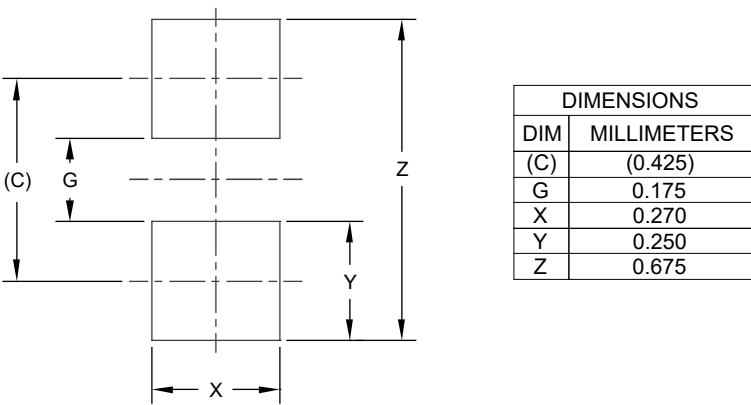
Table 1 - Assembly Guidelines

Assembly Parameter	Recommendation
Solder Stencil Design	Laser Cut, Electro-Polished
Aperture Shape	Rectangular with Rounded Corners
Solder Stencil Thickness	0.075mm (0.003") or 0.100mm (0.004")
Solder Paste Type	Type 4 Size Sphere or Smaller
Solder Reflow Profile	Per JEDEC J-STD-020
PCB Solder Pad Design	Solder Mask Defined
PCB Pad Finish	OSP or NiAu

Outline Drawing - SLP0603P2X3F



Land Pattern - SLP0603P2X3F



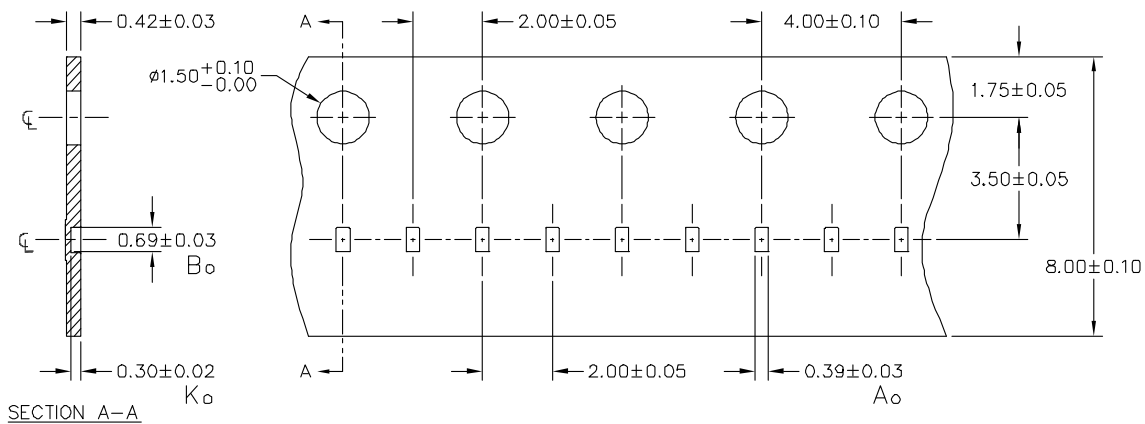
- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
 2. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Marking Code

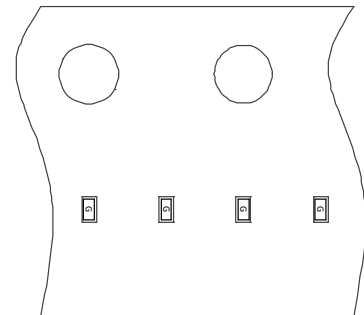
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Notes: Device is electrically symmetrical

Tape and Reel Specification



NOTES: ALL DIMENSIONS IN MILLIMETERS UNLESS OTHERWISE SPECIFIED.



Ordering Information

Part Number	Qty per Reel	Reel Size
RClamp3351ZATFT	15000	7 Inch
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