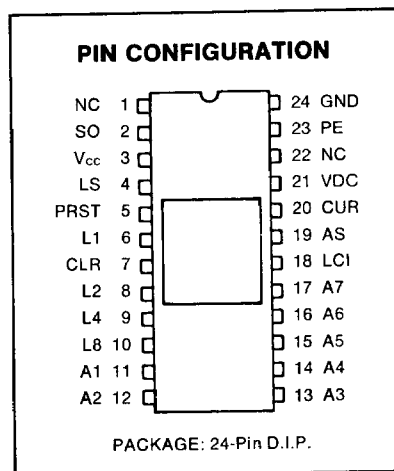


Dot Matrix Character Generator

128 Characters of 7 × 11 Bits

FEATURES

- ☐ On chip character generator (mask programmable)
 - 128 Characters
 - 7 x 11 Dot matrix block
- ☐ On chip video shift register
 - Maximum shift register frequency
 - CRT 7004A 20MHz
 - CRT 7004B 15MHz
 - CRT 7004C 10MHz
 - Access time 400ns
- ☐ No descender circuitry required
- ☐ On chip cursor
- ☐ On chip character address buffer
- ☐ On chip line address buffer
- ☐ Single +5 volt power supply
- ☐ TTL compatible
- ☐ MOS N-channel silicon-gate COPLAMOS® process
- ☐ CLASP® technology — ROM
- ☐ Compatible with CRT 5027 VTAC®
- ☐ Enhanced version of CG5004L-1



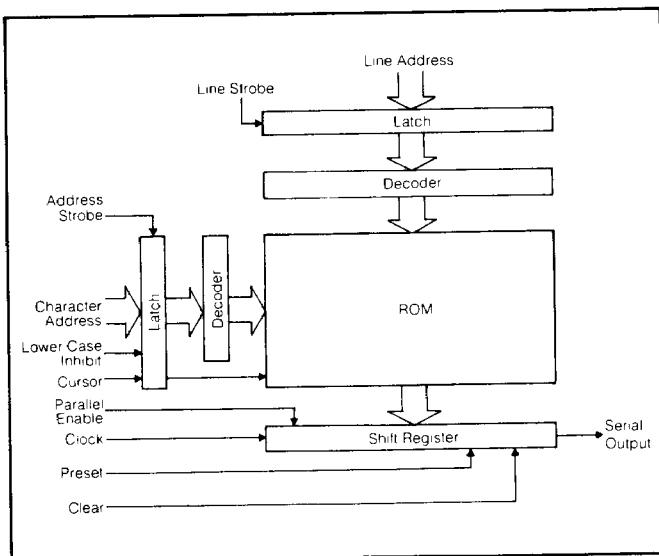
SECTION V

GENERAL DESCRIPTION

SMC's CRT 7004 is a high speed character generator with a high speed video shift register designed to display 128 characters in a 7 x 11 dot matrix. The CRT 7004 is an enhanced, pin for pin compatible, version of SMC's CG5004L-1. It is fabricated using SMC's patented COPLAMOS® and CLASP® technologies and employs depletion mode loads, allowing operation from a single +5v supply. This process permits reduction of turn-around time for ROM patterns.

The CRT 7004 is a companion chip to SMC's CRT 5027 VTAC®. Together these two chips comprise the circuitry required for the display portion of a CRT video terminal.

FUNCTIONAL BLOCK DIAGRAM



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	- 55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	-0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off.

In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A=0°C to 70°C, V_{CC}= - 5V ± 5%, unless otherwise noted)

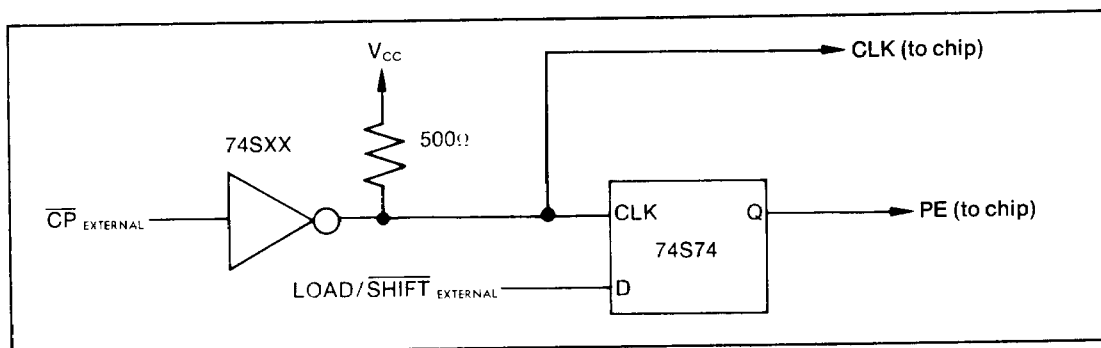
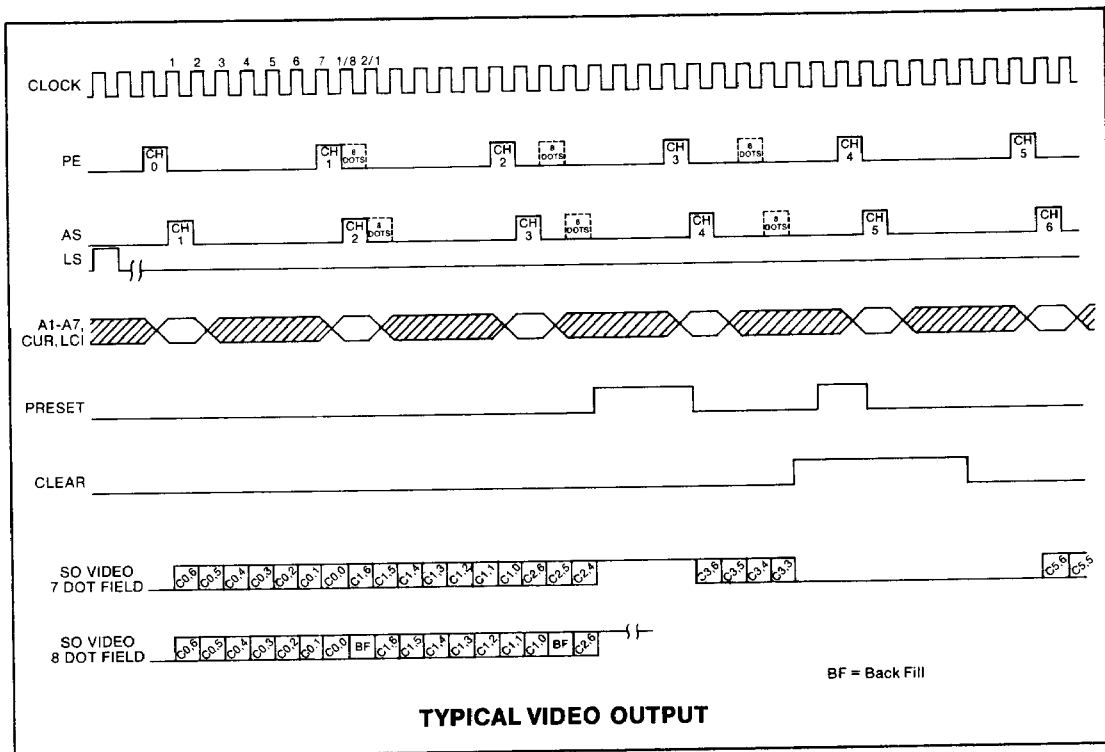
Parameter	Min.	Typ.	Max.	Unit	Comments
D.C. CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}	2.0		0.8	V	excluding VDC
High-level, V_{IH}				V	excluding VDC
INPUT VOLTAGE LEVELS-CLOCK					
Low-level, V_{IL}	4.3		0.8	V	See AC Timing Diagram
High-level, V_{IH}				V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}	2.4		0.4	V	$I_{OL} = 0.4 \text{ mA}$, 74LSXX load
High-level, V_{OH}				V	$I_{OH} = -20\mu\text{A}$
INPUT CURRENT					
Leakage, I_I			100	μA	$V_{IN} = 0, \text{LS, AS, A1-A7, Cursor LCI}$
			10	μA	$0 \leq V_{IN} \leq V_{CC}$, All others
INPUT CAPACITANCE					
Data		10		pF	@ 1 MHz
PE		20		pF	@ 1 MHz
CLOCK		25		pF	@ 1 MHz
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

SYMBOL	PARAMETER	CRT 7004A		CRT 7004B		CRT 7004C		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
VDC	Video Dot Clock Frequency	1.0	20	1.0	15	1.0	10	MHz
PW _H	VDC — High Time	13.5		21		36		ns
PW _L	VDC — Low Time	13.5		21		36		ns
t _{CYAS}	Address strobe to PE high	400		533		800		ns
t _{CYLS}	Line strobe to PE high	1.0		1.0		1.0		μs
t _r , t _f	Rise, fall time		10		10		10	ns
t _i	PE set-up time	5		20		20		ns
t ₂	PE hold time	15		15		15		ns
AS _{PW}	Address strobe pulse width	50		50		50		ns
LS _{PW}	Line strobe pulse width	50		50		50		ns
t _{SET-UP}	Input set-up time	≥ 0		≥ 0		≥ 0		ns
t _{HOLD}	Input hold time	15		15		15		ns
t _{Pd1} , t _{Pd0}	Output propagation delay		45		60		90	ns

ANNOUNCES

ANNOUNCES





NOTE

The differences between the CRT 7004 and CG5004L-1 are detailed below:

CG5004L-1

1. If both the Preset and Clear inputs are brought high simultaneously the Serial Output is disabled and may be wire-ORed.
2. All Inputs $V_{IH} = V_{CC} - 1.5v$
3. SO $V_{OL} = 0.4v @ I_{OL} = 0.2mA$
4. Shift Register is static
5. Clear—directly forces the output low; when released, the output is determined by the state of the shift register output.
6. General Timing Differences—See Timing Diagram

CRT 7004

1. Clear overrides Preset, no output disable is possible.
2. All inputs (except CLK) $V_{IH} = 2.0v, min.$
CLK $V_{IH} = 4.3v, min.$
3. SO $V_{OL} = 0.4v @ I_{OL} = 0.4mA$ 74LSXX load
4. Shift Register is dynamic
5. Clear directly forces the output low and will be latched (for a character time) by PE.
6. General Timing Differences—See Timing Diagram

Dot Matrix Character Generator

A3..A0		0000		0001		0010		0011		0100		0101		0110		0111		1000		1001		1010		1011		1100		1101		1110		1111	
		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0		C6...C0	
000	R1																																
	R11																																
001	R1																																
	R11																																
010	R1																																
	R11																																
011	R1																																
	R11																																
100	R1																																
	R11																																
101	R1																																
	R11																																
110	R1																																
	R11																																
111	R1																																
	R11																																

The Cursor for the CRT 7004-003 is presented as a double underscore on Rows 8 and 9.