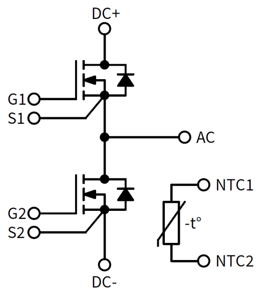
CAB011M12FM3, CAB011M12FM3T

1200 V, 11 mΩ, Silicon Carbide, Half-Bridge Module

V_{DS}	**1200 V**
$R_{DS(on)}$	**11 mΩ**

Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation
- Optional Pre-Applied Thermal Interface Material



Applications

- DC-DC Converters
- EV Chargers
- High-Efficiency Converters / Inverters
- Renewable Energy
- Smart-Grid / Grid-Tied Distributed Generation

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Maximum Parameters (Verified by Design)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V		
Gate-Source Voltage, Maximum Value	$V_{GS\,max}$	-8		+19		Transient, < 100 ns	Fig. 33
Gate-Source Voltage, Recommended	$V_{GS\,op}$	-4		+15		Static	
DC Continuous Drain Current ($T_{VJ} \le 150$ °C)	I_D		117		A	V_{GS} = 15 V, T_{HS} = 50 °C, $T_{VJ} \le 150$ °C	Fig. 20
DC Continuous Drain Current ($T_{VJ} \le 175$ °C)				120		V_{GS} = 15 V, T_{HS} = 50 °C, $T_{VJ} \le 175$ °C	
DC Source-Drain Current (Body Diode)	$I_{SD\,BD}$		69			V_{GS} = -4 V, T_{HS} = 50 °C, $T_{VJ} \le 175$ °C	
Pulsed Drain Current	$I_{D\,(pulsed)}$			240		t_{Pmax} limited by T_{VJmax} V_{GS} = 15 V, T_{HS} = 50 °C	
Virtual Junction Temperature	$T_{VJ\,op}$	-40		150	°C	Operation	
		-40		175		Intermittent with Reduced Life	

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MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_D = 35 mA	
			2.0		V	V_{DS} = V_{GS}, I_D = 35 mA, T_{VJ} = 150 °C	
Zero Gate Voltage Drain Current	I_{DSS}		2	50	μA	V_{GS} = 0 V, V_{DS} = 1200 V	
Gate-Source Leakage Current	I_{GSS}		0.02	0.5	μA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		10.5	14.0	mΩ	V_{GS} = 15 V, I_D = 100 A	Fig. 2 Fig. 3
			16.3		mΩ	V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 150 °C	
			19.0		mΩ	V_{GS} = 15 V, I_D = 100 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		73		S	V_{DS} = 20 V, I_D = 100 A	Fig. 4
			69		S	V_{DS} = 20 V, I_D = 100 A, T_{VJ} = 150 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{On}		1.28 1.34 1.43		mJ	V_{DD} = 600 V, I_D = 100 A, V_{GS} = -4 V/15 V, $R_{G(OFF)}$ = 1.0 Ω, $R_{G(ON)}$ = 1.0 Ω, L = 13.6 μH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{Off}		0.71 0.70 0.71		mJ		
Internal Gate Resistance	$R_{G(int)}$		3.2		Ω	f = 100 kHz, V_{AC} = 25 mV	
Input Capacitance	C_{iss}		10.3		nF	V_{GS} = 0 V, V_{DS} = 800 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		0.39		nF		
Reverse Transfer Capacitance	C_{rss}		30		pF		
Gate to Source Charge	Q_{GS}		49		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V, I_D = 100 A, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		100		nC		
Total Gate Charge	Q_G		324		nC		
FET Thermal Resistance, Junction to Heatsink	$R_{th\ JHS}$		0.428		°C/W	Measured with Pre-Applied TIM	Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Body Diode Forward Voltage	V_{SD}		5.1		V	V_{GS} = -4 V, I_{SD} = 100 A	Fig. 7
			4.7		V	V_{GS} = -4 V, I_{SD} = 100 A, T_{VJ} = 150 °C	
Reverse Recovery Time	t_{RR}		20.5		ns	V_{GS} = -4 V, I_{SD} = 100 A, V_R = 600 V, di/dt = 13.5 A/ns, T_{VJ} = 150 °C	Fig. 32
Reverse Recovery Charge	Q_{RR}		1.85		μC		
Peak Reverse Recovery Current	I_{RRM}		144		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{RR}		0.16 0.48 0.64		mJ	V_{DD} = 600 V, I_D = 100 A, V_{GS} = -4 V/15 V, $R_{G(ON)}$ = 1.0 Ω, L = 13.6 μH	Fig. 14

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	R_{HS}		2.23		mΩ	T_C = 125°C, I_D = 100 A, Note 1
Package Resistance, M2 (Low-Side)	R_{LS}		2.06		mΩ	T_C = 125°C, I_D = 100 A, Note 1
Stray Inductance	L_{Stray}		11.4		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Mounting Torque	M_S		2.0	2.3	N-m	M4 bolts
Weight	W		21		g	
Case Isolation Voltage	V_{isol}	3			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	200				
Clearance Distance			5.0		mm	Terminal to Terminal
			10.0		mm	Terminal to Heatsink
Creepage Distance			6.3		mm	Terminal to Terminal
			11.5		mm	Terminal to Heatsink

Notes:
[1] Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

NTC Thermistor Characterization

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rated Resistance	R_{NTC}		5.0		kΩ	T_{NTC} = 25°C
Resistance Tolerance at 25 °C	ΔR/R	-5		5	%	
Beta Value (T_2 = 50 °C)	$\beta_{25/50}$		3380		K	
Beta Value (T_2 = 80 °C)	$\beta_{25/80}$		3468		K	
Beta Value (T_2 = 100 °C)	$\beta_{25/100}$		3523		K	
Power Dissipation	P_{Max}			10	mW	T_{NTC} = 25°C

Typical Performance

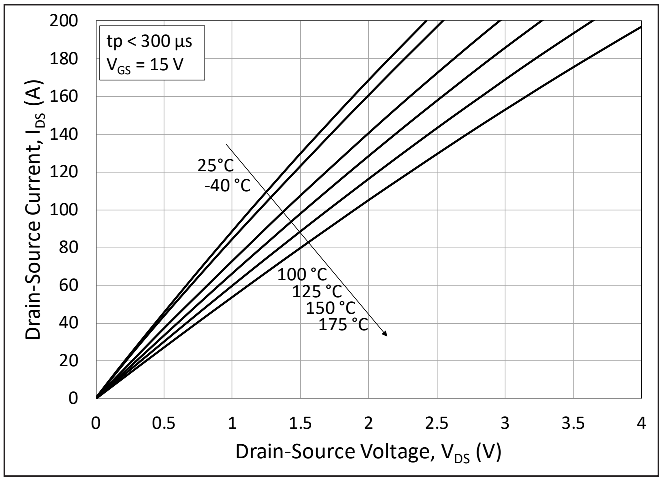


Figure 1. Output Characteristics for Various Junction Temperatures

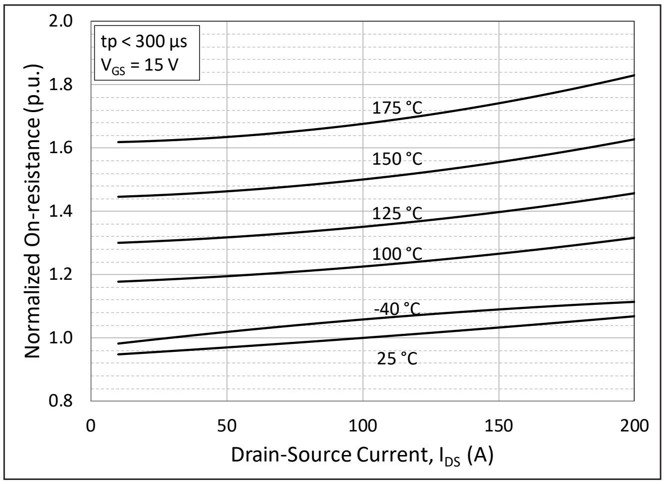


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

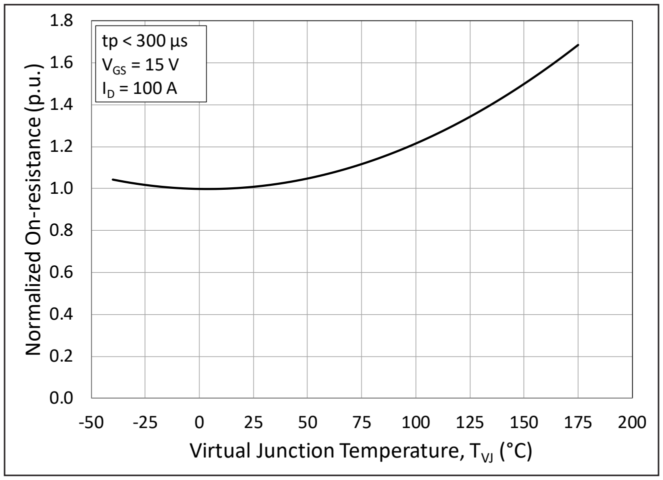


Figure 3. Normalized On-State Resistance vs. Junction Temperature

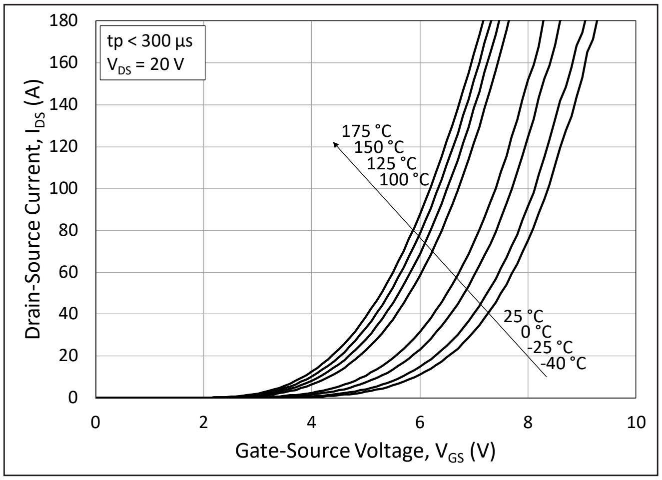


Figure 4. Transfer Characteristic for Various Junction Temperatures

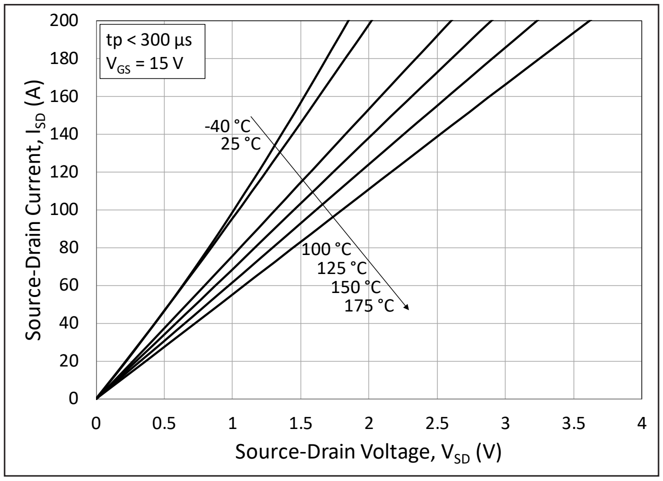


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

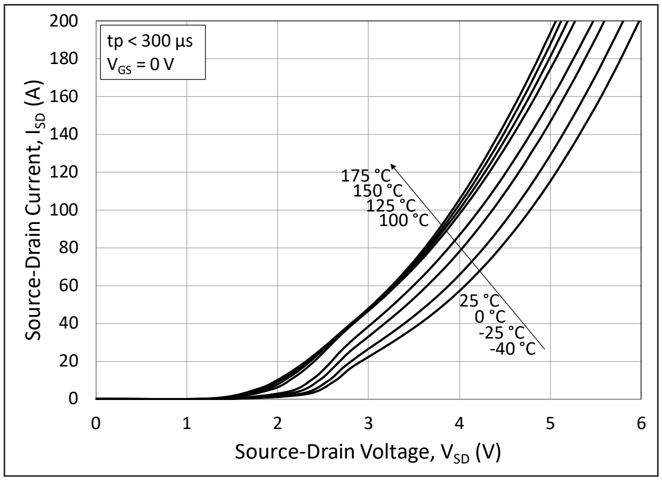


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V

Typical Performance

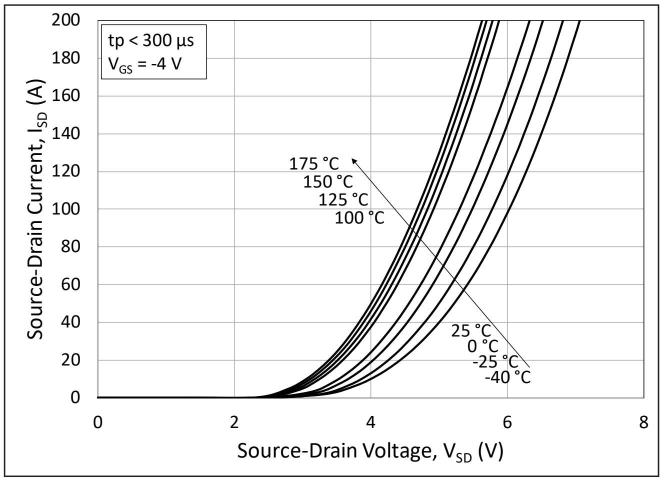


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -4 V (Body Diode)

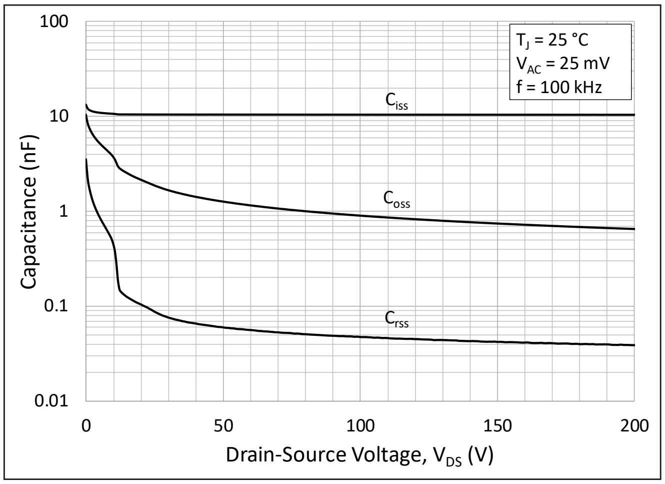


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

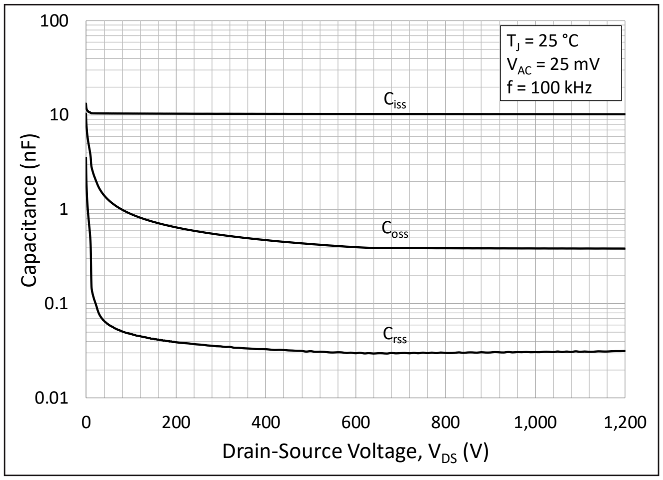


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)

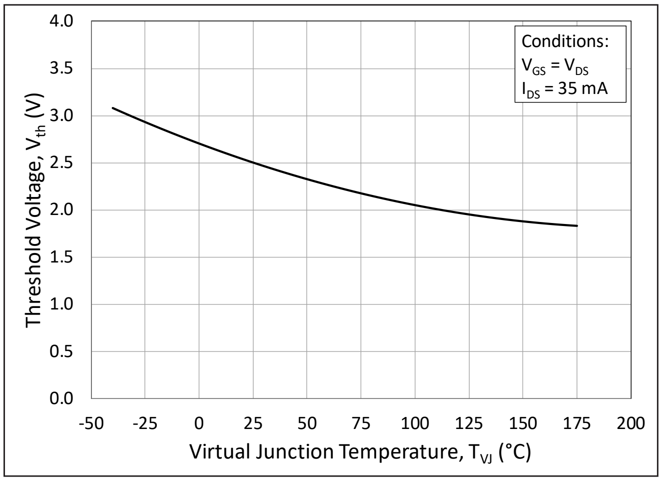


Figure 10. Threshold Voltage vs. Junction Temperature

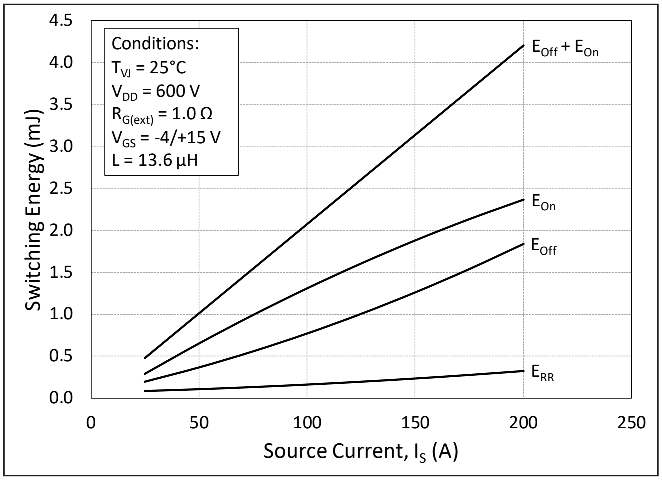


Figure 11. Switching Energy vs. Drain Current (V_{DD} = 600 V)

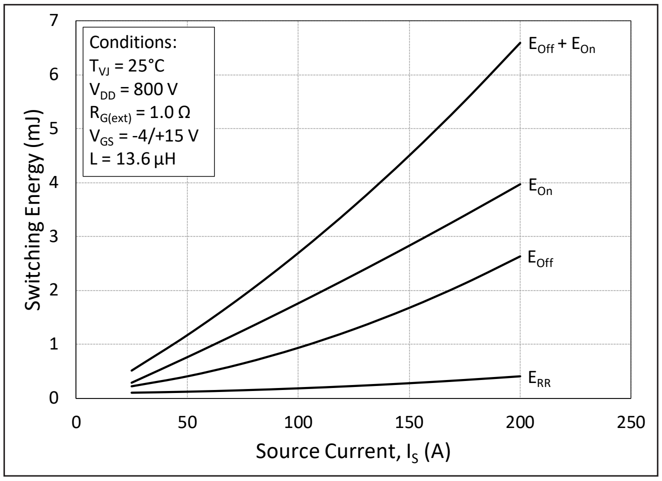


Figure 12. Switching Energy vs. Drain Current (V_{DD} = 800 V)

Typical Performance

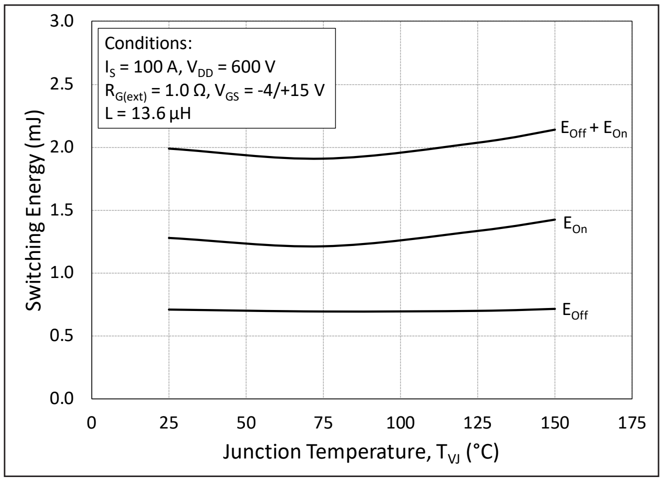


Figure 13. MOSFET Switching Energy vs. Junction Temperature

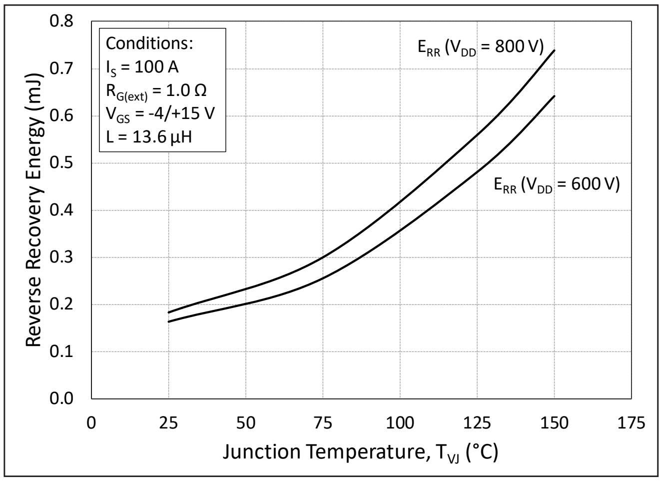


Figure 14. Reverse Recovery Energy vs. Junction Temperature

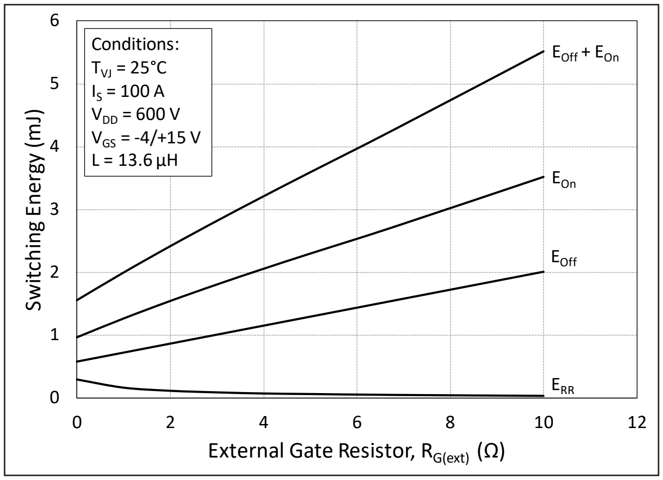


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

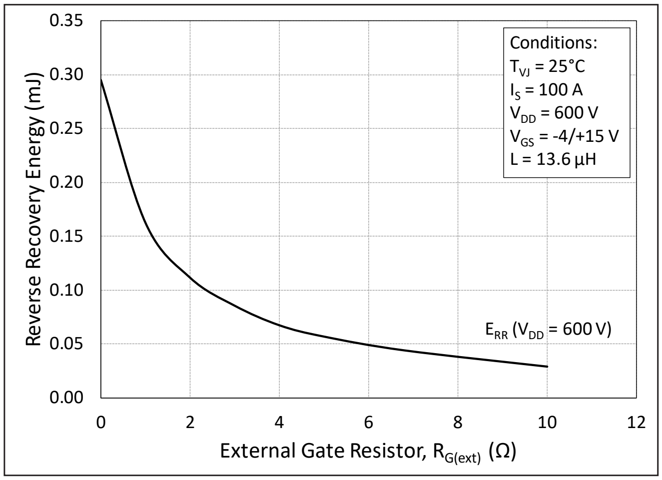


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

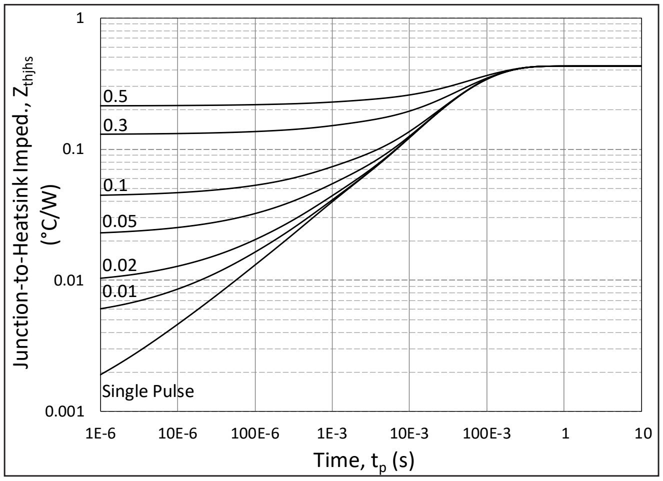


Figure 17. MOSFET Junction to Heatsink Transient Thermal Impedance, $Z_{th\ JHS}$ (°C/W)

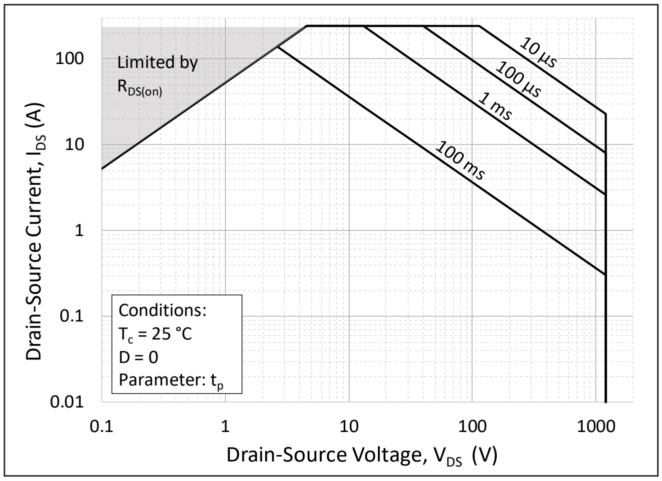


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

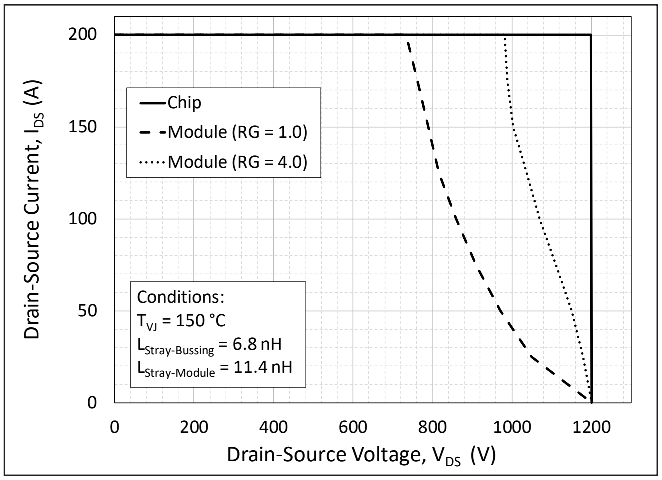


Figure 19. Switching Safe Operating Area

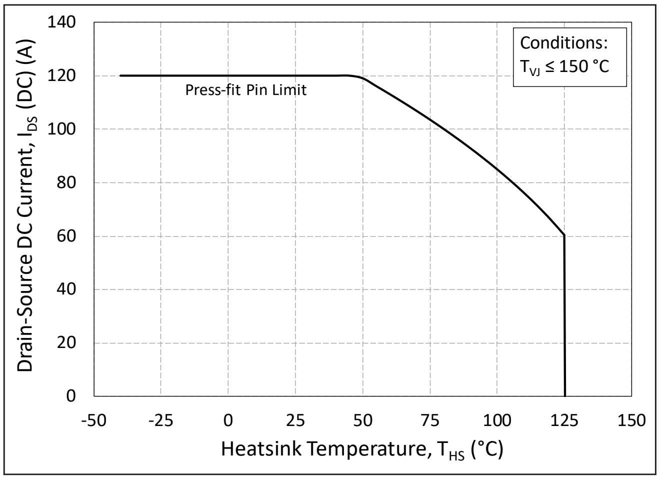


Figure 20. Continuous Drain Current Derating vs. Heatsink Temperature

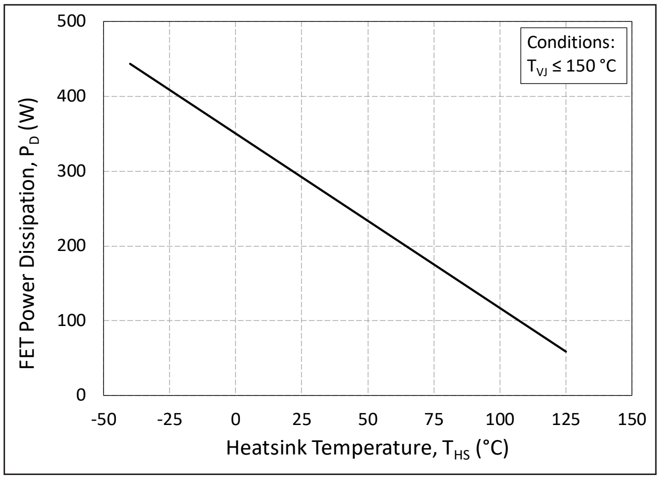


Figure 21. Maximum Power Dissipation Derating vs. Heatsink Temperature

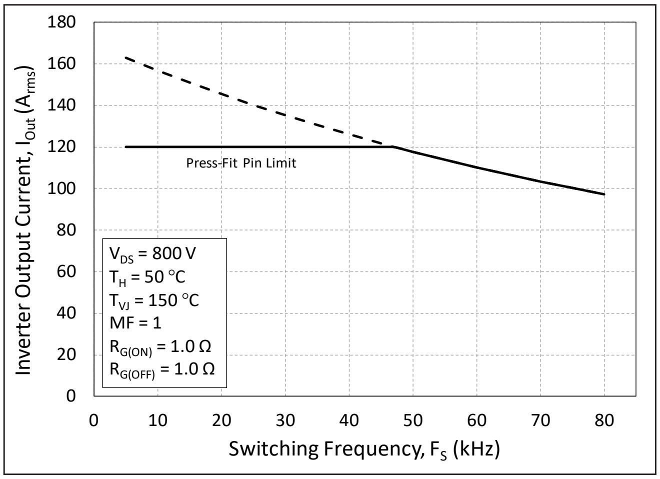


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

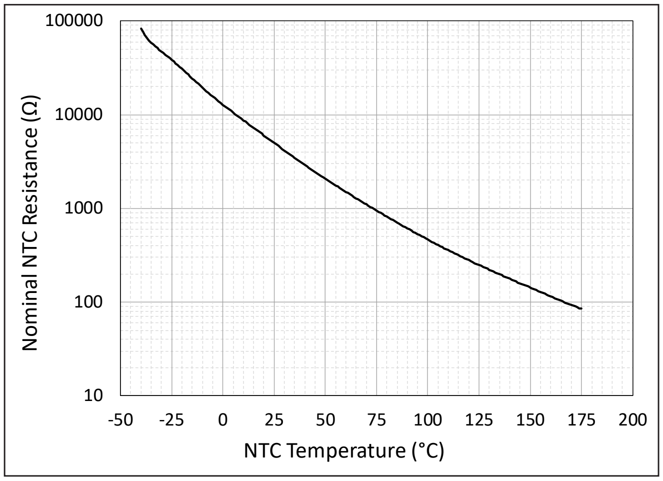


Figure 23. Nominal NTC Resistance vs. NTC Temperature

Timing Characteristics

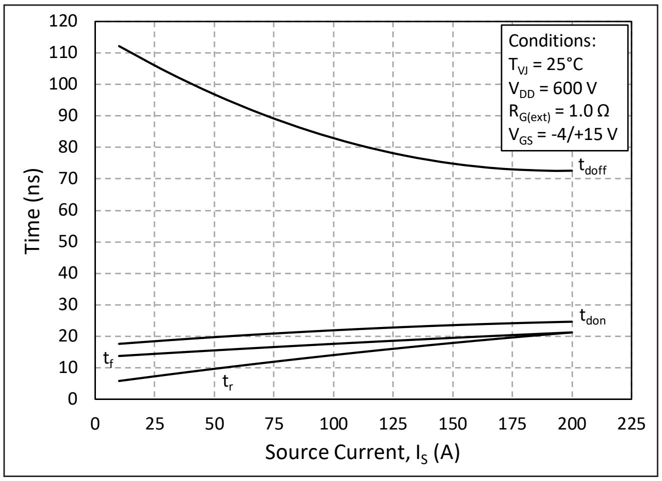


Figure 24. Timing vs. Source Current

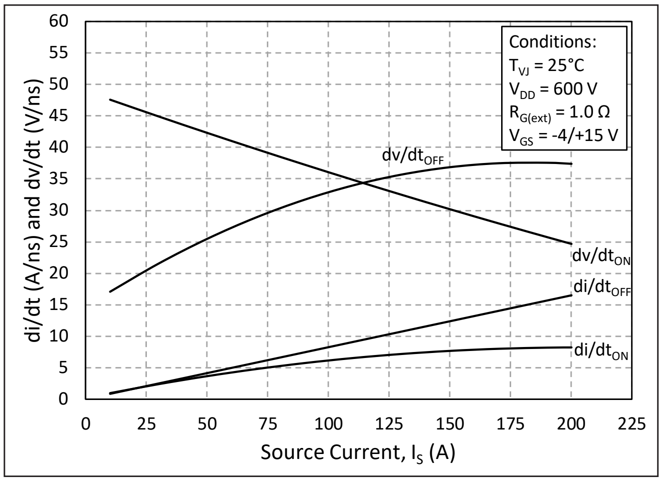


Figure 25. dv/dt and di/dt vs. Source Current

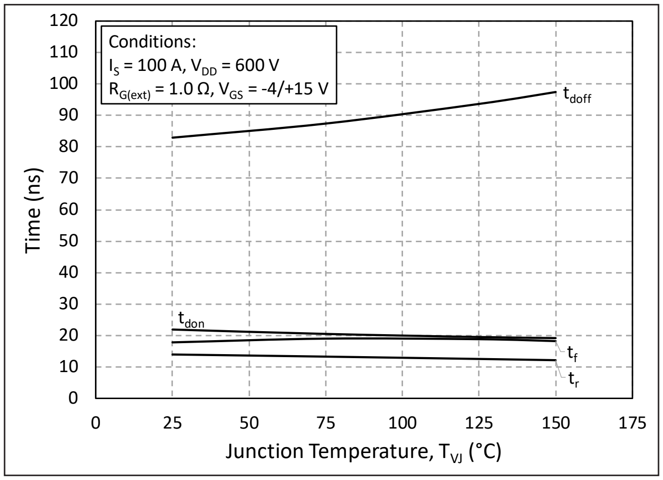


Figure 26. Timing vs. Junction Temperature

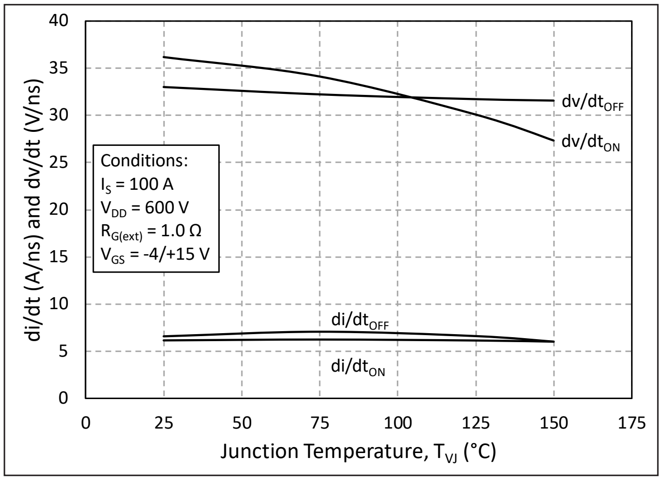


Figure 27. dv/dt and di/dt vs. Junction Temperature

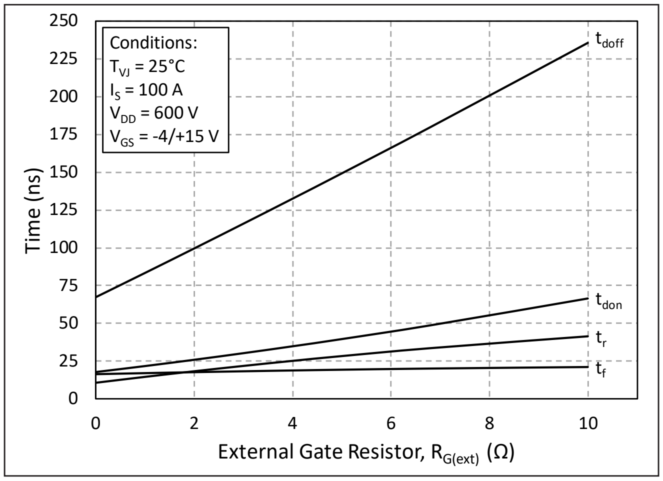


Figure 28. Timing vs. External Gate Resistance

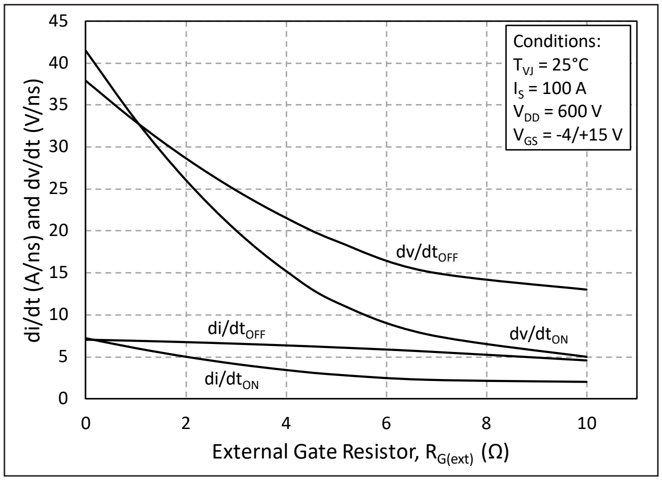


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

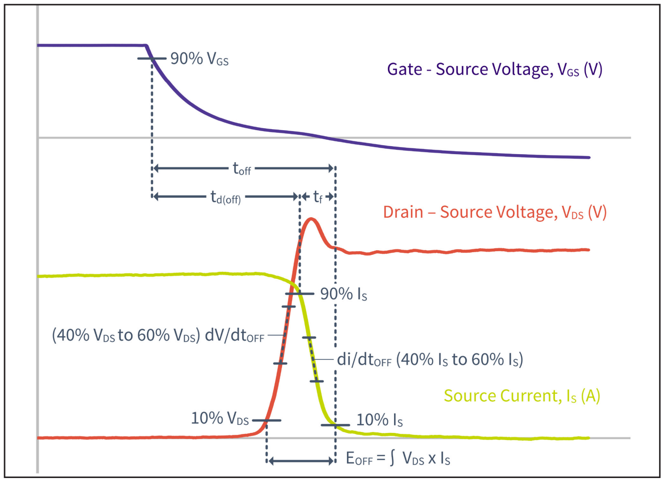


Figure 30. Turn-off Transient Definitions

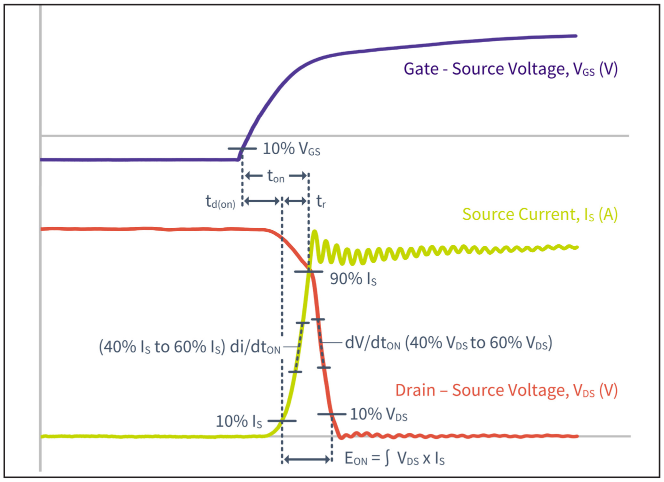


Figure 31. Turn-on Transient Definitions

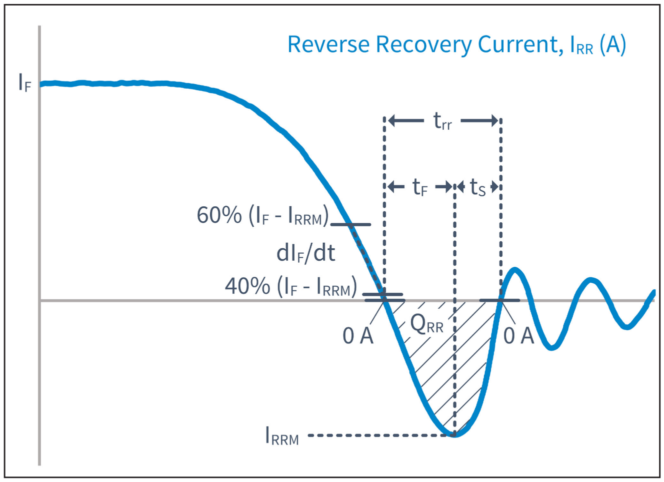


Figure 32. Reverse Recovery Definitions

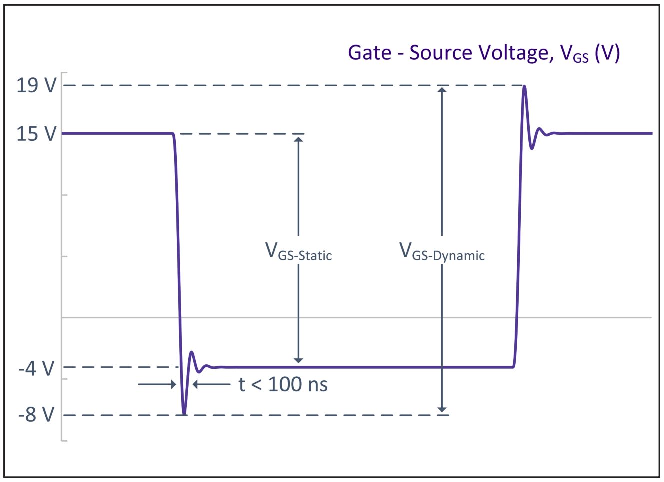
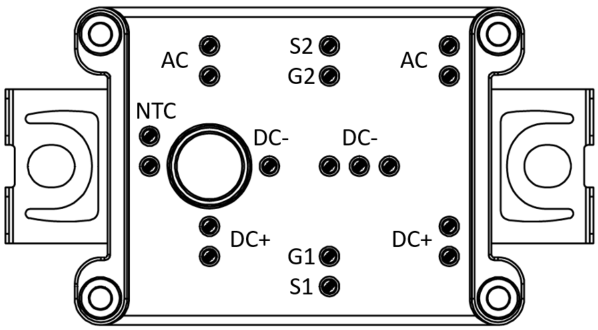
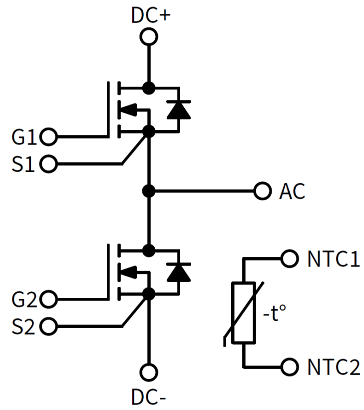


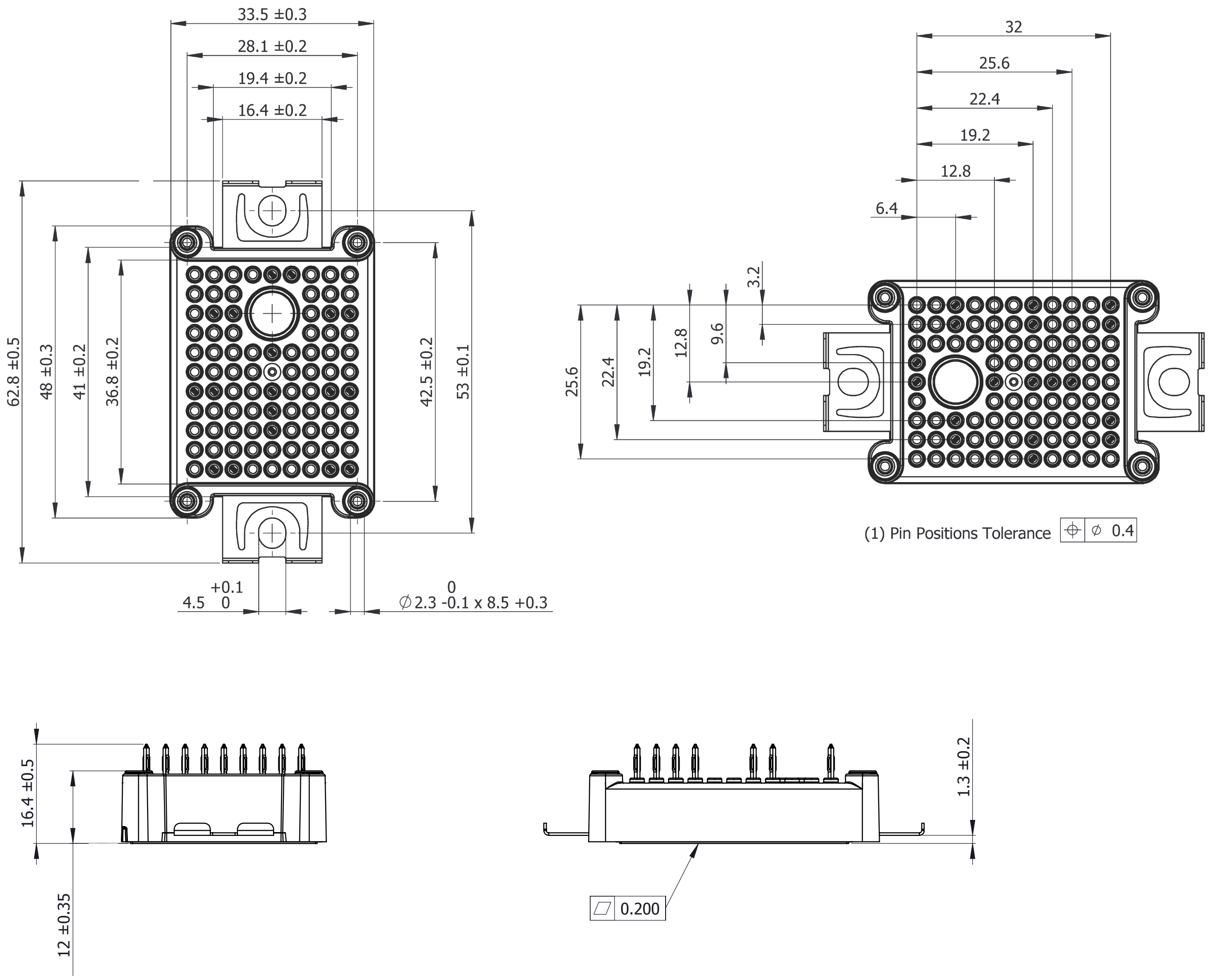
Figure 33. V_{GS} Transient Definitions

Pinout





Package Dimension (mm)



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Product Ordering Code

Part Number	Description
CAB011M12FM3	Without Pre-Applied Phase Change Thermal Interface Material
CAB011M12FM3T	With Pre-Applied Phase Change Thermal Interface Material

Supporting Links & Tools

Evaluation Tools & Support

- All LTSpice Models
- All PLECS Models
- KIT-CRD-CIL12N-FMA: Dynamic Evaluation Board for Half-Bridge FM3 Modules
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Dual-Channel Gate Driver Board

- EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board
- Si823H-AxWA-KIT: Skyworks® Gate Driver Board
- ACPL-355JC: Broadcom® Gate Driver Board
- CGD1700HB2M-UNA: Wolfspeed Gate Driver Board
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- CPWR-AN41: Mounting Instructions and PCB Requirements
- CPWR-AN42: Thermal Interface Material Application Note
- CPWR-AN45: Dynamic Performance Application Note

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REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

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