STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd., Hauppauge, N.Y. 11788
(516) 273-3100 • FAX: 516-231-6004

MSD95C00

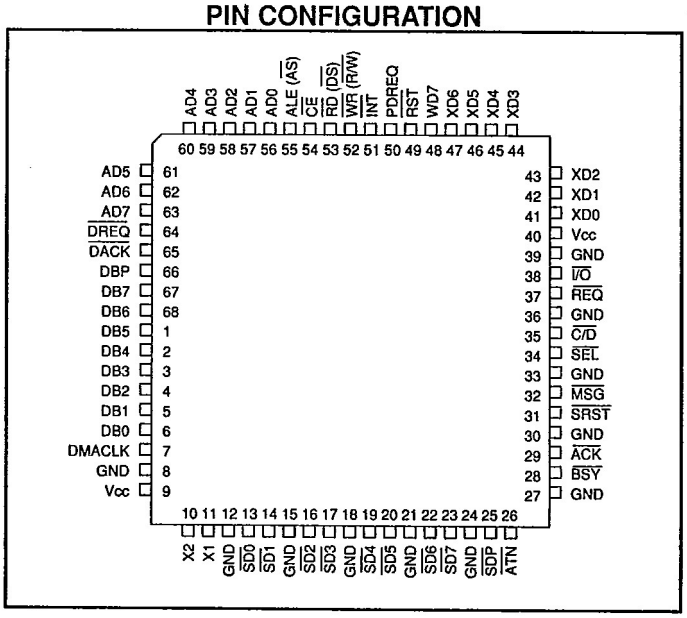
T-52-33-27

Small Computer System Interface (SCSI) Controller-SCSIC

FEATURES

- Initiator and Target Operation
- 5 MByte/Sec Synchronous and 3 MByte/Sec Asynchronous Data Transfers
- Automatic Arbitration and (Re) Selection
- Supports both Arbitration and Non-Arbitration/Applications
- Internal Twelve Byte Buffer
- Internal 24-bit Byte Transfer Counter
- Built-in 48 mA High-current SCSI Bus Drivers
- User Selectable Selection Timeout
- Separate Busses for Data and Microprocessor
- Separate DMA for Processor and Data Channels
- Burst Mode DMA Transfers on Data Bus
- Programmed I/O or DMA Transfers on Processor Data Bus
- Eight Bit Bi-Directional General Purpose I/O Port
- Bus Architecture allows caching
- Compatible with MSD95C02 and MSD95C01 Storage Controllers
- Low Power CMOS
- TTL compatible inputs and outputs

PIN CONFIGURATION



SCSI OVERVIEW

Up to 8 SCSI devices, known as Initiators and Targets, may be connected to a single SCSI bus. These SCSI devices communicate across the SCSI bus using a protocol based on ten distinct bus phases. Target devices execute high level commands which they receive from Initiator devices.

A SCSI device may have up to 256 Logical Units associated with it. Host adapters, disk drives and printers are examples of Logical Units. Any SCSI device may be connected to a SCSI port. This allows the user to connect any SCSI compatible device to any SCSI bus providing that the operating system is able to associate the type of device connected with its SCSI ID and Logical Unit Number.

The SCSI bus phases are Bus Free, Arbitration, Selection, Reselection, Command, Data In, Data Out, Message In, Message Out and Status. A target is capable of generating an Arbitration, Reselection, Command, Data In, Data Out, Message In, Message Out or Status phase. An initiator is capable of generating an Arbitration or Selection phase. When the SCSI devices are not generating any of the above phases, the system is said to be in the Bus Free phase. Note that the Arbitration phase may be generated by either a target or an initiator. For a complete description of the SCSI protocol, refer to the ANSI X3.131 specification.

GENERAL DESCRIPTION

The MSD95C00 SCSI Controller is capable of arbitrating for and supporting data transfer on an ANSI SCSI (Small Computer System Interface) compatible computer bus. The internal twelve byte buffer makes this device suitable for both peripheral and host adapter applications in systems that support both Asynchronous and Synchronous data transfer modes.

The MSD95C00 includes circuitry that automatically arbitrates for the SCSI bus and selects or reselects another device. This feature combined with the size of the internal buffer allows a selected Target device to transfer an entire command from an Initiator with a minimum of processor intervention on either side.

The MSD95C00 has three independent busses: one connects to the local microprocessor (the System bus), a second which connects to the data Ring buffer (the Data bus) and a third which connects to the SCSI bus. Information transfers may be made between the SCSI bus and either of the other two buses. The Data bus supports burst mode DMA transfers and the System Bus supports both programmed I/O and DMA transfers.

Accesses to the Ring buffer are controlled via a DMA request/acknowledge handshake. Local processor transfers, as well as transfers to logical units (e.g. media transfers), are asynchronous with respect to transfers across the SCSI bus.

The MSD95C00 can be combined with the flexible MSD95C02 or MSD95C01 Storage Controllers, a standard microprocessor, and static RAM to support embedded SCSI peripheral applications with minimum component count and synchronous SCSI speeds of up to 5 megabytes per second.

T-52-33-27

TABLE OF CONTENTS

DESCRIPTION OF PIN FUNCTIONS

T-52-33-27

SCSI INTERFACE NOTE: These Signals are Active Low.				
PIN NO.	**NAME**	**SYMBOL**	**I/O**	**DESCRIPTION**
13,14,16, 17, 19, 20, 22, 23, 25	SCSI DATA and PARITY	$\overline{SD0\text{-}SD7}$, $\overline{SDP}$	I/O	These pins are the eight bi-directional SCSI data signals and the SCSI parity signal to/from the SCSI bus. Except during arbitration, their direction depends on the state of the I/O signal and the mode, Initiator or Target, of the chip. Parity is not valid during arbitration.
26	ATTENTION	$\overline{ATN}$	I/O	This pin is the bi-directional ATTENTION signal to/from the SCSI bus. It is an output when the controller is programmed as an initiator and an input when programmed as a target.
28	BUSY	$\overline{BSY}$	I/O	This pin is the bi-directional BUSY signal to/from the SCSI bus.
29	ACKNOWLEDGE	$\overline{ACK}$	I/O	This pin is the bi-directional ACKNOWLEDGE signal to/from the SCSI bus. It is an output when the controller is programmed as an initiator and an input when programmed as a target.
31	SCSI BUS RESET	$\overline{SRST}$	I/O	This pin is the bi-directional RESET signal to/from the SCSI bus. A low on this pin indicates a SCSI bus Reset.
32	MESSAGE	$\overline{MSG}$	I/O	This pin is the bi-directional MESSAGE signal to/from the SCSI bus. It is an output when the controller is programmed as a target and an input when programmed as an initiator.
34	SELECT	$\overline{SEL}$	I/O	This pin is the bi-directional SELECT signal to/from the SCSI bus.
35	COMMAND/ DATA	$\overline{C/D}$	I/O	This pin is the bi-directional COMMAND/DATA signal to/from the SCSI bus. It is an output when the controller is programmed as a target and an input when programmed as an initiator.
37	REQUEST	$\overline{REQ}$	I/O	This pin is the bi-directional REQUEST signal to/from the SCSI bus. It is an output when the controller is programmed as a target and an input when programmed as an initiator.
38	INPUT/OUTPUT	$\overline{I/O}$	I/O	This pin is the bi-directional INPUT/OUTPUT signal to/from the SCSI bus. It is an output when the controller is programmed as a target and an input when programmed as an initiator.

RING BUFFER INTERFACE				
PIN NO	**NAME**	**SYMBOL**	**I/O**	**DESCRIPTION**
1-6 67,68	RING BUFFER DATA BUS	DB0-DB7	I/O	These pins are the eight bi-directional data signals to/from the Ring Buffer.
7	DMA CLOCK	DMACLK	O	This output is a buffered clock signal derived from the X1 input.
64	$\overline{DMA\ REQUEST}$	$\overline{DREQ}$	O	This active low output to the external DMA controller is used to request a DMA transfer of data to/from the Ring Buffer.
65	$\overline{DMA\ ACKNOWLEDGE}$	$\overline{DACK}$	I	This active low input from the external DMA controller is used to strobe data to/from the Ring Buffer.
66	SYSTEM DATA BUS PARITY	DBP	I/O	This pin is the parity bit for the Ring Buffer Data Bus.

DESCRIPTION OF PIN FUNCTIONS (CONTINUED)

T-52-33-27

MICROPROCESSOR INTERFACE

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
41-48	BI-DIRECTIONAL EXTERNAL DATA BUS	XD0-XD7	I/O	These pins are open drain general purpose I/O bus signals and have internal 1K pullup resistors.
50	PROCESSOR DMA REQUEST	PDREQ	O	This output is active high when byte transfers to/from the Processor is required.
51	INTERRUPT	INT	O	This output is the interrupt signal to the local processor. This output is active low open drain and has an internal pullup resistor.
52	WRITE STROBE (READ/WRITE)	WR (R/W)	I	When the SCSIC is configured for ALE, this active low strobe is used to latch write data from the AD7-0 bus into the SCSIC. When the SCSIC is configured for AS, the R/W input is used to qualify DS for a read or write cycle.
53	READ STROBE (DATA STROBE)	RD (DS)	I	When the SCSIC is configured for ALE, this active low strobe is used to enable read data from the SCSIC onto the AD7-0 bus. When the SCSIC is configured for AS, this active low signal is used to strobe data into or out of the SCSIC.
54	CHIP ENABLE	CE	I	This input, when low, enables the SCSIC's registers for reading and writing.
55	ADDRESS LATCH ENABLE (ADDRESS STROBE)	ALE (AS)	I	When active, this signal indicates a valid address is on the AD7-0 bus. The local processor must read a SCSIC register to configure the chip for ALE or AS operation.
56-63	LOCAL PROCESSOR ADDRESS/ DATA BUS	AD0-AD7	I/O	These eight signals are the multiplexed address/data bus to/from the local processor.

MISCELLANEOUS

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
49	RESET	RST	I	This active low input causes the MSD95C00 to reset to an initial state. This signal must be held low for at least 1ms. All SCSI signals are deasserted. DREQ is inactive high. PDREQ is inactive low. INT is inactive high. AD7-0 are inputs. DB7-0 are inputs. Refer to individual register descriptions for the reset state of each register.
11	CRYSTAL INPUT	X1	I	A 20 MHz. (max) crystal is connected to this input. A TTL clock may be used as an input to this pin.
10	CRYSTAL OUTPUT	X2	O	A 20 MHz. (max) crystal is connected to this output. If a TTL is clock is connected to X1, this input must be left floating.

POWER and GROUND

PIN NO	NAME	SYMBOL	I/O	DESCRIPTION
8,12,15, 18,21,24, 27,30,33, 36,39	GROUND	GND	P	Ground connections.
9,40	POWER	Vcc	P	+5V Power connection.

SYSTEM DESCRIPTION

The block diagram in Figure 1 illustrates a typical implementation of the MSD95C00 used in a hard drive application. The MSD95C00 provides simple interfacing to the SCSI bus, microprocessor and controller logic.

SCSI Interface

The eighteen SCSI signals may be connected directly to a single ended (open collector) SCSI bus. The MSD95C00 drivers and receivers are fully capable of driving and receiving SCSI bus signals as defined by the ANSI X3.131 specification.

Microprocessor Interface

The microprocessor interface consists of an 8-bit data bus and control bus. With the exception of optional address decoding logic for the $\overline{CE}$ input, all signals are tied directly to the microprocessor eliminating the need for external circuitry.

Controller Interface

The controller interface consists of and 8-bit bi-directional data bus, a clock and a pair of request/acknowledge handshake signals. These signals may be connected directly to memory and controller logic such as the SMC MSD95C02 or MSD95C01 storage controllers.

FUNCTIONAL DESCRIPTION

Arbitration Phase

Arbitration is a system option which allows a SCSI device to gain control of the SCSI bus. Arbitration is required in systems which contain more than one initiator or in systems which support Reselection. While generating an Arbitration phase the MSD95C00 will assert the SCSI Busy signal and it's own ID bit.

Since the Arbitration Phase is a system option, its generation is enabled or disabled via software. Arbitration is enabled in the MSD95C00 by writing a logic 1 to bit 1 of the Mode register during initialization. Arbitration phase timing an Bus Free detection is handled completely by the MSD95C00. If enabled, this phase will be generated prior to a Selection or Reselection phase, with no additional microprocessor intervention, after a Select command (writing a logic 1 to bit 6 of the Command register) has been issued to the MSD95C00. The Arbitrating device with the highest ID typically wins arbitration with Bit 7 having the highest priority and bit 0 having the lowest. Parity is not valid during the Arbitration Phase.

Selection Phase

The Selection phase is generated by an Initiator. The MSD95C00 will assert the SCSI I/O and Select signals during the Selection phase. During the Selection phase the MSD95C00 also asserts it's own SCSI ID bit as well as the SCSI ID bit of the target it wishes to select. Selection phase timing, including Selection Timeout, is handled completely by the MSD95C00. This phase will be generated after a Select command (writing a logic 1 to bit 6 of the Command register) has been issued to the MSD95C00 if bit 0 of the Mode register is set to a logic "1" (Initiator Mode). If bit 0 of the Control register has been set to a logic 1 the SCSI Attention signal will be asserted during the Selection phase. This is part of the SCSI protocol which allows an Initiator to inform the Target being selected that it wishes to send a message to the target.

T-52-33-27

Reselection Phase

Reselection is a system option. The Reselection phase is generated by a Target. The MSD95C00 will assert the SCSI Select signal during the Reselection phase. During the Reselection phase, the MSD95C00 also asserts it's own SCSI ID bit as well as the SCSI ID bit of the initiator it wishes to reselect. Reselection phase timing, including Reselection Timeout, is handled completely by the MSD95C00. This phase will be generated after a Select command (writing a logic 1 to bit 6 of the Command register) has been issued to the MSD95C00 if bit 0 of the Mode register is reset to a logic '0' (Target Mode). This phase should only be used if an Initiator had previously selected a Target and the Target then performed a Disconnect. The Reselection would again establish a connection between the original Initiator Target pair in an effort to complete the command.

Command Phase

The Command phase is generated by a Target. The local microprocessor must write a logic 1 to bit 2 of the Command 2 register. The phase is initiated and data transfer begins when the local microprocessor writes the Byte Counter Low register. The phase is terminated by initiating a new phase or performing a Disconnect command. The Command phase allows a Target to request a Command Descriptor Block (CDB) from the Initiator. Command discriptor blocks are six, ten or twelve bytes in length. The first byte of the command discriptor block indicates the number of bytes which comprise the command discriptor block. After the first byte is passed from the Initiator to the Target the local microprocessor must read the byte from the Target's FIFO, calculate the number of remaining bytes and set up the Target to transfer the remaining bytes. The remaining bytes of the command discriptor block are then transferred to the Target's FIFO. The target microprocessor is informed, via interrupt or polling, of the completion of this transfer. This block is then transferred, via DMA or programmed I/O, from the FIFO to the target microprocessor's memory. The target microprocessor must then digest and execute the command.

Data-In Phase

The Data-In phase is generated by a Target. The Target microprocessor writes a logic 1 into bit 1 of the Command 2 register. The phase is initiated and data transfer begins when the Target microprocessor writes to the Byte Counter Low register. The phase is terminated by initiating a new phase or executing a Disconnect command. The Data-In phase allows data to be transferred from a Target to an Initiator. Data-In and Data-Out transfers may be asynchronous or synchronous. All other transfers, such as message, status and command, are defined by the SCSI protocol as being asynchronous. A typical data-in transfer would transfer data from the Target Ring buffer, through the Target SCSIC's FIFO, across the SCSI bus, into the Initiator SCSI's FIFO and into the Initiators local memory. The Target microprocessor would set up the Target to perform the transfer, initiate the transfer by writing to the Byte Counter Low register and then wait for an interrupt indicating the transfer has been completed. The three bus architecture of the MSD95C00 allows the Initiator and Target microprocessors to perform their housekeeping duties while the data transfer is taking place.

T-52-33-27

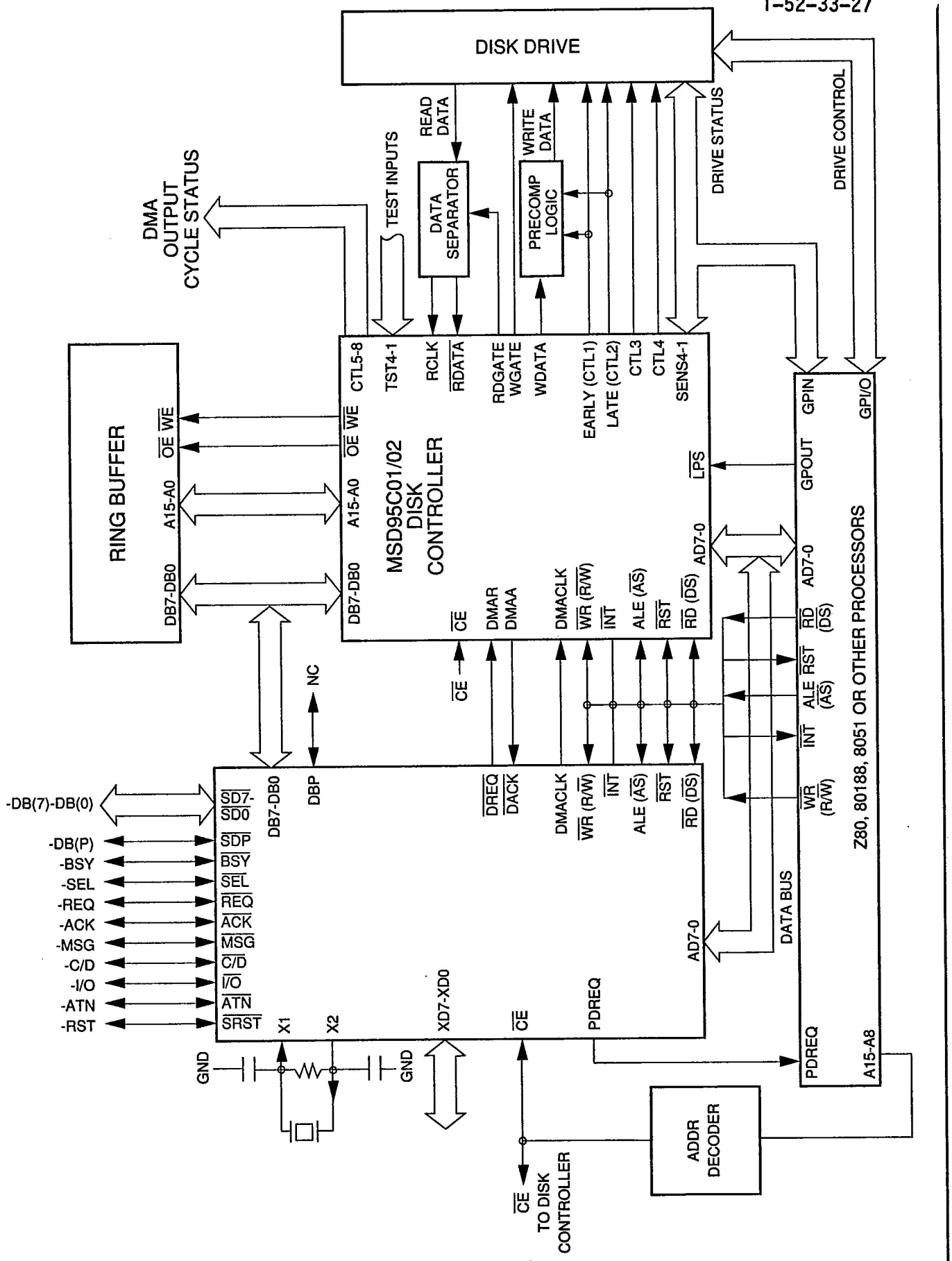


FIGURE 1 - TYPICAL SYSTEM CONFIGURATION (EMBEDDED SCSI DISK DRIVE)

T-52-33-27

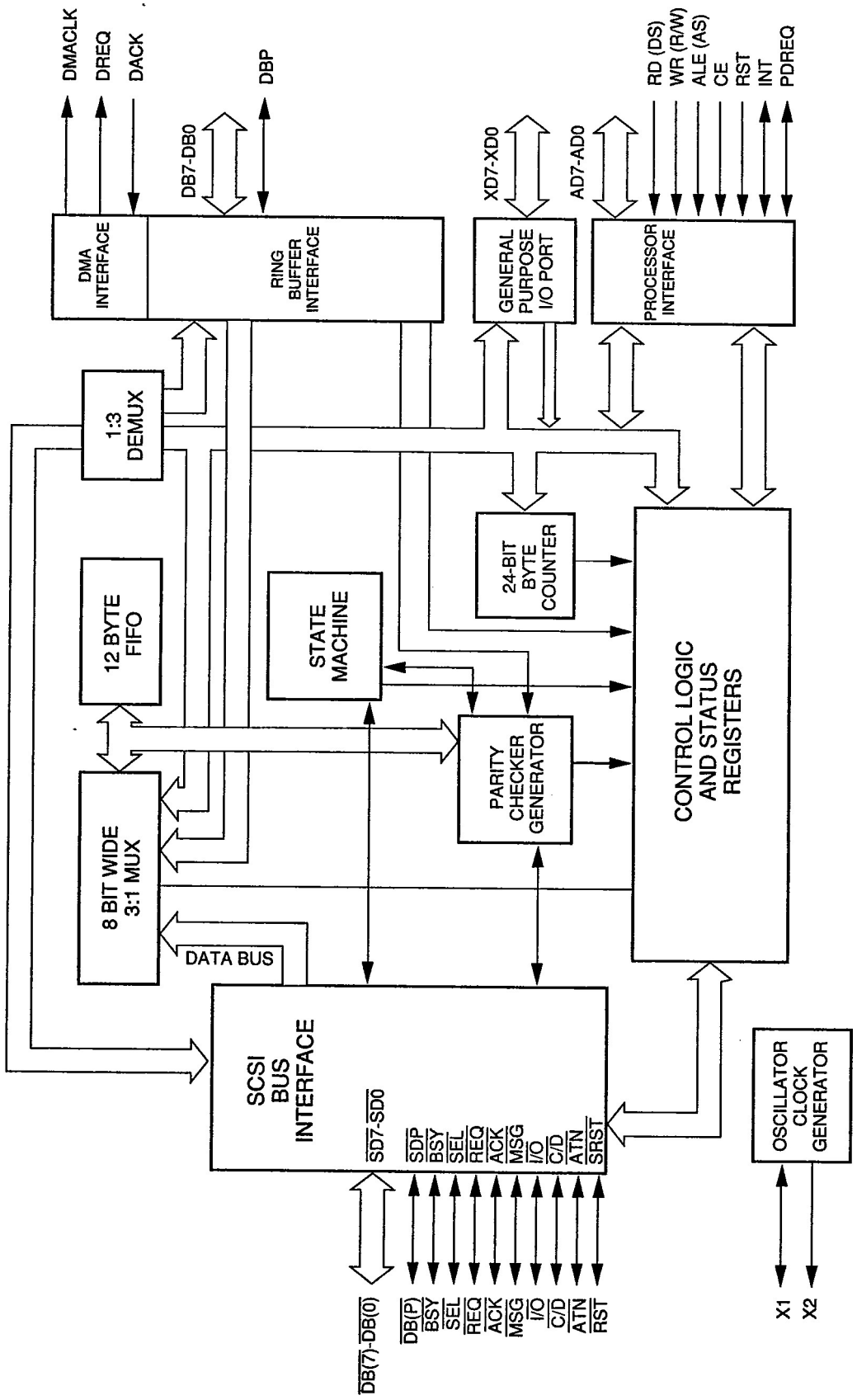


FIGURE 2 - MSD95C00 BLOCK DIAGRAM

Data-Out Phase

The Data-Out phase is generated by a Target. The Target microprocessor writes a logic 0 into each bit of the Command 2 register. The phase is initiated and transfer begins when the Target microprocessor writes to the Byte Counter Low register. The phase is terminated by initiating a new phase or executing a Disconnect command. The Data-Out phase allows data to be transferred from an Initiator to a Target. Data-In and Data-Out transfers may be asynchronous or synchronous. All other transfers, such as message, status and command, are defined by the SCSI protocol as being asynchronous. A typical data-out transfer would transfer data from Initiator memory to the Initiator SCSIC's FIFO, over the SCSI bus, through the Target SCSIC's FIFO then to the Target Ring buffer. The Target microprocessor would set up the Target to perform the transfer, initiate the transfer by writing to the Byte Counter Low register and then wait for an interrupt indicating the transfer has been completed. The three bus architecture of the MSD95C00 allows the Initiator and Target microprocessors to perform their housekeeping duties while the data transfer is taking place.

Message-In Phase

The Message-In phase is generated by a Target. The Target microprocessor writes a logic 1 into bit 7 of the Command 2 register. The phase is initiated and transfer begins when the Target microprocessor writes to the Byte Counter Low register. The phase is terminated by initiating a new phase or executing a Disconnect command. Messages are typically one byte in length. The local microprocessor would write the message byte(s) into the Target FIFO and set the Target up for the proper number of bytes to be transferred. Writing to the Byte Counter Low register generates the phase and initiates the transfer.

Message-Out Phase

The Message-Out phase is generated by a Target. The Target microprocessor writes a logic 1 into bit 6 of the Command 2 register. The phase is initiated and transfer begins when the Target microprocessor writes to the Byte Counter Low register. The phase is terminated by initiating a new phase or executing a Disconnect command. Messages are typically one byte in length. The Initiator microprocessor would write the message byte(s) into the Initiator FIFO. The target microprocessor would set up the Target for a one byte transfer. Writing to the Byte Counter Low register initiates the transfer. If the target microprocessor detects an extended message is to be transferred it must load the Byte Counter to allow the target to transfer the remainder of the message bytes.

Status Phase

The Status phase is generated by a Target. The Target microprocessor writes a logic 1 into bit 3 of the Command 2 register. The phase is initiated and transfer begins when the Target microprocessor writes to the least significant byte of the Byte counter. The phase is terminated by initiating a new phase or executing a Disconnect command. Status transfers are one byte in length. The Target microprocessor would write the status byte into the Target FIFO and set the Target up for a one byte transfer.

Bus Free Phase

The Bus Free phase occurs when no SCSI devices are driving the SCSI bus and the SCSI SEL and BUSY signals have been false for a specified period of time.

Being Selected or Reselected T-52-33-27

Typically Targets may be selected and Initiators may be reselected. A device responds to selection or reselection during a selection or reselection phase if it recognizes it's SCSI ID bit on the bus and there are not more than two ID bits on the bus. Parity, if enabled, must not be in error. The MSD95C00 has two bits, bits 1 and 2 of the Control register, which enable or disable it from responding to an attempted selection or attempted reselection regardless of whether the MSD95C00 is programmed to be an initiator or target. If a selection or reselection is attempted, maskable interrupts may be generated and the appropriate status bits are set.

Interrupts

There are fifteen interrupt causing conditions generated by the MSD95C00, all of which are maskable. These interrupt causing conditions generate status bits in the Status 2, 3 and 4 registers. Reading the Status 2, 3 or 4 registers will reset the interrupt causing condition in that register. Some of these status bits are ORed together and are readable through the Status 1 register. The remaining status bits are directly readable through the Status 1 register. Reading the Status 1 register allows the software to decide which of Status 2, 3 or 4 registers to read. Reading the Status 1 register does not reset the interrupt causing condition. Please refer to Figure 3.

Transfer Modes

Data (any information being passed through the system is referred to as data) may be transferred between the SCSI bus and microprocessor memory. Data may also be transferred between the SCSI bus and the Ring buffer memory. All data transfers to and from the SCSI bus pass through the MSD95C00's FIFO. Data cannot be transferred between the microprocessor and the Ring Buffer through the MSD95C00.

Interrupt Driven I/O

The processor responds to an interrupt by reading the Interrupt Status register. If the SCSIC status bit is active high, the Processor reads the Status 1 register to determine the source of the interrupt.

If the Transfer Requested status bit is active high, the Processor should read the Status 3 register to determine whether it was set by Byte Available or Byte Requested. In response the SCSIC resets the Transfer Requested status bits.

If the Byte Available status bit is set, the processor should read the SCSI Data Out register. The SCSIC clears the Byte Available status bit if, and only if, there is no more data in the FIFO. If the Byte Available status bit is still set, the SCSIC generates a new transfer Request interrupt.

If the Byte Requested status bit is set, the processor should write a byte of data to the SCSIC Data Out register. The SCSIC then clears the Byte Requested status bit if the Byte Counter equals zero or if the FIFO is full. If the Byte Requested status bit remains set after the processor writes the byte of data, the SCSIC generates another Transfer Request interrupt.

DMA Driven I/O

A DMA controller may be used to transfer a Command Descriptor Block, a message or status byte between the MSD95C00's FIFO and processor memory. Transfers are performed when the PDREQ is a function of the Byte

T-52-33-27

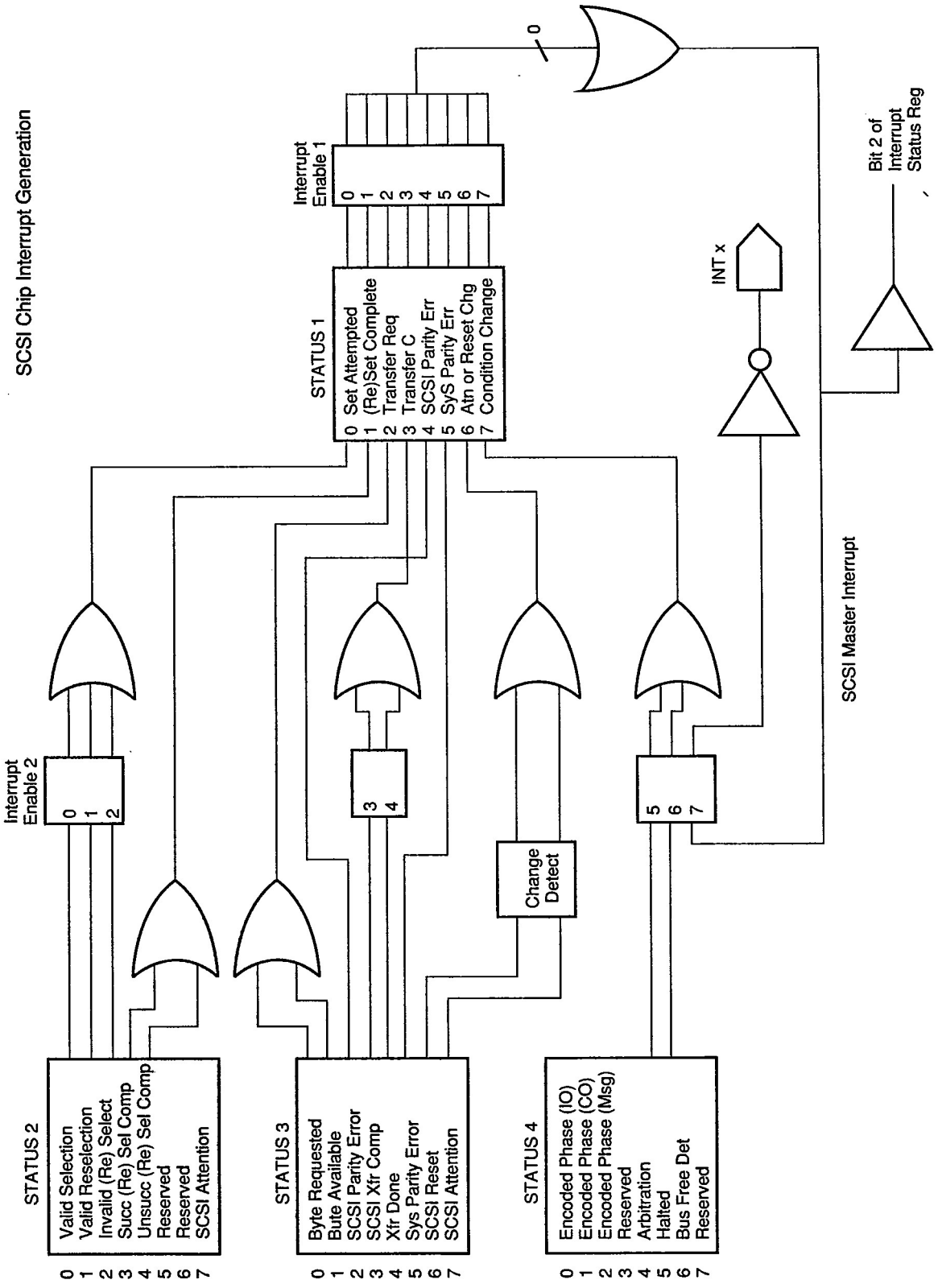


FIGURE 3 - SCSI CHIP INTERRUPT GENERATION

Requested status bit when writing to the FIFO and is a function of the Byte Available bit when reading the FIFO.

Polled I/O

The processor reads the Status 3 register to see if either the Byte Available or Byte Requested status bits are high.

If Byte Available is high, the Processor transfers the byte from the SCSIC Data In register to the Processor or the Processor RAM. If there is no more data in the buffer, the SCSIC clears the Byte Available status bit.

If the Byte Requested is high, the processor transfers the byte from the processor or the processor RAM to the SCSIC Data Out register. If no SCSI REQs are pending or the Buffer is full, the Byte Requested status bit is cleared.

SCSI Parity Error Handling

Initiator (Status, Message In, Data In Phases):

If the Halt On Parity Error bit in the Control Register is set to 1 the SCSIC will halt and set the Halted and PE status bits if data has even parity. If these bits are set, the SCSIC will generate a PE interrupt. If enabled, a Condition Change interrupt will also be generated. In response to the interrupt, the processor reads the Status registers and resets the Parity Error and Condition Change Interrupts.

The processor asserts ATN to request Message Out Phase in order to signal its desire to send either a Message Reject or Message Parity Error. The processor then issues a (Re) Start Command.

Target (Command, Message Out, Data Out Phases):

The SCSIC will set the PE status bit if data has even parity. If the PE bit is set, the SCSIC will generate a PE interrupt. In response to the interrupt, the processor reads the Status registers. Finally, the SCSIC resets the Parity Error Interrupts.

Note: The Halt On Parity Error bit in the Control Register does not affect Target operation.

OPERATION DESCRIPTION

SCSI Read Sequence of Events

The following is an example of a SCSI Initiator reading from a SCSI Target.

A Host system with SCSI ID of 80h wishes to read data from a peripheral containing a hard disk drive with SCSI ID of 04h. The initiator and target SCSI ID's are encoded using three of the 8 bits available at the general purpose I/O port. Assume the system supports arbitration and parity checking. The Host's MSD95C00 has been initialized as per Table 1.

The host µP assembles the six byte Command Descriptor Block in local memory.

Upon detecting the "Halted" interrupt, the host microprocessor must determine the current bus phase. If the Command phase is detected, the host microprocessor must load the Byte counter with the proper number of bytes. The CDB is transferred to the FIFO one byte for each received SREQ.

The host µP then issues a Select command to its MSD95C00. This is accomplished by writing a "1" to bit 6 of the Command 1 register.

The initiator MSD95C00 will wait for a Bus Free Phase. Upon detection the Bus Free phase the initiator MSD95C00 will arbitrate for the bus. If unsuccessful the initiator MSD95C00 will again wait for the Bus Free phase. When successful, the initiator MSD95C00 will generate the Selection phase. If the target MSD95C00 responds to the selection prior to the initiator's selection timeout period the initiator MSD95C00 will set the Successful Selection Complete bit in Status 2 register and generate an interrupt. If the target MSD95C00 does not respond to the selection within the initiator's selection timeout period the initiator MSD95C00 will set the Unsuccessful Selection Complete bit in the Status 2 register and generate an interrupt. Arbitration and Selection phase timing are handled fully by the MSD95C00. The host microprocessor need only initiate the Select command and wait for an interrupt (or poll the Status 1 register for the (re)selection complete bit). Assuming the target MSD95C00 has responded to the selection the CDB would have to be transferred to the target. The target MSD95C00 has been initialized as per Table 2.

The target MSD95C00 will detect when it has been selected. It will respond by asserting the SCSI Busy signal, internally latching the Source ID (the selecting initiator's ID with the target's ID masked off) and generating a Valid Selection (Status 2 register bit 0) interrupt. The target µP would typically read the Interrupt Status register and decide if the target MSD95C00 is the interrupt causing device. If so it would then read the Status 1 register. Reading the Status 1 register allows the µP to decide which of the remaining status registers holds the interrupt causing status bit. In this

TABLE 1

Register	Data	Comments
00h	00h	Asynchronous transfer mode.
01h	7Fh	Initiator, arbitration enable, parity check enable, DREQ multiple, PDREQ level, selection timeout = 1.6 ms.
06h	13h	Enable the following interrupts: Selection Attempted, (Re) Selection Complete, SCSI parity error.
07h	82h	Enable the following interrupts: Valid Reselection, SCSI Master Interrupt.
08h	C4h	Enable reselection, enable PDREQ, enable DREQ.
0Eh	80h	Initiator ID.

TABLE 2 T-52-33-27

Register	Data	Comments
00h	00h	Asynchronous Transfer mode.
01h	66h	Target, Enable Arbitration, Enable Parity, DREQ Single Pulse, PDREQ Pulsed, Selection Timeout = 1.6 ms.
06h	1Bh	Enable the following interrupts: Selection Attempted, (Re)Selection Complete, Transfer Complete, SCSI Parity Error.
07h	99h	Enable the following interrupts: Valid Selection, SCSI Transfer Complete, Transfer Done, SCSI Master Interrupt.
08h	C2h	Enable Selection, Enable REQ, Enable DREQ.
0Eh	04h	Target ID.

case the Status 2 register should be read. The target µP would determine the interrupt causing condition(s) (in this case the Valid Selection bit, Bit 0, would be set). The target uP should also examine the SCSI Attention signal, bit 7 of the Status 2 register, at this time. This will allow the target to determine if the initiator is requesting a Message-Out phase. A Message-Out phase would be necessary if the initiator wished to perform synchronous data transfers for the first time.

If the SCSI Attention Signal is not asserted the target would typically respond with a Command phase. To accomplish this, the target uP would write a 04h into the Command 2 register and an FEh into the Byte Counter Low register. Upon writing the Byte Counter Low register the target MSD95C00 will generate the Command phase and a SCSI REQ signal. The initiator MSD95C00 will respond by supplying the first byte of the CDB and the SCSI ACK signal. The handshaking is automatically handled by the initiator and target MSD95C00 pair.

The target uP would receive an interrupt (or poll the Transfer Complete bit in the Status 1 register) caused by the SCSI Transfer Complete bit in the Status 3 register. It would respond by reading the Data-In register of the MSD95C00.

The target µP would then examine this first byte. The three MSB's indicate the group code and therefore the number of bytes in the CDB. For the Read command a group code "000" is expected, indicating a six byte CDB including the first byte. The target µP would then write an FFh, FFh, FAh to the Byte Counter register. This would initiate a transfer for the remaining five CDB bytes. The SCSI Transfer Complete bit in the Status 3 register would cause a second interrupt informing the µP that the remainder of the CDB is in the target MSD95C00's FIFO.

The target µP could either transfer five bytes from the MSD95C00's FIFO into it's own memory or use a handshake method, by interrogating the Byte Available bit in the Status 3 register, to transfer the remainder of the CDB.

Once the CDB has been transferred to the target µP's memory the µP must digest and execute the Read command.

The target µP then sets-up the hard disk controller, such as the SMC MSD95C01/02, and the target MSD95C00 for the transfer. The target µP initiates a Data-In Phase by writing an 02h to the Command 2 register, and writing the proper byte count, in 1's complement form, into the Byte Counter registers. Upon writing the Byte Counter Low register the target MSD95C00 will generate a Data-In phase and perform the transfer by handshaking with both the initiator MSD95C00 and the MSD95C01/02. The target µP is free to perform any other tasks during the read operation and will be interrupted by the Transfer Done bit, bit 4 of the Status 3 register, at the completion of the transfer.

The initiator's µP would need to examine and respond to the SCSI bus phases. When the Data-In phase is detected, the initiator µP would load the Byte counter with the 1's complement of the number of bytes to be transferred and set up it's DMA controller, if one existed. Upon completion of the transfer the initiator µP would receive a Transfer Done interrupt (Bit 4 of the Status 3 register).

Using a similar algorithm, Status and Message Phase transfers would take place. The target would then disconnect from the SCSI bus allowing a new operation to take place.

REGISTER DESCRIPTION

Reset Register
8-Bits Read Only (ADDRESS 00H)

An initial dummy read configures the chip for ALE or $\overline{AS}$ type timing. Reading the Reset register address places the MSD95C00 into the same state as driving the RST input low and simultaneously reads the general purpose I/O port. A write to any other MSD95C00 register will terminate the reset state as well as write to the addressed register. Both the hardware and software resets will perform the same function as the Clear command in addition to resetting certain register bits as detailed below.

Negotiation Register
8-Bit Write Only (ADDRESS 00H)

The 4 MSB's, bits 7 - 4, of this eight bit write only register are used to program the Transfer Period for synchronous data transfers. The transfer period will be (2 + N)T where T is twice the clock period. For a 20 MHz crystal with the Negotiation register programmed for 0xh the transfer frequency is (2 + 0) 100ns = 200ns = 5MHz.

The 4 LSB's are used to program the SCSI REQ/ACK offset and are reset to zero by a hard or soft System Reset. Programming the 4 LSB's to zero configures the SCSIC for Asynchronous operation. Programming the 4 LSB's for 1 thru 12 configures the SCSIC for Synchronous operation with a REQ/ACK offset value equal to the value programmed. The maximum offset value the MSD95C00 will support is 12. This register should be programmed with a REQ/ACK Offset value regardless of whether the chip is operating in Initiator or Target mode.

MSD95C00
REGISTER BIT MAPS

T-52-33-27

NEGOTIATION REGISTER (WRITE REGISTER—ADDRESS 00H)

TRANSFER PERIOD	REQ/ACK OFFSET

MODE REGISTER (WRITE REGISTER—ADDRESS 01H)

RESERVED	SELECTION TIMEOUT bit 1	bit 0	PDREQ LEVEL/ PULSED	DREQ MULTIPLE/ SINGLE PULSE	PARITY CHECK ENABLE/ DISABLE	ARBITRATE ENABLE/ DISABLE	INITIATOR/ TARGET

BYTE COUNTER HIGH REGISTER (WRITE REGISTER-ADDRESS 02H)

MOST SIGNIFICANT BYTE OF BYTE COUNT REGISTER (1's compliment)

BYTE COUNTER MIDDLE REGISTER (WRITE REGISTER—ADDRESS 03H)

MIDDLE BYTE OF BYTE COUNT REGISTER (1's compliment)

BYTE COUNTER LOW REGISTER (WRITE REGISTER—ADDRESS 04H)

LEAST SIGNIFICANT BYTE OF BYTE COUNT REGISTER (1's compliment)

I/O REGISTER (WRITE REGISTER—ADDRESS 05H)

LATCHED DATA TO XD7 TO XD0 PINS

INTERRUPT ENABLE 1 REGISTER (WRITE REGISTER—ADDRESS 06H)

CONDI-TION CHANGE	ATN or RESET CHANGE	SYSTEM PARITY ERROR	SCSI PARITY ERROR	TRANSFER COMPLETE	TRANSFER REQUEST	(RE)-SELECT COMPLETE	SELEC-TION ATTEMPT-ED

INTERRUPT ENABLE 2 REGISTER (WRITE REGISTER—ADDRESS 07H)

SCSI MASTER INTER-RUPT	BUS FREE DETECT	HALT INTERRUPT	TRANSFER DONE	SCSI TRANSFER COMPLETE	INVALID (RE)-SELECT	VALID RESELECT	VALID SELECT

CONTROL REGISTER (WRITE REGISTER—ADDRESS 08H)

ENABLE DREQ	ENABLE PDREQ	HALT ON PARITY ERROR	ALWAYS 0	ALWAYS 0	ENABLE RESELECT	ENABLE SELECT	AUTO ATTEN-TION ASSERT

COMMAND 1 REGISTER (WRITE REGISTER—ADDRESS 09H)

DISCON-NECT	SELECT	(RE)-START	CLEAR	NEGATE ATTEN-TION	ASSERT ATTEN-TION	NEGATE SCSI RESET SIGNAL	ASSERT SCSI RESET SIGNAL

COMMAND 2 REGISTER (WRITE REGISTER—ADDRESS 0AH)

SET MESSAGE IN	SET MESSAGE OUT	RESERVED	RESERVED	SET STATUS PHASE	SET COMMAND PHASE	SET DATA IN	RESERVED

RESERVED (WRITE REGISTER—ADDRESS 0BH)

(MSB)	RESERVED	(LSB)

RESERVED (WRITE REGISTER—ADDRESS 0CH)

(MSB)	RESERVED	(LSB)

DESTINATION ID REGISTER (WRITE REGISTER—ADDRESS 0DH)

(MSB)	DESTINATION ID	(LSB)

SCSI ID REGISTER (WRITE REGISTER—ADDRESS 0EH)

(MSB)	SCSI ID (NODE ID)	(LSB)

DATA OUT REGISTER (WRITE REGISTER—ADDRESS 0FH)

(MSB)	DATA TO BE OUTPUT TO THE SCSI BUS	(LSB)

RESET REGISTER (READ REGISTER—ADDRESS 00H)

XD7-XD0 (IN)

MODE REGISTER (READ REGISTER—ADDRESS 01H)

RESERVED	SELECTION TIMEOUT	PDREQ LEVEL/ PULSED	DREQ MULTIPLE/ SINGLE PULSE	PARITY CHECK ENABLE/ DISABLE	ARBITRA-TION ENABLE/ DISABLE	INITIATOR/ TARGET

BYTE COUNTER HIGH REGISTER (READ REGISTER-ADDRESS 02H)

(MSB)	MOST SIGNIFICANT BYTE	(LSB)

BYTE COUNTER MIDDLE REGISTER (READ REGISTER—ADDRESS 03H)

(MSB)	MIDDLE SIGNIFICANT BYTE	(LSB)

BYTE COUNTER LOW REGISTER (READ REGISTER—ADDRESS 04H)

(MSB)	LEAST SIGNIFICANT BYTE	(LSB)

I/O REGISTER (READ REGISTER—ADDRESS 05H)

(MSB)	LATCHED DATA FROM XD7-XD0 PINS (IN)	(LSB)

INTERRUPT ENABLE 1 REGISTER (READ REGISTER—ADDRESS 06H)

CONDI-TION CHANGE	ATN or RESET CHANGE	SYSTEM PARITY ERROR	PARITY ERROR	TRANSFER DONE	TRANSFER REQUEST	(RE)-SELECT COMPLETE	SELEC-TION ATTEMPT-ED

INTERRUPT ENABLE 2 REGISTER (READ REGISTER—ADDRESS 07H)

MASTER INTER-RUPT	BUS FREE DETECT	HALT INTERRUPT ENABLE	TRANSFER DONE	SCSI TRANSFER COMPLETE	INVALID (RE)-SELECT	VALID RESELECT	VALID SELEC-TION

CONTROL REGISTER (READ REGISTER—ADDRESS 08H)

ENABLE DREQ	ENABLE PDREQ	HALT ON PARITY ERROR	ALWAYS 0	ALWAYS 0	ENABLE RESELECT	ENABLE SELECT	AUTO ATTEN-TION ASSERT

INTERRUPT STATUS REGISTER (READ REGISTER—ADDRESS 09H)

RESERVED	SCSI INTER-RUPT	RESERVED

STATUS 1 REGISTER (READ REGISTER—ADDRESS 0AH)

CONDI-TION CHANGE	ATTN or RESET CHANGE	SYSTEM PARITY ERROR	SCSI PARITY ERROR	TRANSFER COMPLETE	TRANSFER REQUEST	(RE)-SELECT COMPLETE	SELEC-TION AT-TEMPTED

STATUS 2 REGISTER (READ REGISTER—ADDRESS 0BH)

SCSI ATTN SIGNAL	RESERVED	RESERVED	UNSUC-CESS (RE)-SELECT COMPLETE	SUC-CESSFUL (RE)-SELECT COMPLETE	INVALID (RE)-SELECT	VALID RESELECT	VALID SELEC-TION

STATUS 3 REGISTER (READ REGISTER—ADDRESS 0CH)

SCSI ATTN SIGNAL	SCSI RESET	SYSTEM PARITY ERROR	TRANSFER DONE	SCSI TRANSFER COMPLETE	SCSI PARITY ERROR	BYTE AVAILABLE	BYTE RE-QUESTED

STATUS 4 REGISTER (READ REGISTER—ADDRESS 0DH)

RESERVED	BUS FREE DETECTED	HALTED	ARBITRA-TION	RESERVED	ENCODED PHASE MSG	ENCODED PHASE C/D	ENCODED PHASE I/O

SCSI BUS ID REGISTER (READ REGISTER—ADDRESS 0EH)

(MSB)	SCSI BUS ID (NODE SOURCE ID)	(LSB)

DATA IN REGISTER (READ REGISTER—ADDRESS 0FH)

(MSB)	DATA FROM BUFFER	(LSB)

T-52-33-27

Mode Register
8-Bits Read/Write (ADDRESS 01H)

This 8 bit Read/Write register defines the operating mode of the SCSIC. The bits in this register are reset to zero by a hard or soft System Reset. Refer to Table 3 for the description of the Mode Register bits.

TABLE 3 - Mode Register

BIT NO.	BIT NAME	DESCRIPTION
0	Initiator/ Target	Writing a "1" to this bit will place the chip into an initiator mode. Writing a "0" to this bit places the chip into a target mode. The state of this bit will not prevent the chip from being selected or reselected by another device. The state of this bit determines whether the select command will start either the select function or the reselect function.
1	Arbitration Enable/ Disable	Writing a "1" to this bit enables Arbitration. Writing a "0" to this bit disables Arbitration. An Arbitration phase will occur following a Bus Free Phase if the Select Command has been issued (bit 6 of the Command 1 register) if Arbitration Enable/Disable = 1.
2	Parity Check Enable	Writing a "1" to this bit enables the MSD95C00 parity checking for all SCSI bus phases except Bus Free and Arbitration. When this bit is "0", Parity on the SCSI bus will not be checked.
3	DREQ Multiple/ Single Pulse Mode	Writing a "1" to this bit will allow the SCSIC to generate up to 12 $\overline{\text{DREQ}}$ pulses before receiving the first $\overline{\text{DACK}}$ from the external controller logic. When this bit is "0", the SCSIC will not generate the next $\overline{\text{DREQ}}$ unless it has received the previous $\overline{\text{DACK}}$. In both cases, a transfer is not considered complete until the number of $\overline{\text{DACK}}$'s received equals the number of $\overline{\text{DREQ}}$'s generated.
4	PDREQ Level/ Pulsed	Writing a "1" to this bit will cause the PDREQ signal to operate as a level. When receiving from the SCSI bus PDREQ will be high as long as the buffer is not empty. When sending to the SCSI bus PDREQ will be high as long as the buffer is not full. Writing a "0" to this bit will cause the PDREQ signal to operate as a pulse. The MSD95C00 will drive PDREQ low if receiving and the Data IN register is read. PDREQ will also be driven low when sending and the Data Out register is written. PDREQ will then be driven high if there is more data to transfer.
6,5	Selection Timeout	These two bits are used to select the following SCSI Selection Timeout:
7	Reserved.	Must be reset to "0".

Bit 6	Bit 5	Timeout*
0	0	839ms
0	1	210ms
1	0	52ms
1	1	1.6ms

*based on 20MHz crystal operation

Byte Counter High Register
8-Bit Read/Write (Address 02H)

This 8-bit Read/Write register holds the most significant byte that is to be loaded into the Byte Counter. The data is transferred from the Byte Counter High Register into the Byte Counter when the Byte Counter Low register is loaded. Bit 7 is the MSB and bit 0 is the LSB. The Byte Counter registers are loaded with the 1's complement of the desired byte count.

Byte Counter Middle Register
8-Bit Read/Write (Address 03H)

This 8- bit Read/Write register holds the middle byte of data that is to be loaded into the Byte Counter. The data is transferred from the Byte Counter Middle Register into the Byte Counter when the Byte Counter Low register is loaded. Bit 7 is the MSB and bit 0 is the LSB. The Byte Counter registers are loaded with the 1's complement of the desired byte count.

Byte Counter Low Register
8-Bit Read/Write (Address 04H)

This 8-bit Read/Write register holds the least significant byte of data that is to be loaded into the Byte Counter. The data is transferred into the Byte Counter when the Byte Counter Low register is loaded. Bit 7 is the MSB and bit 0 is the LSB. The Byte Counter registers are loaded with the 1's complement of the desired byte count.

I/O Register
8-Bit Read/Write (Address 05H)

This 8-bit Read/Write register is an eight bit bi-directional I/O port available to the processor. Data written to this register will be latched and available on the XD7-XD0 pins. Inverted data present on the XD7-XD0 pins will be available to the Processor when this register is read. The XD7-XD0 I/O pins are open drain with internal pullup resistors.

Interrupt Enable 1 Register
8-Bit Read/Write (Address 06H)

This eight bit Read/Write register enables or disables certain interrupt causing conditions to the microcomputer. Reading this register reflects the states of the bits in it. The bits in this register are cleared to zero by a hard or soft System Reset. Refer to Table 4 for a description of the Interrupt Enable 1 Register bits.

TABLE 4 - Interrupt Enable 1 Register T-52-33-27

BIT NO.	BIT NAME	DESCRIPTION
0	Selection Attempted Interrupt	When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit high when the Selection Attempted bit in the Status 1 register is set to one. When this bit is reset to "0", the Master Interrupt will not be driven high for this condition.
1	(Re)Selection Complete Interrupt Enable	When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the (Re)Selection Complete bit in the Status 1 register is set to one. If this bit is "0", the Master Interrupt will not be driven high for this condition.
2	Transfer Request Interrupt	When the bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the Transfer Request bit in the Status 1 register is set to one. If this bit is "0", the Master Interrupt will not be driven high for this condition.
3	Transfer Complete Interrupt Enable	When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the Transfer Complete Interrupt bit in the Status 1 register is set to one. The Master Interrupt will not be driven high for this condition.
4	SCSI Parity Error Interrupt Enable	When this bit is set to "1", the MSD95C00 drives the SCSI Master Interrupt bit active high when the SCSI Parity Error bit in the Status 1 register is set to one. When this bit is "0", the Master Interrupt will not be driven high for this condition.
5	System Parity Error Interrupt Enable	When this bit is set to "1", the MSD95C00 will drive the SCSI Master Interrupt bit active high when the System Parity Error bit in the Status 1 register is set to one. When this bit is "0", the Master Interrupt will not be driven high for this condition.
6	SCSI ATN or Reset Change Interrupt Enable	When this bit is set to "1", The MSD95C00 will drive the SCSI Master Interrupt bit active high when the SCSI ATN or Reset Change bit in the Status 1 register is set to 1. When this bit is "0", the Master Interrupt will not be driven high for this condition.
7	Condition Change Interrupt Enable	When this bit is set to "1", the MSD95C00 will drive the SCSI Master Interrupt bit active high when the Condition Change bit in the Status 1 register is set to one. When this bit is "0", the Master Interrupt will not be driven high for this condition.

Interrupt Enable 2 Register
8-Bit Read/Write (Address 07H)

This eight bit Read/Write register enables or disables certain microprocessor interrupt causing conditions. Reading this register reflects the states of the bits in it. The bits in this register are cleared to zero by a hard or soft System Reset. Refer to Table 5 for a description of the Interrupt Enable 2 Register bits.

TABLE 5 - Interrupt Enable 2 Register

BIT NO.	BIT NAME	DESCRIPTION
0	Valid Selection Interrupt Enable	When this bit is set to "1", the SCSIC will set the Selection Attempted bit in the Status 1 register to one when the Valid Reselection bit in the Status 2 register is active high. When this bit is "0", the Selection Attempted bit cannot be set by this condition.
1	Valid Reselection Interrupt Enable	When this bit is set to "1", the SCSIC will set the Selection Attempted bit in the Status 1 register to one when the Valid Reselection bit in the Status 2 register is active high. When this bit is "0", the Selection Attempted bit cannot be set by this condition.
2	Invalid (Re)Selection Interrupt Enable	Setting this bit to "1" will cause the SCSIC to set the Selection Attempted bit in the Status 1 register to one when the Invalid (Re)Selection bit in the Status 2 register is active high. If this bit is "0", the Selection Attempted bit cannot be set by this condition.
3	SCSI Transfer Complete Interrupt Enable	Setting this bit to "1" will cause the SCSIC to set the Transfer Complete Interrupt bit in the Status 1 register to one when the SCSI Transfer Complete bit in the Status 3 register is active high. If this bit is "0", the Transfer Complete Interrupt bit cannot be set by this condition.
4	Transfer Done Interrupt Enable	Setting this bit to "1" will cause the MSD95C00 to set the Transfer Complete Interrupt bit in the Status 1 register to one when the Transfer Done bit in the Status 3 register is active high. If this bit is "0", the Transfer Complete Interrupt bit cannot be set by this condition.

TABLE 5 - Interrupt Enable 2 Register

BIT NO.	BIT NAME	DESCRIPTION
5	Halted Interrupt Enable	Setting this bit to "1" will cause the MSD95C00 to set the Condition Change bit in the Status 1 register to one when the Halted bit in the Status 4 register goes high. If this bit is "0", the Condition Change bit cannot be set by this condition.
6	Bus Free Phase Detect Interrupt Enable	Setting this bit to "1" will cause the MSD95C00 to set the Condition Change bit in the Status 1 register to one when the Bus Free Phase Detect bit in the Status 4 register is active high. If this bit is "0", the Condition Change bit cannot be set by this condition.
7	SCSI Master Interrupt Enable	Setting this bit to "1" will cause the MSD95C00 to drive its $\overline{INT}$ output active low when an enabled condition causes one of the bits in the Status 1 register to go high. If this bit is "0", the $\overline{INT}$ pin cannot be driven low.

Control Register
8-Bit Read/Write (Address 08H)

This 8 bit Read/Write register is used to control chip operation. The bits are reset to zero by a hard or soft System Reset. Refer to Table 6 for a description of the Control Register bits.

TABLE 6 - Control Register

BIT NO.	BIT NAME	DESCRIPTION
0	Auto ATN Assert	When this bit is set to "1", the MSD95C00 will automatically assert the SCSI bus ATN signal before beginning the selection phase of the Select command. When this bit is reset to "0", ATN will not be asserted.
1	Enable Selection	When this bit is set to "1", the MSD95C00 will generate a Valid Selection interrupt when selected by another SCSI device. When this bit is reset to "0", the MSD95C00 will generate an Invalid (Re)Selection interrupt when another SCSI device tries to select it. The state of this bit will not prevent the chip from attempting to select or reselect another SCSI device.
2	Enable Reselection	When this bit is set to "1", the MSD95C00 will generate a Valid Reselection interrupt when reselected by another SCSI device. When this bit is reset to "0", the MSD95C00 will generate an Invalid (Re)Selection interrupt when another SCSI device tries to reselect it. The state of this bit will not prevent the chip from attempting to select or reselect another SCSI device.
3		Always 0
4		Always 0
5	Halt On Parity Error	When this bit is set to "1" and the MSD95C00 is operating in the Initiator mode, the MSD95C00 will not assert SACK for bytes with bad parity during Status, Message-In or Data-In phase transfers. This bit does not affect operation in Target mode. When this bit is reset to "0", the MSD95C00 will negate SACK regardless of parity.
6	Enable PDREQ	When this bit is set to "1", the SCSIC will be able to drive the PDREQ output active high. When this bit is reset to "0", the PDREQ output will be driven low.
7	Enable DREQ	When this bit is set to "1", the MSD95C00 will be able to drive the $\overline{DREQ}$ output active low. When this bit is reset to "0", the $\overline{DREQ}$ output will be driven high.

Interrupt Status Register
8-Bit Read Only (Address 09H)

This 8 bit Read Only register contains information about the internal MSD95C00 operation. Refer to Table 7 for a description of the Interrupt Status Register bits.

TABLE 7 - Interrupt Status Register

BIT NO.	BIT NAME	DESCRIPTION
1,0		Always 0
2	SCSI Interrupt	This bit is set to "1" when one of the enabled interrupt causing conditions causes a bit in the Status 1 register to go active high. It is reset to "0" when the interrupt causing condition(s) are cleared.
7,6, 5,4,3		Always 0

Command 1 Register
8 - Bit Write Only (Address 09H)

This Write Only register is used to initiate one of the Select or Reselect operations and to assert or negate the SCSI bus signals. Except for the Clear bit, the states of these bits are used to generate a strobe and are not latched in the MSD95C00. A hard or soft System Reset will cause the signals controlled by this register to be negated and the Clear bit to be reset to "0". Refer to Table 8 for a description of the Command 1 Register bits

TABLE 8 - Command 1 Register

BIT NO.	BIT NAME	DESCRIPTION
0	Assert SCSI Reset Signal	Setting this bit to "1" will cause the MSD95C00 to assert the SCSI bus Reset signal (SRST).
1	Negate SCSI Reset Signal	Setting this bit to "1" will cause the MSD95C00 to negate the SCSI bus Reset signal (SRST).
2	Assert ATN Signal	Setting this bit to "1" will cause the MSD95C00 to assert the SCSI bus Attention signal (ATN).
3	Negate ATN Signal	Setting this bit to "1" will cause the SCSI chip to negate the SCSI bus Attention signal (ATN).
4	Clear	Setting this bit to "1" will cause the chip to go into the Clear state and reset all of the internal counters, reset the latched status bits, reset the SCSI Master Interrupt Enable, reset the bits in the Command 2 Register, disconnect from the SCSI bus and negate the SCSI control signals. Resetting this bit to "0" will terminate the Clear state. After setting this bit to "1", the Processor must wait a minimum of one microsecond before clearing it.
5	(Re)Start	When the MSD95C00 is operating in the Initiator mode, writing a "1" to this bit will cause chip operation, that was interrupted by detection of a parity error on the SCSI data bus, to continue (this condition can only occur when the Halt On Parity Error bit in the Control register is set to "1"). Also, writing a "1" to this bit after the MSD95C00 was halted by SREQ going active when the byte counter was equal to "0" will cause the MSD95C00 to respond with SACK. This will allow the Initiator to perform single byte transfers without loading the Byte Counter (data may be written to the buffer before or after writing to the Command register). This bit does not affect Target mode chip operation.
6	Select	Setting this bit to "1" will cause the MSD95C00 to initiate a Select operation, a Select with ATN asserted operation, an Arbitrate and Select operation, an Arbitrate and Select with ATN asserted operation or an Arbitrate and Reselect operation. The operation initiated depends on the state of the Target/Initiator and Arbitration Enable/Disable bits in the Mode register and the Auto-ATN Assert bit in the Control register.
7	Disconnect	Setting this bit to "1" will cause the MSD95C00 to stop driving all of the SCSI Data bus and Control signals.

Status 1 Register
8-Bit Read Only (Address 0AH)

This 8-bit Read only register contains information about the internal MSD95C00 operation. Refer to Table 9 for a description of the Status 1 Register bits.

TABLE 9 - Status 1 Register

BIT NO.	BIT NAME	DESCRIPTION
0	Selection Attempted	This bit is set to "1" by the active and enabled state of either the Valid Select, Valid Reselect or Invalid (Re)Select status bits in the Status 2 register. It is reset by reading the Status 2 register.
1	(Re)Selection Complete	This bit is set to "1" by the active state of either the Successful (Re)Selection Complete or Unsuccessful (Re)Selection Complete status bits in the Status 2 register. It is reset by reading the Status 2 register.
2	Transfer Request	This bit is set to "1" by the active state of either the Byte Available or Byte Requested status bits in the Status 3 register. It is reset by reading the Status 3 register. It will be set again after the Data-In Register is read if Byte Available is still high or when the Data-Out Register is written and Byte Requested is still high.
3	Transfer Complete	This bit is set to "1" when either the Transfer Done or SCSI Transfer Complete bits in the Status 3 register go active high and their respective bits in the Interrupt Enable 2 Register are set to one. It reset by reading the Status 3 register.
4	SCSI Parity Error	This bit is set to "1" when the SCSI Parity Error bit in the Status 3 register goes active high. It is reset by reading the Status 3 register.
5	System Parity Error	This bit is set to "1" when the System Parity Error bit in the Status 3 register goes active high. It is reset by reading the Status 3 register.

TABLE 9 - Status 1 Register (continued)

T-52-33-27

BIT NO.	BIT NAME	DESCRIPTION
6	SCSI ATN or RESET Change	This bit is set to "1" when either the SCSI ATN or RESET signal changes from the high to low or low to high state. It is reset by reading the Status 3 register.
7	Condition Change	This bit is set to "1" when either the (enabled) Bus Free Detected or Halted bits in the Status 4 register go active high. It is reset by reading the Status 4 register.

Command 2 Register
8-Bit Write Only (Address 0AH)

This Write Only register is used to initiate a new phase when the SCSIC is in Target mode. A hard or soft System Reset or a Disconnect command will clear all the bits in this register to "0". When the Initiator detects that the SCSI Data Bus is changing direction from out (the Initiator driving) to in (the Target driving) it will release the SCSI Data bus within a Data Release Time (400ns) of I/O being asserted. This condition can occur when the Target begins a Message In, Status or Data In phase.

When the Target switches the SCSI Data Bus direction from in (the Target driving) to out (the Initiator driving) it will release the SCSI Data bus within a Deskew delay (45ns) of negating I/O. This condition can occur when the Target begins a Message Out, Command or Data Out phase.

Note that the Processor must delay at least 800ns after issuing a Set Phase type command before writing to the byte counter. The phase will be generated upon writing to the LSB of the Byte Count register. Phases must not be changed unless the FIFO is empty. Refer to table 10 for a description of the Command 2 Register bits. The Message Out Phase is generated by setting bits 7 thru 0 to zero causing C/D, I/O and MSG to be negated.

TABLE 10 - Command 2 Register

BIT NO.	BIT NAME	DESCRIPTION
0	Reserved	Must be set to "0" at all times.
1	Set Data In Phase	Setting this bit to "1" will cause the MSD95C00 to assert the I/O signal and negate the MSG and C/D signals.
2	Set Command Phase	Setting this bit to "1" will cause the MSD95C00 to assert the C/D signal and negate the I/O and MSG signal.
3	Set Status Phase	Setting this bit to "1" will cause the MSD95C00 to assert the C/D and I/O signals and negate the MSG signal.
5,4	Reserved	Must be set to "0" at all times.
6	Set Message Out Phase	Setting this bit to "1" will cause the MSD95C00 to assert the C/D and MSG signals and negate the I/O signal.
7	Set Message In Phase	Setting this bit to "1" will cause the MSD95C00 to assert the C/D, I/O and MSG signals.

Status 2 Register
8 - Bit Read Only (Address 0BH)

This 8 bit Read Only register contains information about the internal MSD95C00 operation. Refer to Table 11 for a description of the Status 2 Register bits.

TABLE 11 - Status 2 Register

BIT NO.	BIT NAME	DESCRIPTION
0	Valid Selection	This bit is set to "1" when the MSD95C00 has been selected by another SCSI device. In order to be selected, the Enable Selection bit in the Control Register must be in the correct state. This bit is reset by reading the Status 2 register.
1	Valid Reselection	This bit is set to "1" when the MSD95C00 has been reselected by another SCSI device. In order to be reselected, the Enable Reselection bit in the Control Register must be in the correct state. This bit is reset by reading the Status 2 register.
2	Invalid (Re)Selection	This bit is set to "1" when another SCSI device attempts to select or reselect the SCSIC and the corresponding enable bit in the Mode register is not in the correct state. This bit is reset by reading the Status 2 register.
3	Successfu (RE)Selection Complete	This bit is set to "1" when the MSD95C00 has successfully selected or reselected another SCSI device and that device has responded by asserting BSY. Also, this bit is set to "1" at the trailing edge of SEL when a device has selected or reselected this device. This bit is reset by reading the Status 2 register.
4	Unsuccessful (RE)Selection Complete	This bit is set to "1" when the MSD95C00 has attempted to select or reselect another SCSI device and that device has not responded by asserting BSY within the programmed Selection Timeout Delay. This bit is reset by reading the Status 2 register.
6,5	Reserved	
7	SCSI ATN	This bit reflects the state of the ATN bit on the SCSI bus. It is active high when the ATN signal is asserted and active low when the ATN signal is deasserted.

Status 3 Register
8-Bit Read Only (Address 0CH) T-52-33-27

This 8 bit Read Only register contains information about the internal MSD95C00 operation. Refer to Table 12 for a description of the Status 3 Register bits.

TABLE 12 - Status 3 Register

BIT NO.	BIT NAME	DESCRIPTION
0	Byte Requested	This bit is active high when transferring to the SCSI Data bus if there is room for more requested data in the FIFO and the Byte counter is not zero.
1	Byte Available	This bit is active high whenever there is data from the SCSI Data Bus in the FIFO for transfer to the Processor or Ring Buffer Ram.
2	SCSI Parity Error	This bit is set to "1" if parity checking is enabled and the SCSI chip detects even (bad) parity on received transfers over the SCSI data bus during any Information phase. It is reset by reading the Status 3 register.
3	SCSI Transfer Complete	This bit is active high when the Byte Counter End Count condition is active high and the last byte has been transferred from the SCSI Bus into the FIFO when the chip is operating in the Target mode during Message Out, Command or Data Out phases. In all other cases, this status bit will function the same as Transfer Done.
4	Transfer Done	This bit is active high when the Byte Counter End Count condition is active high and the last byte has been transferred out of the FIFO to the SCSI Data bus, the Processor port or the Ring Buffer DMA port.
5	System Parity Error	This bit is set to "1" when the MSD95C00 detects even (bad) parity on the System Data Bus. It is reset by reading the Status 3 register.
6	SCSI Reset	This bit reflects the state of the RST signal on the SCSI bus. It is high when the RST signal is asserted and low when the RST signal is deasserted.
7	SCSI Attention	This bit reflects the state of the ATN signal on the SCSI bus. It is high when the ATN signal is asserted and low when the ATN signal is deasserted.

Status 4 Register
8-Bit Read Only (Address 0DH)

This 8 bit Read Only register contains information about the internal SCSIC operation. Refer to Table 13 for a description of the Status 4 Register bits.

TABLE 13 - Status 4 Register

BIT NO.	BIT NAME	DESCRIPTION
2-0	Encoded Phase	<table><tr><th>Bit 2 MSG</th><th>Bit 1 C/D</th><th>Bit 0 I/O</th><th>INFORMATION PHASE</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Data Out Phase</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Data In Phase</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Command Phase</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Status Phase</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Reserved</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Reserved</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Message Out Phase</td></tr><tr><td>1</td><td>1</td><td>1</td><td>Message In Phase</td></tr></table> These bits reflect the SCSI MSG, C/D and I/O signals. They are used to identify the SCSI Information phases. Refer to the table above.
3		Reserved.
4	Arbitration (window)	This bit goes high four to five internal clock cycles after BSY and SEL are both continuously false. The bit remains high three to four internal clock cycles after the bus is no longer free.
5	Halted	This bit can only be set when the chip is operating in the Initiator mode. It is set by SREQ going active when the Byte Counter is "0". It can also be set when a parity error is detected on the SCSI Data bus. This bit is reset by reading the Status 4 register.
6	Bus Free Phase Detect	This bit is the output of the Bus Free detection circuit. It is latched high when the Bus Free phase, as specified in the SCSI specification, is detected on the SCSI Bus. This bit is reset by reading Status 4 register.
7		Reserved.

Destination ID Register
8-Bit Write Only (Address 0EH)

This 8-bit register Write Only is used to hold the value of the SCSI ID of the device that is to be Selected or Reselected.

SCSI Bus ID Register
8-Bit Read Only (Address 0EH)

This 8-bit Read Only register holds the ID that had been latched from the SCSI bus when an attempt was made to Select or Reselect the SCSIC. The SCSIC's SCSI ID bit is masked off leaving the ID of the device attempting the Selection or Reselection.

SCSI ID Register
8-Bit Write Only (Address 0EH)

This 8-bit Write Only register is used to hold the ID assigned to the MSD95C00.

Data In Register
8-Bit Read Only (Address 0FH) T-52-33-27

This 8-bit Read Only register is used by the processor during programmed I/O or processor port DMA transfers. It is used to read data received from the SCSI bus which is presently in the internal buffer.

Data Out Register
8-Bit Write Only (Address 0FH)

This 8-bit Write Only register is used by the Processor during programmed I/O or Processor port DMA transfers. The data loaded into this register is output to the SCSI bus via the internal buffer.

COMMANDS

The SCSIC is an interface between the SCSI bus and the initiator/target unit. When programmed as an initiator (or target supporting reselection), it controls the selection and arbitration process. As a target, it manages the receipt of the command packet from the initiator. All other operations are managed by an outside processor. The typical flow of control progresses as follows:

1) The initiator's processor builds the command block.
2) The processor then instructs the initiating SCSIC to begin Selection. Arbitration, if enabled, is handled by the chip.
3) Once the target unit is selected, the target's processor instructs the target SCSIC to set up a command phase (other phases possible at this point include message, status or data phases).
4) The first byte is transmitted to the target.
5) The target SCSIC modifies its processor (through polling/interrupt) that it is holding the byte. The processor reads the byte in order to determine the command length.
6) The target processor instructs its SCSIC to transfer the remaining bytes.
7) The command packet now resides in the target SCSIC's FIFO buffer.
8) The target SCSIC notifies its processor (through polling/interrupt) that the command packet is available.
9) The processor transfers the command packet into its own memory. The processor is now responsible for digesting and executing the command.
10) While the target's processor executes each command, the initiator and target SCSIC's handle handshaking associated with the command.

TABLE 14 - MSD95C00 COMMANDS

COMM CODE (HEX)	COMMAND	SCSI	CCS
00	Test Unity Ready	optional	mandatory
03	Request Sense	mandatory	mandatory
04	Format Unit	mandatory	mandatory
08	Read	mandatory	mandatory
0A	Write	mandatory	mandatory
01	Rezero Unit	optional	optional
05	Check Track Format	vendor unique	
0B	Seek	optional	optional
12	Inquiry	extended	mandatory
1A	Mode Sense	optional	optional
25	Read Capacity	extended	mandatory
06	Format Track	vendor unique	
0E	Assign Alt Track	vendor unique	
15	Mode Select	optional	optional
16	Reserve Unit	optional	mandatory
17	Release Unit	optional	optional
1C	Receive Diag Result	optional	optional
1D	Send Diagnostics	optional	mandatory
2E	Write and Verify	optional	optional

T-52-33-27

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0° to +70°C
Storage Temperature Range ..... -55° to +150°C
Lead Temperature (soldering, 10 sec.) ..... +300°C
Positive Voltage on any Pin, with respect to Ground ..... V_{cc} +0.3V
Negative Voltage on any Pin, with respect to Ground ..... -0.3V
Maximum Voltage on V_{cc} pin 7.0V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL SPECIFICATIONS (T_A = 0° to 70°C, V_{cc} = 5.0V ± 5%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Supply Current	I_{cc}			35	mA	V_{cc} = 5.25V
Output Voltage						
High	V_{OH1}	2.4			V	I_{OH1} = -400µA. All outputs except SCSI, Interrupt and XD0-XD7.
	V_{OH2}	2.4			V	I_{OH2} = -400µA. XD0- XD7 and Interrupt. Open drain with pull-up.
Low	V_{OL1}			0.4	V	I_{OL1} = 4mA. All outputs except SCSI and XD0 - XD7.
	V_{OL2}			0.4	V	I_{OL2} =2mA. XD0 - XD7.
	V_{OL3}			0.4	V	I_{OL3} = 48mA. SCSI outputs.
Input Voltage						
High	V_{IH1}	3.5			V	All inputs except X_1. Use external pull-up.
	V_{IH2}	2.0			V	X_1 input.
Low	V_{IL}			0.8	V	All inputs.
Input Leakage				±10	µA	All pins.
Pull-up current		-200		-800	µA	XD0 - XD7.

T-52-33-27

TABLE 15

SYMBOL	R/W DS MODE		RD WR MODE		UNITS	COMMENTS
	MIN	MAX	MIN	MAX		
T1	45		45		ns	ALE (AS) active pulse width
T2	30		30		ns	Address setup to ALE inactive
T3	15		15		ns	Address hold from ALE inactive
T4	120		120		ns	Read Strobe low pulse width
T5		70		115	ns	RD (DS) active to read data valid
T6	10		10		ns	Read Data hold from RD (DS) high
T7	110		110		ns	Write Strobe low pulse width
T8	135		135		ns	Write Data valid to WR (DS) inactive
T9	25		25		ns	Write Data hold from WR (DS) inactive
T10	20		20		ns	ALE (AS) inactive to Read Strobe active
T11	20		20		ns	ALE (AS) inactive to Write Strobe active
T12	0		0		ns	RD (DS) inactive to ALE active
T13	0		0		ns	WR (DS) inactive to ALE active
T14		0		0	ns	CE valid to RD, WR or DS
T15	0				ns	R/W valid to AS inactive

TABLE 16

Parameter	Min	Max
t1 DREQ pulse width	1 clock - 15ns	1 clock + 15ns.
t2 DREQ inactive time	1 clock - 15ns	1 clock + 15ns for consecutive pulses. DC for non-consecutive pulses.
t3 DREQ period	2 clocks	2 clocks for consecutive pulses (typical 5MHz). DC for non-consecutive pulses.
t4 DACK Pulse width	50ns	DC This is a Function of the external device.
t5 DACK inactive time	50ns	DC This is a Function of the external device.
t6 DACK period	2 clocks	2 clocks for consecutive pulses (typical 5MHz). DC for non-consecutive pulses.

Since ACK is a function of an external device which may be asynchronous to the MSD95C00, there is no timing relationship between LE of DREQ and LE of DACK.

For 5 MByte/Sec SCSI transfer rates a 20MHz external crystal or TTL clock is required. The external clock is internally divided by 2. The term 'clock' above refers to the internal clock period (typical 10MHz).

SCSI Bus Timing

All timing related to the SCSI bus signals meet the SCSI bus timing requirements defined in the ANSI X3.131 - 1986 specification.

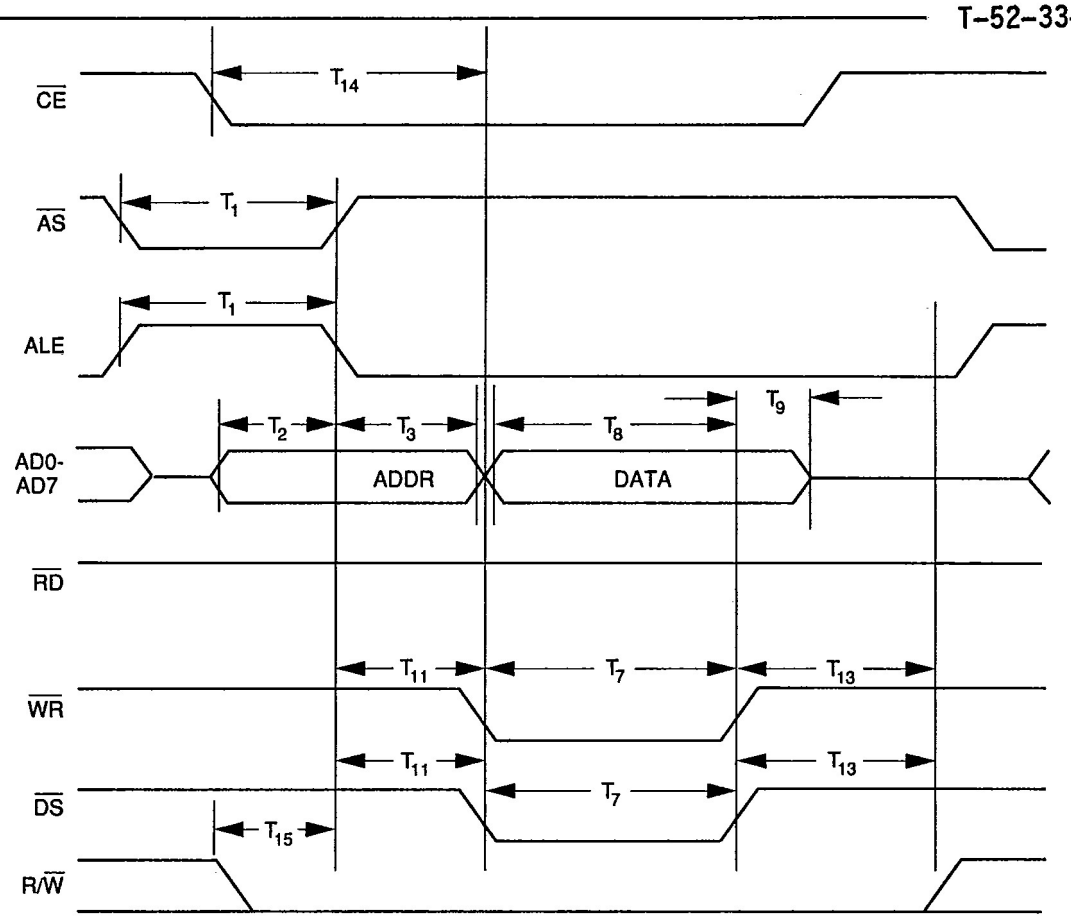


FIGURE 4: MICROPROCESSOR INTERFACE TIMING (WRITE)

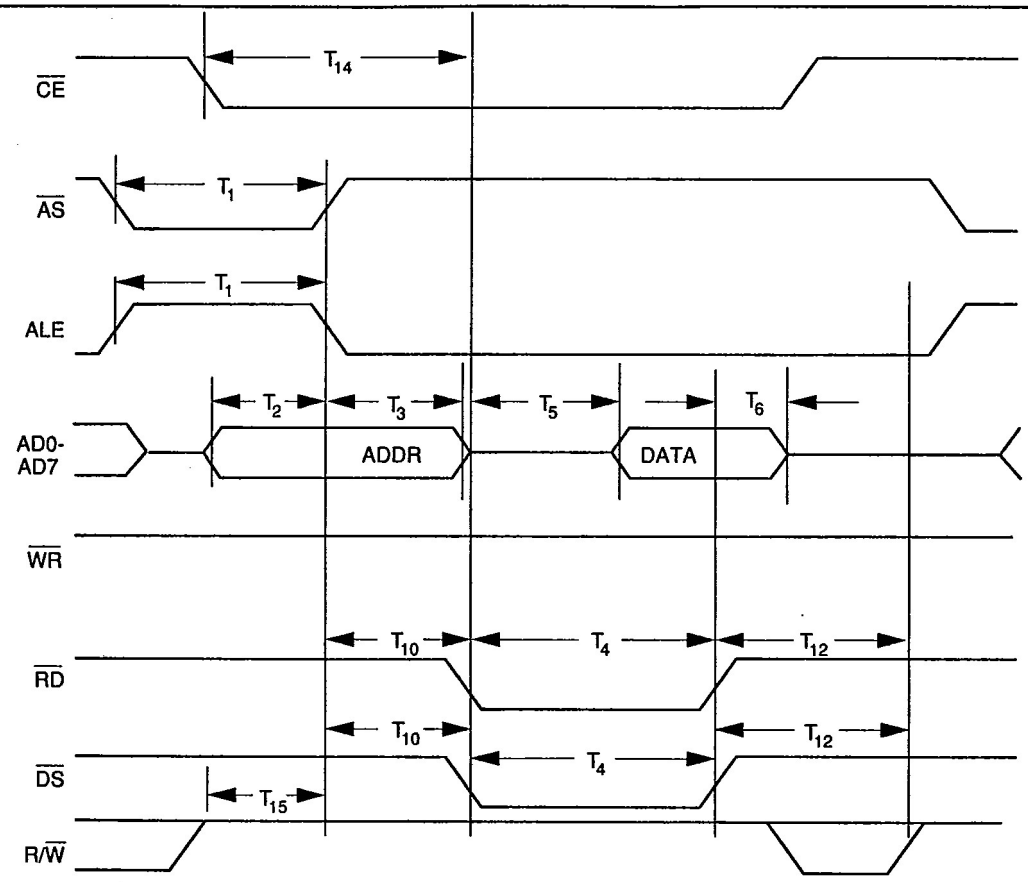
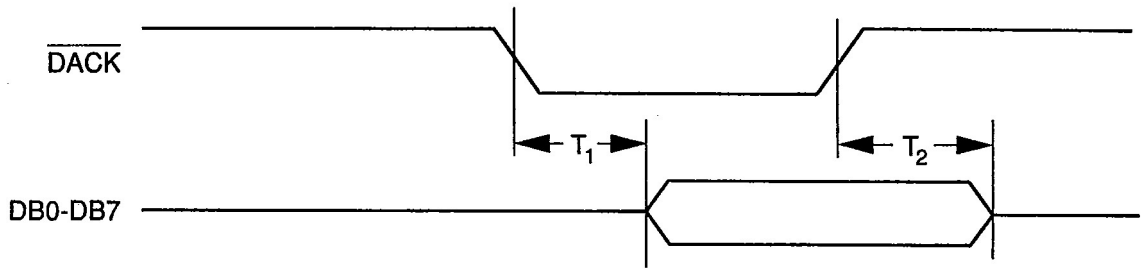


FIGURE 5: MICROPROCESSOR INTERFACE TIMING (READ)

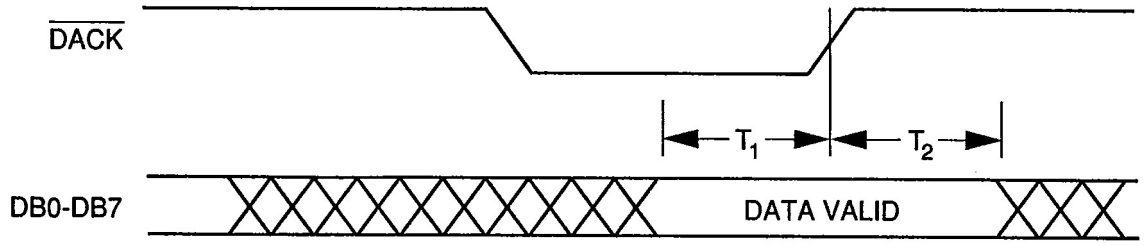
Refer to Table 14 for timing.

T-52-33-27



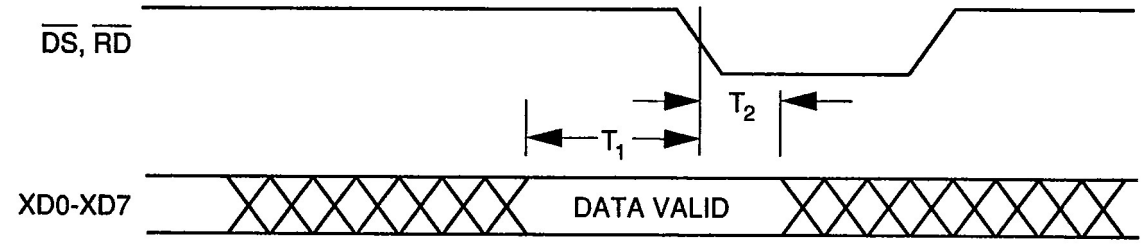
SYMBOL	MIN	MAX	UNITS	COMMENTS
T1		35	ns	LE DACK TO DATA VALID
T2	10	25	ns	TE DACK TO DATA INVALID

FIGURE 6: MSD95C00 DMA WRITE CYCLE



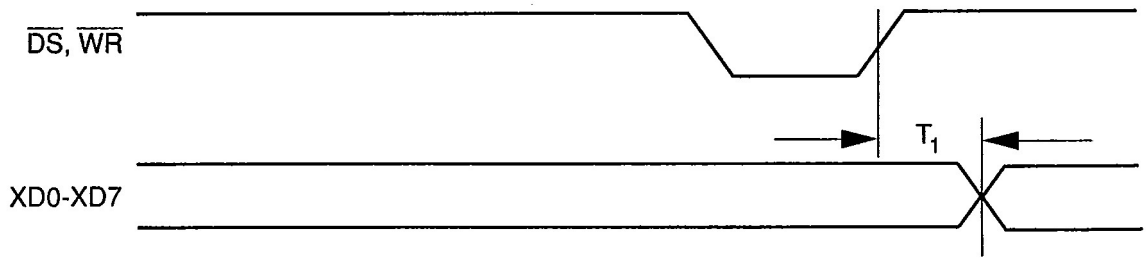
SYMBOL	MIN	MAX	UNITS	COMMENTS
T1	40		ns	DATA SETUP TIME
T2	10		ns	DATA HOLD TIME

FIGURE 7: MSD95C00 DMA READ CYCLE



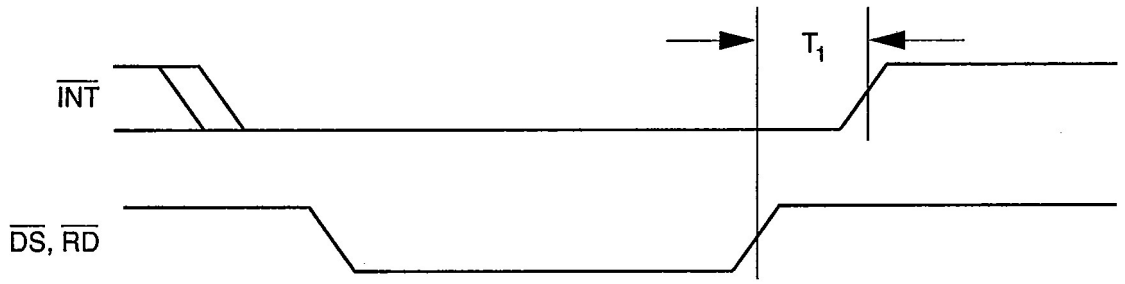
SYMBOL	MIN	MAX	UNITS	COMMENTS
T1	50		ns	DATA SETUP
T2	10		ns	DATA HOLD

FIGURE 8: MSD95C00 MPU READ PORT TIMING



SYMBOL	MIN	MAX	UNITS	COMMENTS
T1		50	ns	TE WR TO DATA VALID

FIGURE 9: MSD95C00 MPU WRITE PORT TIMING



SYMBOL	MIN	MAX	UNITS	COMMENTS
T1		50	ns	TE RD or DS to INTERRUPT INACTIVE

FIGURE 10: MSD95C00 INTERRUPT TIMING

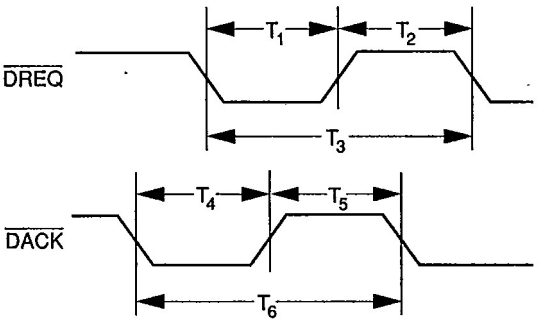
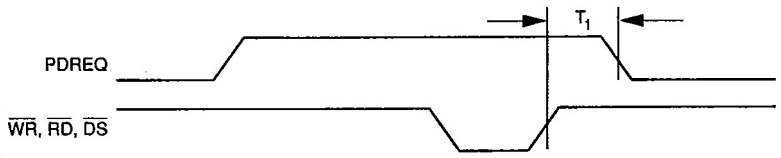


FIGURE 11: MSD95C00 DREQ, DACK



SYMBOL	MIN	MAX	UNITS	COMMENTS
T1	30	1 Clock + 30 ns	ns	TE WR, RD, DS to TE PDREQ

FIGURE 12: MSD95C00 PDREQ TIMING

Refer to Table 15 for DREQ and DACK timing.

FOR FURTHER INFORMATION ON PROGRAMMING OR USE OF THIS DEVICE, PLEASE CONTACT YOUR LOCAL SMC FIELD APPLICATION ENGINEER OR CONTACT FACTORY.

STANDARD MICROSYSTEMS CORPORATION
35 Marcus Blvd. Hauppauge, N.Y. 11788
(516) 273-3100 • FAX 516-231-6004