TMS4C1050B
262 264-WORD BY 4-BIT FIELD MEMORY

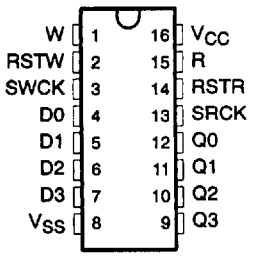
SMGS050E–JANUARY 1988–REVISED DECEMBER 1992

- **Organization . . . 262 264 × 4**
- **Single 5-V Power Supply (± 10% Tolerance)**
- **Fast FIFO (First-In First-Out) Operation**
  - **Full Word Continuous Read/Write**
  - **Asynchronous Read/Write**
- **Fully-Static (Refresh Free)**
- **High-Speed Read/Write Operation**

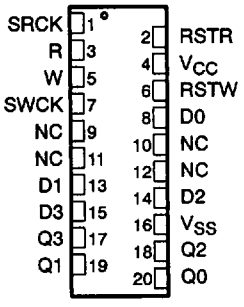
	ACCESS TIME (MAX)	CYCLE TIME READ (MIN)	CYCLE TIME WRITE (MIN)
TMS4C1050B-30	25 ns	30 ns	30 ns
TMS4C1050B-40	30 ns	40 ns	40 ns
TMS4C1050B-60	50 ns	60 ns	60 ns

- **Low Power Dissipation (Average I_{DD} = 50 mA at Minimum Cycle)**
- **Plastic 16-Pin 300-mil-Wide DIP, 20-Pin 400-mil ZIP, or 20/26-Lead Surface-Mount (SOJ) Package**
- **Texas Instruments EPIC™ (Enhanced Performance Implanted CMOS) Technology**
- **Operating Free-Air Temperature 0°C to 70°C**
- **Fully Compatible With TMS4C1050**

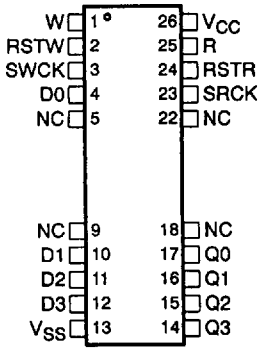
N PACKAGE†
(TOP VIEW)



SD PACKAGE†
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



† The packages are shown for pinout reference only.

PIN NOMENCLATURE	
D0–D3	Data-In
Q0–Q3	Data-Out
R	Read Enable
RSTR	Reset Read
RSTW	Reset Write
SRCK	Serial Read Clock
SWCK	Serial Write Clock
W	Write Enable
NC	No Internal Connection
V_{CC}	5-V Power Supply
V_{SS}	Ground

description

The TMS4C1050B is a Field Memory (FMEM) which reads and writes data exclusively through serial ports, 4 bits wide. Maximum storage capacity is 262 264 words by four bits each. Addressing is controlled by write address and read address pointers which must be reset to zero before memory access begins.

Read and write access may occur asynchronously. When read access is delayed relative to write access, the TMS4C1050B functions like a First-In First-Out (FIFO) register. The amount of delay determines the length of the FIFO register.

Unlike a conventional FIFO register, data may be read as many times as desired after it is written into the storage array.

Minimum delay between writing into the device and reading out data is 600 SWCK cycles. Maximum delay is one full field (262 264 write cycles).

The TMS4C1050B employs state-of-the-art EPIC™ (Enhanced Performance Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

EPIC is a trademark of Texas Instruments Incorporated.

description (continued)

To achieve high density, dynamic data storage cells are employed as the main data memory . Self-refresh and arbitration logic are implemented in the TMS4C1050B, supplying a refresh-free system. This logic prevents any conflict between data-saving/data-loading/memory-refresh requests.

If the memory is to be used as a delay element only, it is not necessary to reset the address pointers. After the memory has been completely filled and the write address pointer reaches its maximum value, it will wrap around again to the first address of the main array (address 120). The read address pointer behaves in the same manner.

The TMS4C1050B is offered in a 16-pin dual-in-line plastic package (N suffix) designed for insertion in mounting hole rows on 7,62-mm (300-mil) centers. This device is also offered in a 20-pin 400-mil ZIP package (SD suffix) and a 300-mil 20/26 J-lead plastic surface mount SOJ package (DJ suffix). The SOJ package is still in development, and the ADVANCE INFORMATION notice in this data sheet applies to this package. The TMS4C1050B is characterized for operation from 0°C to 70°C.

operation

write operation

The write operation is controlled by W and two clocks, SWCK and RSTW. It is accomplished by cycling SWCK and holding W high after the write address pointer reset operation (RSTW). Each write operation, beginning with RSTW, must contain at least 120 active write cycles (SWCK cycles while W is high). To transfer the last data written into the device (which at that time is still stored in the write line buffer) to the memory array, an RSTW operation is required after the last SWCK cycle.

reset write (RSTW)

The first positive transition of SWCK after RSTW going high, resets the write address pointers to zero. RSTW setup and hold times are referenced to the rising edge of SWCK. The state of W may be high or low during any reset operation. Before RSTW may be brought high again for a further reset operation, it must have been low for at least two SWCK cycles.

data inputs (D0-D3) and write clock (SWCK)

The SWCK input latches the data inputs on chip when W is high and also increments the internal write address pointer. Data-in setup and hold times ($t_{su(D)}$, $t_{h(D)}$) are referenced to the rising edge of SWCK.

write enable (W)

W is used as a data-in enable/disable. A logic high on the W input enables the input, and a logic low disables the input and holds the internal write address pointer.

Note that W setup and hold times are referenced to the rising edge of SWCK.

read operation

The read operation is controlled by R and two clocks, SRCK and RSTR. It is accomplished by cycling SRCK and holding R high after a read address pointer reset operation (RSTR). Each read operation, which begins with RSTR, must contain at least 120 active read cycles (SRCK cycles while R is high).

reset read (RSTR)

The first positive transition of SRCK after RSTR goes high resets the read address pointers to zero. RSTR setup and hold times are referenced to the rising edge of SRCK. The state of R may be high or low during any reset operation. Before RSTR may be brought high again for a further reset operation, it must have been low for at least two SRCK cycles.

data out (Q0-Q3) and read clock (SRCK)

Data is shifted out of the data registers on the rising edge of SRCK when R is high during a read operation. The SRCK input increments the internal read address pointer when R is high.

The three-state output buffer provides direct TTL compatibility (no pullup resistor required). Data out is the same polarity as data in. The output becomes valid after the access time interval t_{AC} that begins with the positive transition of SRCK.

Output valid time [$t_{v(OUT)}$] is referenced to the rising edge of SRCK in the next cycle.

output enabling and disabling

When R changes state, the outputs will become enabled or disabled. However, SRCK must go low also, before a change of the state of R can be noticed at the outputs. The state of SRCK influences the outputs only during the first SRCK cycle following each change of state of R.

In order for the outputs to become enabled, R must go high and SRCK must go low. Enable time is determined by whichever transition (R going high or SRCK going low) occurs last. In order for the outputs to become disabled, R must go low and SRCK must go low. Disable time is determined by whichever transition (R going low or SRCK going low) occurs last. See the timing diagrams under read cycle timing (output enable and disable) for an illustration of enable and disable timing.

read enable (R)

R performs a double function. First, R gates the SRCK clock for incrementing the read pointer. When R is high before the rising edge of SRCK, the read pointer is incremented. When R is low, the read pointer is not incremented. R setup times ($t_{su(RH)}$ and $t_{su(RL)}$ and R hold times [$t_{h(R)}$] are referenced to the rising edge of the SRCK clock.

The second function of R is to enable and disable the outputs. See the appropriate section on output enabling and disabling.

power up and initialization

When powering up, the device is designed to begin proper operation after at least 100 µs after V_{CC} has stabilized to a value within the range of recommended operating conditions. This time is defined as $t_{POWER\text{-}OK}$. While it is acceptable to start the initialization sequence during V_{CC} ramp-up (before $t_{POWER\text{-}OK}$), the full sequence must be repeated at least once after $t_{POWER\text{-}OK}$. The required initialization sequence for the write pointers is as follows:

At least one SWCK clock cycle, followed by a reset write operation, followed by at least 130 dummy write operations with W at high level, followed by another reset write operation. All timing parameters must be within specifications for the initialization sequence. After initialization, the write address pointers are set to zero, and writing may begin.

The initialization sequence for the read pointers is analogous to write pointer initialization, and must be performed at least once after $t_{POWER\text{-}OK}$.

old/new data access

There must be a minimum delay of 600 SWCK cycles between writing into memory and reading out from memory. If reading from the first field starts with an RSTR operation, before the start of writing the second field, (before the next RSTW operation), then the data just written in will be read out.

The start of reading out the first field of data may be delayed past the beginning of writing in the second field of data for as many as 119 SWCK cycles. If the RSTR operation for the first field read-out occurs less than 120 SWCK cycles after the RSTW operation for the second field write-in, then the internal buffering of the device assures that the first field will still be read out. The first field of data that is read out while the second field of data is written is called old data.

In order to read out new data, i.e., the second field written in, the delay between an RSTW operation and an RSTR operation must be at least 600 SRCK cycles. If the delay between RSTW and RSTR operations is more than 120 but less than 600 cycles, then the data read out will be undetermined. It may be old data or new data or a combination of old and new data. Such a timing should be avoided.

internal operation

writing into memory

The first 120 words of data following the initial RSTW operation after power-up are written into a cache buffer (A) initially, and will never be stored elsewhere, to allow read-out of data later without the delay involved in retrieving it from the main memory array.

Starting from address 120, data is written into the write line buffer, top block, until this block (256 words long) is full. Further writing then occurs to the bottom block of the write line buffer, while the top block is transferred to the main memory array. By the time the bottom block is full, the top block has been transferred to memory and can be used again to receive new incoming data. The channeling of input data into the top or bottom block is controlled internally by the device and is transparent to the user.

After the 120-word long cache buffer has been filled with incoming data, the input line selector switches the connection of the input port over to the B line buffer to assure that the next field of data, which will arrive later after a subsequent RSTW operation, does not over write the content of the cache buffer. Each subsequent filling of the cache buffer toggles the connection of the input port between the A and the B line buffers with the 121st SWCK pulse. The A and B line buffers, as well as the input line selector, are static registers.

The connection of the output port will also be toggled between A and B line buffers by the 121st SWCK pulse, providing no read operation from a cache buffer is in progress at this time. The output port will always be connected to the line buffers opposite to the one connected to the input port. In case a read operation from a cache buffer is in progress when the 121st SWCK occurs, the toggling of the output port connection will be delayed until the cache buffer has been read out completely.

The requirement stated on page 2 that each write operation must contain at least 120 active SWCK cycles, exists in order to assure that the toggling of the input and output ports between the A line buffer and the B line buffer functions without errors as described above.

The serial write pointer stores the (column) address of the last input data word received, while the write counter stores the row address.

After the last word of a full write cycle has been latched in (with a positive transition of the SWCK clock), the write line buffer most likely will be partially filled without having been transferred to the main memory array. To assure that the information contained in the write line buffer is stored and cannot be lost, it is required that an RSTW operation be performed when write clocking has stopped.

In addition to transferring the partially filled write line buffer into the main memory array, this RSTW operation will also reset the write addresses (serial write pointer) to zero. Regardless of how much later a new write cycle starts, it is not necessary to perform another RSTW operation again at that time.

reading from memory

After an RSTR operation, data from the main memory array (starting at address 120) will be transferred to a read line buffer. Because this transfer requires some time, the first 120 words will be read out of the A or B line buffers, where they had been previously stored (see writing into memory above).

If the first RSTR operation occurs after the first RSTW operation but before the second RSTW operation, read access will be to the same buffer that data had been written into during the first write cycle. Thus old data will be read out.

If the first RSTR operation occurs after the second RSTW operation, i.e. after the writing in of new data has already started, then the delay between the second RSTW and the first RSTR operation determines whether old data or new data will be read out.

If this delay is less than 120 SWCK cycles, data will be read out from the line buffer that was written into during the previous write cycle; i.e., old data will be read out. A delay of less than 120 SWCK cycles also assures that all following data bits are old data, because replacement of old data by new data in the main memory array will occur later than the respective read access to each address in the array.

If this delay is more than 600 SWCK cycles, data will be read out from the line buffer that it was written into during the current write cycle; i.e., new data will be read out. A delay of more than 600 SWCK cycles also assures that all following data bits are new data, because replacement of old data by new data in the main memory array will occur before the respective read access to each address in the array.

If this delay is more than 120 words, words, but less than 600 SWCK cycles, data read out can be either old or new or a mixture of old and new data, because it cannot be predicted accurately whether a word accessed for reading has already been replaced by new data or not. Such a situation should be avoided.

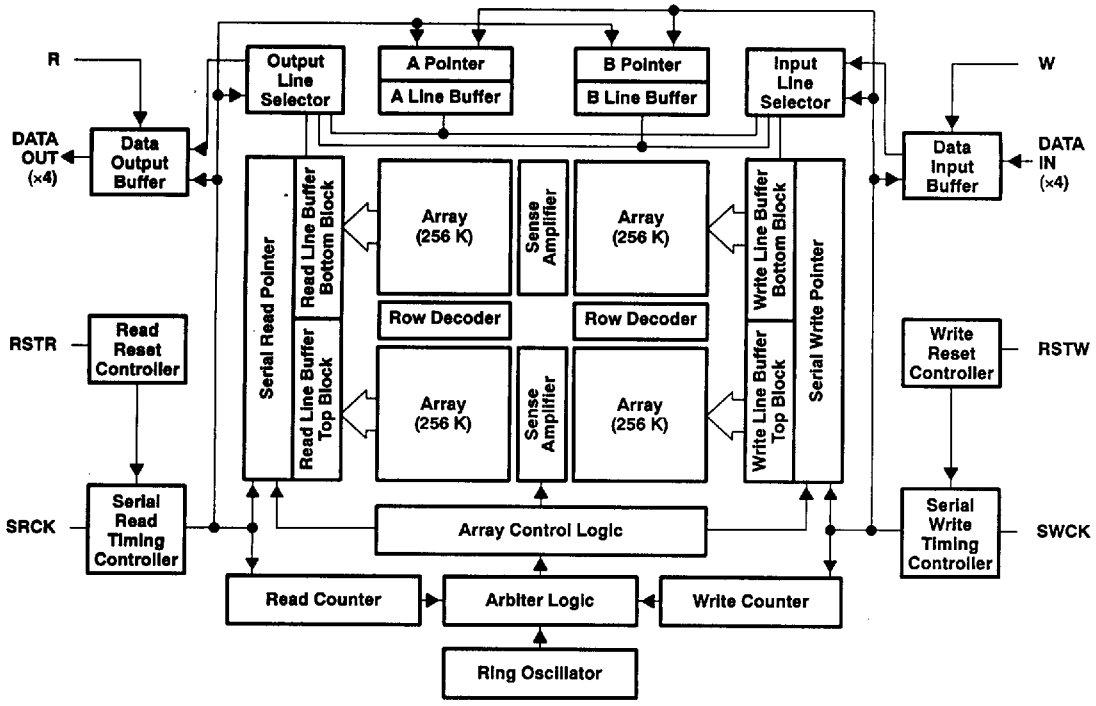
After the first 120 words are read out of the A or B line buffer, read transfer from the main memory array to the read line buffer is finished, and subsequent reading will occur from this buffer. Similar to the write operation, while one half of this buffer is being read out, the other half will be filled again by a new read transfer from the main memory array.

The serial read pointer stores the (column) address of the last data word read out, while the read counter stores the row address.

self-refresh and arbitration logic

The self-refresh and arbitration logic will keep the main memory information refreshed automatically without requiring any user action, control the address pointers for both read and write, and control the flow of information both into and out of the main memory.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range on any pin (see Note 1)	−1 V to 7 V
Supply voltage range on V_{CC}	0 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the "recommended operating conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2.4		$V_{CC}+1$	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: V_{IL} = − 1.5 V undershoot is allowed when device is operated in the range of recommended supply voltage.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	'4C1050B-30		'4C1050B-40		'4C1050B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = − 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 to 6.5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	µA
I_O	Output current (leakage)	V_{CC} = 5.5 V, V_O = 0 to V_{CC}, R low		±10		±10		±10	µA
I_{DD1}	Average operating current	Minimum write/read cycle, output open		50		45		35	mA
I_{DD2}	Standby current	After 1 RSTW/RSTR cycle, W and R low		10		10		10	mA

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz†

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_i	Input capacitance	V_I = 0, f = 1 MHz			7	pF
C_o	Output capacitance	V_I = 0, f = 1 MHz			10	pF

† V_{CC} equal to 5 V ± 0.5 V and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	'4C1050B-30		'4C1050B-40		'4C1050B-60		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AC}	Access time from SRCK high	(see Note 3)		25		30		50	ns
$t_{v(OUT)}$	Output valid time after SRCK high	(see Note 3)	6		6		6		ns
$t_{dis(CK)}$	Output disable time after SRCK low	(see Note 4)	4	15	4	15	4	15	ns
$t_{en(CK)}$	Output enable time after SRCK low	(see Note 3)	0	15	0	15	0	15	ns
$t_{en(RH)}$	Output enable time after R high	(see Note 3)	0	15	0	15	0	15	ns
$t_{dis(RL)}$	Output disable time after R low	(see Note 4)	4	15	4	15	4	15	ns

NOTES: 3. The load connected to each output is a 50-pF capacitor to ground, in parallel with a 218-Ω resistor to 1.31 V as illustrated by Figure 1.

4. Disable times are specified from the initiating timing edge until the output is no longer driven by the memory. If disable times are to be measured by observing output voltage waveforms, sufficiently low load resistors and capacitors have to be used, and the RC time constants of the load have to be taken into account.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 5)

		'4C1050B-30		'4C1050B-40		'4C1050B-60		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Write cycle time (see Note 6)	30		40		60		ns
$t_{c(R)}$	Read cycle time (see Note 6)	30		40		60		ns
$t_{w(R)}$	Pulse duration, R low	10		10		10		ns
$t_{w(W)}$	Pulse duration, W low	10		10		10		ns
$t_{w(RH)}$	Pulse duration, SRCK high	12		17		20		ns
$t_{w(RL)}$	Pulse duration, SRCK low	12		17		20		ns
$t_{w(WH)}$	Pulse duration, SWCK high	12		17		20		ns
$t_{w(WL)}$	Pulse duration, SWCK low	12		17		20		ns
$t_{su(D)}$	Data setup time before SWCK high	5		5		5		ns
$t_{su(RH)}$	R-high setup time before SRCK high	0		0		0		ns
$t_{su(RL)}$	R-low setup time before SRCK high	0		0		0		ns
$t_{su(WH)}$	W-high setup time before SWCK high	0		0		0		ns
$t_{su(WL)}$	W-low setup time before SWCK high	0		0		0		ns
$t_{su(RSTR)}$	RSTR setup time before SRCK high	3		3		3		ns
$t_{su(RSTW)}$	RSTW setup time before SWCK high	3		3		3		ns
$t_{h(D)}$	Data hold time after SWCK high	6		6		6		ns
$t_{h(R)}$	R-hold time after SRCK high	6		6		6		ns
$t_{h(W)}$	W-hold time after SWCK high	6		6		6		ns
$t_{h(RSTR)}$	RSTR hold time after SRCK high	6		6		6		ns
$t_{h(RSTW)}$	RSTW hold time after SWCK high	6		6		6		ns
t_T	Transition time	3	30	3	30	3	30	ns

NOTES: 5. Timing measurements are referenced to V_{IH} (MIN) = 2.4 V and V_{IL} (MAX) = 0.8 V. t_T is measured between V_{IH} (MIN) and V_{IL} (MAX).
6. All cycle times assume t_T = 3 ns.

PARAMETER MEASUREMENT INFORMATION

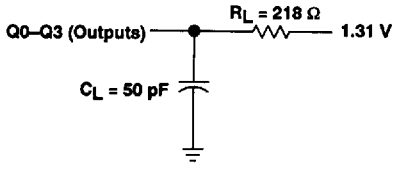


Figure 1. Load Circuit for Timing Parameters

TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77001

PARAMETER MEASUREMENT INFORMATION

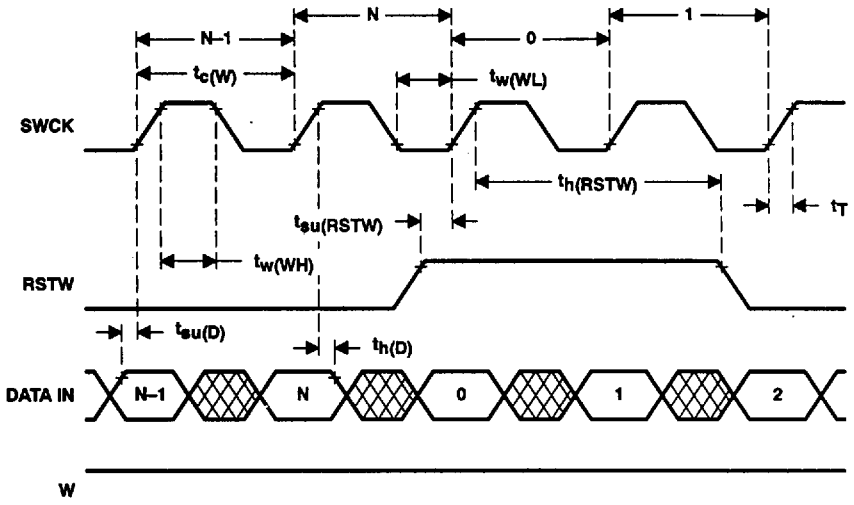


Figure 2. Write Cycle Timing (Reset Write)

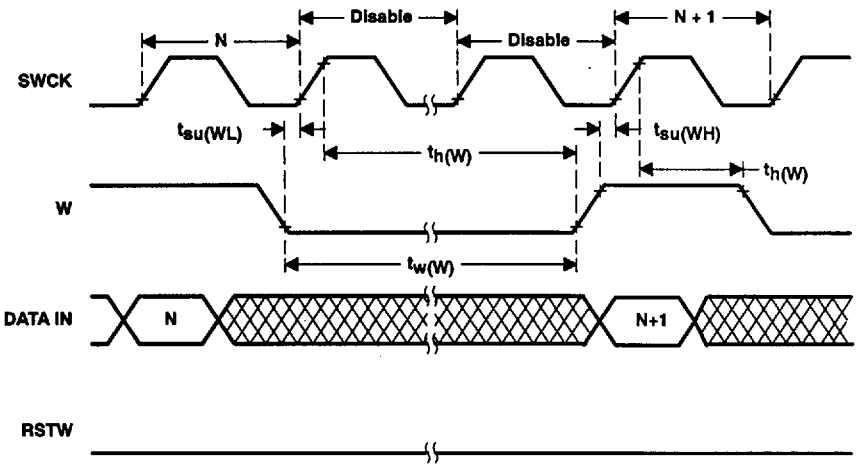


Figure 3. Write Cycle Timing (Write Enable)

PARAMETER MEASUREMENT INFORMATION

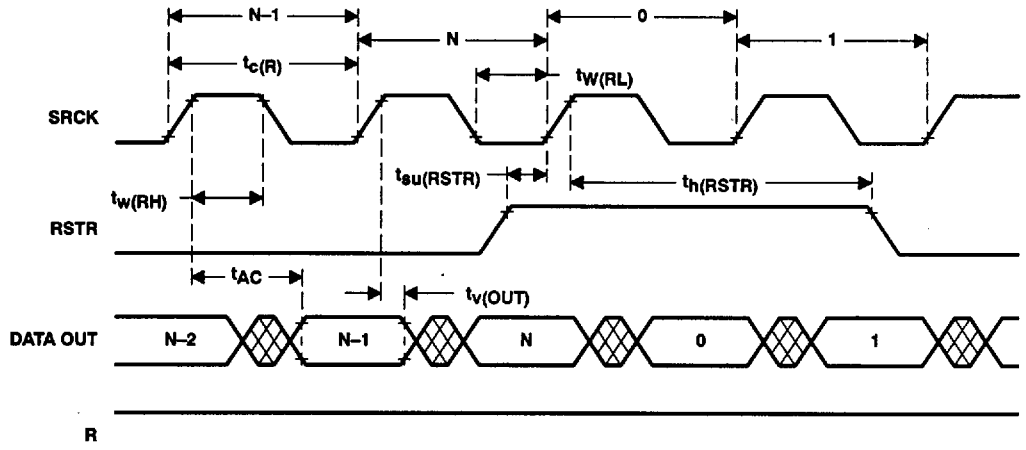


Figure 4. Read Cycle Timing (Reset Read)

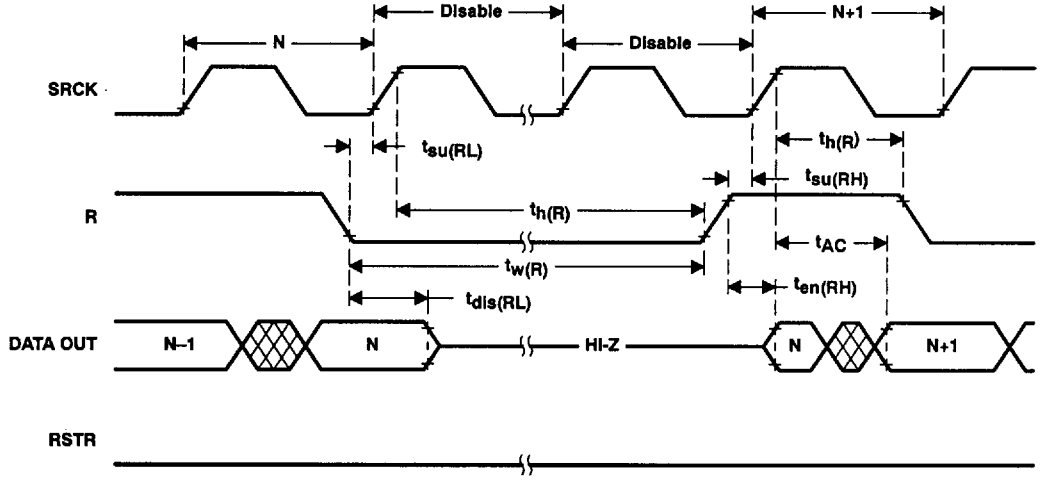


Figure 5. Read Cycle Timing (Read Enable)

PARAMETER MEASUREMENT INFORMATION

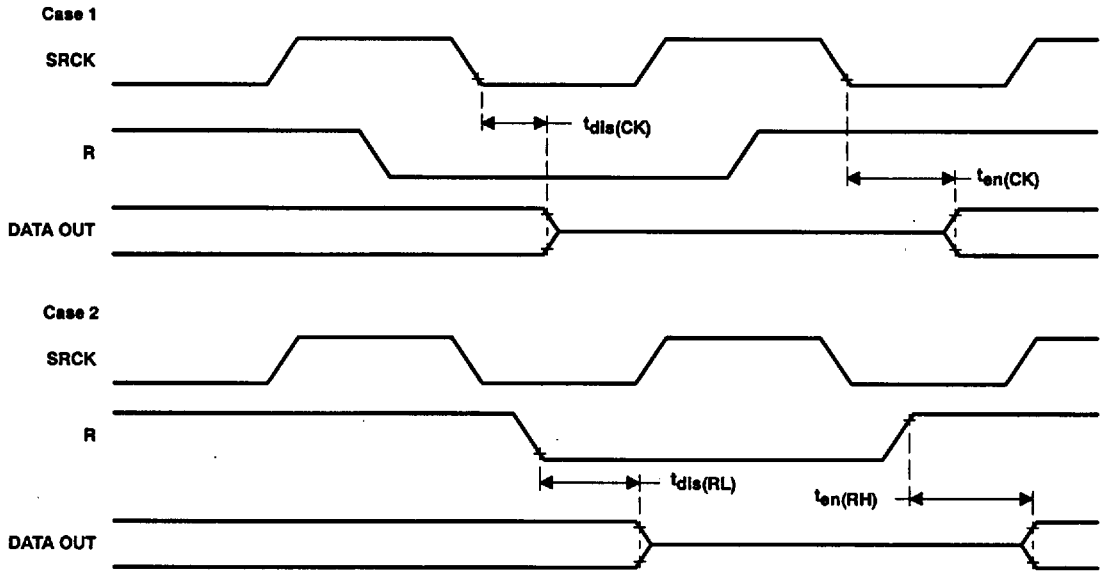


Figure 6. Read Cycle Timing (Output Enable and Disable)

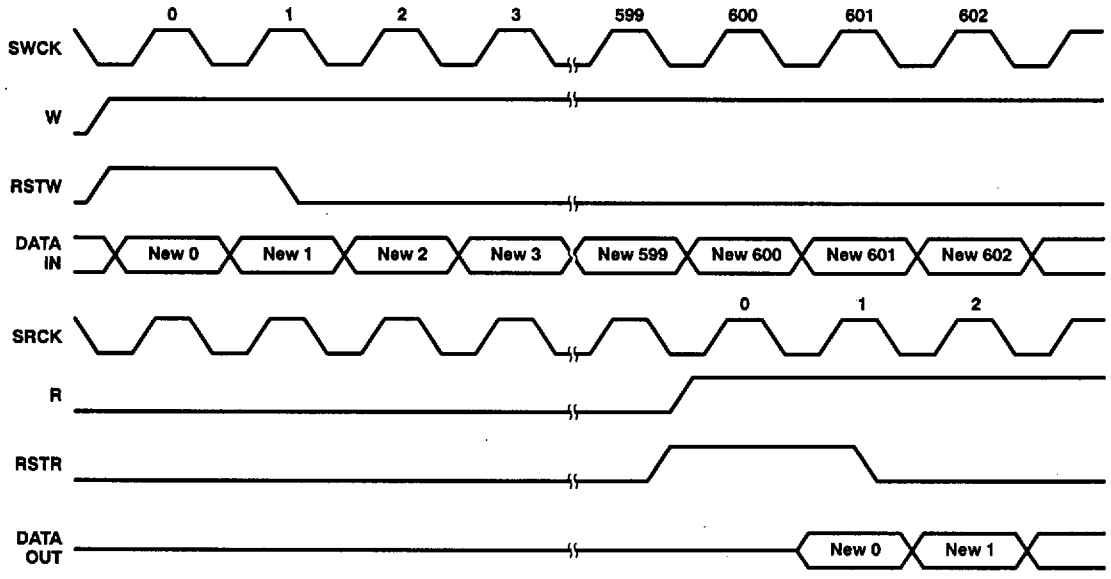


Figure 7. New Data Access Mode

PARAMETER MEASUREMENT INFORMATION

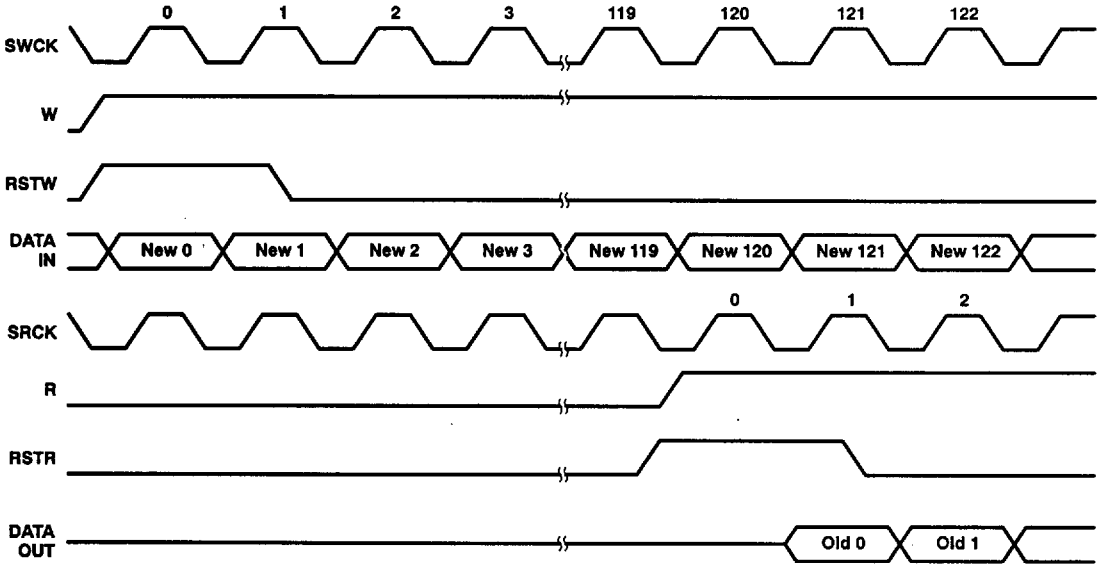


Figure 8. Old Data Access Mode