16-Bit, Isolated, Sigma-Delta Modulator

Data Sheet

ADuM7704

FEATURES

- 5 MHz to 21 MHz master clock input frequency
- Offset drift vs. temperature: ±0.25 µV/°C maximum
- SNR: 82 dB typical
- 16 bits, no missing codes
- Full-scale analog input voltage range: ±64 mV
- ENOB: 13 bits typical
- I_{DD1}: 10 mA maximum
- On-board digital isolator
- Operating temperature range
  - −40°C to +125°C (16-lead SOIC_W)
  - −40°C to +105°C (8-lead SOIC_IC)
- High isolation common-mode transient immunity:
  - 150 kV/µs minimum, V_{DD2} = 3.3 V
- Wide-body SOICs
  - 16-lead SOIC_W
  - 8-lead SOIC_IC with increased creepage
- Safety and regulatory approvals
  - UL recognition
    - 5700 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE Certificate of Conformity
    - DIN V VDE V 0884-10: V_{IORM} = 1270 V_{PEAK}
    - DIN V VDE V 0884-11: V_{IORM} = 1060 V_{PEAK} (pending)

APPLICATIONS

- Shunt current monitoring
- AC motor controls
- Power and solar inverters
- Wind turbine inverters
- Analog-to-digital and optoisolator replacement

FUNCTIONAL BLOCK DIAGRAM

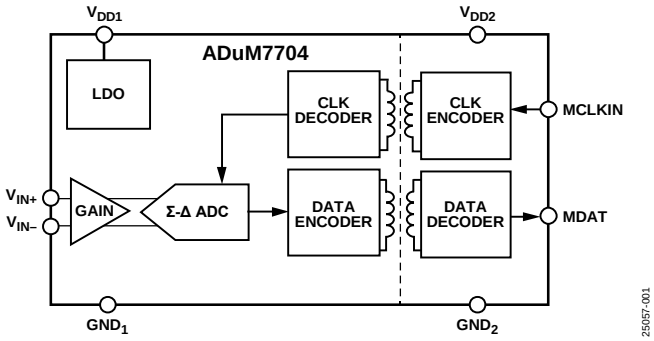

Figure 1.

GENERAL DESCRIPTION

The ADuM7704 is a high performance, second-order, Σ-Δ modulator that converts an analog input signal into a high speed, single-bit data stream, with on-chip digital isolation based on Analog Devices, Inc., *i*Coupler® technology. The device operates from a 4.5 V to 20 V power supply range (V_{DD1}) and accepts a pseudo differential input signal of ±50 mV (±64 mV full-scale). The pseudo differential input is ideally suited to shunt voltage monitoring in high voltage applications where galvanic isolation is required.

The analog input is continuously sampled by a high performance analog modulator and converted to a ones density digital output stream with a data rate of up to 21 MHz. The original information can be reconstructed with an appropriate sinc3 digital filter to achieve an 82 dB signal-to-noise ratio (SNR) at 78.1 kSPS with a 256 decimation rate and a 20 MHz master clock. The serial input and output operates from a 5 V or a 3.3 V supply (V_{DD2}).

The serial interface is digitally isolated. High speed complementary metal-oxide semiconductor (CMOS) technology, combined with monolithic transformer technology, results in the on-chip isolation providing outstanding performance characteristics, superior to alternatives such as optocoupler devices. The ADuM7704 is available in a 16-lead, wide-body SOIC_W with an operating temperature range of −40°C to +125°C and an 8-lead, wide-body SOIC_IC with an operating temperature range of −40°C to +105°C.

Rev. 0 Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support www.analog.com

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REVISION HISTORY

8/2020—Revision 0: Initial Version

SPECIFICATIONS

V_{DD1} = 4.5 V to 20 V, V_{DD2} = 3 V to 5.5 V, V_{IN+} = −50 mV to +50 mV, V_{IN-} = 0 V, T_A = −40°C to +125°C (16-lead SOIC_W), T_A = −40°C to +105°C (8-lead SOIC_IC), MCLKIN frequency (f_{MCLKIN}) = 20 MHz, tested with a sinc3 filter, and a 256 decimation rate, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	Filter output truncated to 16 bits
Integral Nonlinearity (INL)[1]		±2	±8	LSB	
Differential Nonlinearity (DNL)[1]			±0.99	LSB	Guaranteed no missed codes to 16 bits
Offset Error[1]		±0.05	±0.13	mV	Initial at T_A = 25°C
		±0.1	±0.18	mV	
Offset Drift vs. Temperature[1]		±0.1	±0.25	µV/°C	16-lead SOIC_W
		±0.1	±0.6	µV/°C	8-lead SOIC_IC
Offset Drift vs. V_{DD1}		±2.5		µV/V	
Gain Error[1]			±0.2	% FSR	Initial at T_A = 25°C
Gain Error Drift vs. Temperature[1]		±15.6	±31.3	ppm/°C	
		±2	±4	µV/°C	
Gain Error Drift vs. V_{DD1}		±5		ppm/V	
ANALOG INPUT					
Input Voltage Range	−64		+64	mV	Full-scale range
	−50		+50	mV	For specified performance
Input Common-Mode Voltage Range		−0.2 to +0.8		V	
Dynamic Input Current		±1	±2	µA	V_{IN+} = ±50 mV, V_{IN-} = 0 V
		0.05		µA	V_{IN+} = 0 V, V_{IN-} = 0 V
DC Leakage Current		±0.01		µA	
Input Capacitance		25		pF	V_{IN+} or V_{IN-} left floating
DYNAMIC SPECIFICATIONS					V_{IN+} = 1 kHz
Signal-to-Noise-and-Distortion Ratio (SINAD)[1]	76.5	82		dB	
SNR[1]	78.6	82		dB	
Total Harmonic Distortion (THD)[1]	−78	−89		dB	
Peak Harmonic or Spurious-Free Dynamic Range Noise (SFDR)[1]		−97		dB	
Effective Number of Bits (ENOB)[1]	12.4	13		Bits	
ISOLATION COMMON-MODE TRANSIENT IMMUNITY (CMTI)[1]					Common-mode voltage ($\|V_{CM}\|$) = 2 kV
Static and Dynamic	75	150		kV/µs	V_{DD2} = 5.5 V
	150			kV/µs	V_{DD2} = 3.3 V
LOGIC INPUTS					CMOS with Schmitt trigger
Input High Voltage (V_{IH})	0.7 × V_{DD2}			V	
Input Low Voltage (V_{IL})			0.3 × V_{DD2}	V	
Input Current (I_{IN})			±0.6	µA	
Input Capacitance (C_{IN})		10		pF	
LOGIC OUTPUTS					
Output High Voltage (V_{OH})	V_{DD2} − 0.4	V_{DD2} − 0.2		V	Output current (I_{OUT}) = −4 mA
Output Low Voltage (V_{OL})		0.2	0.4	V	I_{OUT} = 4 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{IN+} > 64 mV
V_{DD1}	4.5	15	20	V	
V_{DD2}	3		5.5	V	
V_{DD1} Current (I_{DD1})		8.2	10	mA	
V_{DD2} Current (I_{DD2})		2	3	mA	
Power Dissipation		133	216.5	mW	V_{DD2} = 4.5 V to 5.5 V
		130	211	mW	V_{DD2} = 3 V to 3.6 V

[1] See the Terminology section.

TIMING SPECIFICATIONS

V_{DD1} = 4.5 V to 20 V, V_{DD2} = 3 V to 5.5 V, T_A = −40°C to +125°C (16-lead SOIC_W), and T_A = −40°C to +105°C (8-lead SOIC_IC), unless otherwise noted. Sample tested during initial release to ensure compliance. It is recommended to read the MDAT pin on the MCLKIN rising edge.

Table 2.

	Limit at T_{MIN}, T_{MAX}				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Description**
f_{MCLKIN}	5	20	21	MHz	Master clock input frequency
t_{MCLKIN}	48	50	200	ns	Master clock input period
t_1[1]			16	ns	Data access time after MCLKIN rising edge
t_2[1]	5			ns	Data hold time after MCLKIN rising edge
t_3	0.4 × t_{MCLKIN}			ns	Master clock low time
t_4	0.4 × t_{MCLKIN}			ns	Master clock high time

[1] Defined as the time required from an 80% MCLKIN input level to when the output crosses 0.5 × V_{DD2}, as outlined in Figure 2. Measured with a ±20 µA load and a 25 pF load capacitance.

Timing Diagram

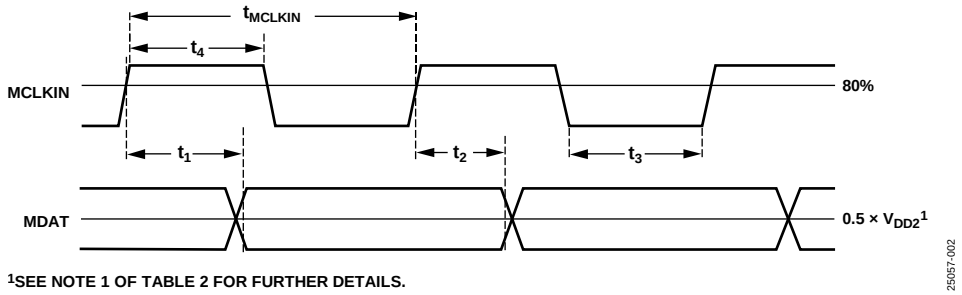


Figure 2. Data Timing Diagram

PACKAGE CHARACTERISTICS

Table 3.

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)	R_{I-O}		10^{12}		Ω	
Capacitance (Input to Output)	C_{I-O}		1		pF	Frequency = 1 MHz

[1] The device is considered a 2-terminal device. For the 16-lead SOIC_W, Pin 1 to Pin 8 are shorted together and Pin 9 to Pin 16 are shorted together. For the 8-lead SOIC_IC, Pin 1 to Pin 4 are shorted together and Pin 5 to Pin 8 are shorted together.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Input to Output Momentary Withstand Voltage	V_{ISO}	5700 min	V rms	1 minute duration
Minimum External Air Gap (Clearance)[1, 2]				
16-Lead SOIC_W	L(I01)	7.8 min	mm	Measured from input terminals to output terminals, shortest distance through air
8-Lead SOIC_IC	L(I01)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)[1]				
16-Lead SOIC_W	L(I02)	7.8 min	mm	Measured from input terminals to output terminals, shortest distance path along body
8-Lead SOIC_IC	L(I02)	8.3 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.041 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		I		Material Group (DIN VDE 0110, 1/89, Table I)

[1] In accordance with IEC 60950-1 guidelines for the measurement of creepage and clearance distances for a pollution degree of 2 and altitudes ≤ 2000 m.
[2] Consideration must be given to pad layout to ensure the minimum required distance for clearance is maintained.

REGULATORY INFORMATION

Table 5.

UL	CSA	VDE
Recognized under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10[2], reinforced insulation, V_{IORM} = 1270 V_{PEAK}, V_{IOSM} = 8000 V_{PEAK}
5700 V rms Isolation Voltage Single Protection	Basic insulation per CSA 60950-1-07 and IEC 60950-1, ADuM7704: 780 V rms (1102 V_{PEAK}), ADuM7704-8: 830 V rms (1173 V_{PEAK}) maximum working voltage[3]	
	Reinforced insulation per CSA 60950-1-07 and IEC 60950-1, ADuM7704: 390 V rms (551 V_{PEAK}), ADuM7704-8: 415 V rms (586 V_{PEAK}) maximum working voltage[3]	Certified according to DIN V VDE V 0884-11, reinforced insulation, V_{IORM} = 1060 V_{PEAK}, V_{IOSM} = 8000 V_{PEAK} (pending)
	Reinforced insulation per IEC 60601-1, 261 V rms (369 V_{PEAK}) maximum working voltage	

[1] In accordance with UL 1577, each ADuM7704 is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec (current leakage detection limit = 15 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM7704 is proof tested by applying an insulation test voltage ≥ 2344 V_{PEAK} for 1 sec (partial discharge detection limit = 5 pC).
[3] Rating is calculated for a pollution degree of 2 and a Material Group III. The ADuM7704 package material is rated by CSA to a comparative tracking index (CTI) of >600 V and, therefore, Material Group I.

DIN V VDE V 0884-10 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Table 6.

Description	Symbol	Characteristic	Unit
INSTALLATION CLASSIFICATION PER DIN VDE 0110			
For Rated Mains Voltage ≤300 V rms		I to IV	
For Rated Mains Voltage ≤450 V rms		I to IV	
For Rated Mains Voltage ≤600 V rms		I to IV	
CLIMATIC CLASSIFICATION		40/125/21	
POLLUTION DEGREE (DIN VDE 0110, TABLE 1)		2	
MAXIMUM WORKING INSULATION VOLTAGE	V_{IORM}	1270	V_{PEAK}
INPUT TO OUTPUT TEST VOLTAGE, METHOD B1			
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, t_m = 1 Second, Partial Discharge < 5 pC	$V_{PD(M)}$	2344	V_{PEAK}
INPUT TO OUTPUT TEST VOLTAGE, METHOD A	$V_{PR(M)}$		
After Environmental Test Subgroup 1			
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC		2032	V_{PEAK}
After Input and/or Safety Test Subgroup 2/Safety Test Subgroup 3			
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC		1524	V_{PEAK}
HIGHEST ALLOWABLE OVERVOLTAGE (TRANSIENT OVERVOLTAGE, t_{TR} = 10 sec)	V_{IOTM}	8000	V_{PEAK}
SURGE ISOLATION VOLTAGE			
1.2 µs Rise Time, 50 µs, 50% Fall Time	V_{IOSM}	8000	V_{PEAK}
SAFETY LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE)[1]			
Case Temperature	T_S	150	°C
Side 1 (P_{VDD1}) and Side 2 (P_{VDD2}) Power Dissipation	P_{SO}		
16-Lead SOIC_W		1.43	W
8-Lead SOIC_IC		1.19	W
INSULATION RESISTANCE AT T_S, VOLTAGE INPUT TO OUTPUT (V_{IO}) = 500 V	R_{IO}	$>10^9$	Ω

[1] See Figure 3.

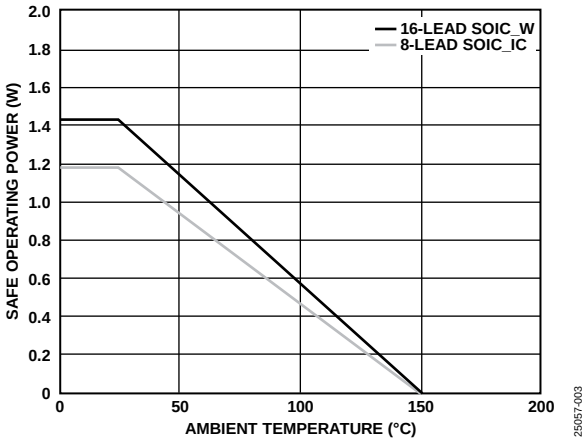


Figure 3. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-10

DIN V VDE V 0884-11 INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by means of protective circuits.

Table 7.

Description	Symbol	Characteristic	Unit
INSTALLATION CLASSIFICATION PER DIN VDE 0110			
For Rated Mains Voltage ≤300 V rms		I to IV	
For Rated Mains Voltage ≤450 V rms		I to IV	
For Rated Mains Voltage ≤600 V rms		I to IV	
CLIMATIC CLASSIFICATION		40/125/21	
POLLUTION DEGREE (DIN VDE 0110, TABLE 1)		2	
MAXIMUM WORKING INSULATION VOLTAGE	V_{IORM}	1060	V_{PEAK}
INPUT TO OUTPUT TEST VOLTAGE, METHOD B1			
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC	$V_{PD(M)}$	1987	V_{PEAK}
INPUT TO OUTPUT TEST VOLTAGE, METHOD A	$V_{PR(M)}$		
After Environmental Test Subgroup 1			
$V_{IORM} \times 1.6 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC		1696	V_{PEAK}
After Input and/or Safety Test Subgroup 2/Safety Test Subgroup 3			
$V_{IORM} \times 1.2 = V_{PR}$, t_m = 60 sec, Partial Discharge < 5 pC		1272	V_{PEAK}
HIGHEST ALLOWABLE OVERVOLTAGE (TRANSIENT OVERVOLTAGE, t_{TR} = 10 sec)	V_{IOTM}	8000	V_{PEAK}
SURGE ISOLATION VOLTAGE			
1.2 µs Rise Time, 50 µs, 50% Fall Time	V_{IOSM}	8000	V_{PEAK}
SAFETY LIMITING VALUES (MAXIMUM VALUE ALLOWED IN THE EVENT OF A FAILURE)[1]			
Case Temperature	T_S	150	°C
Side 1 (P_{VDD1}) and Side 2 (P_{VDD2}) Power Dissipation	P_{SO}		
16-Lead SOIC_W		1.43	W
8-Lead SOIC_IC		1.19	W
INSULATION RESISTANCE AT T_S, V_{IO} = 500 V	R_{IO}	$>10^9$	Ω

[1] See Figure 4.

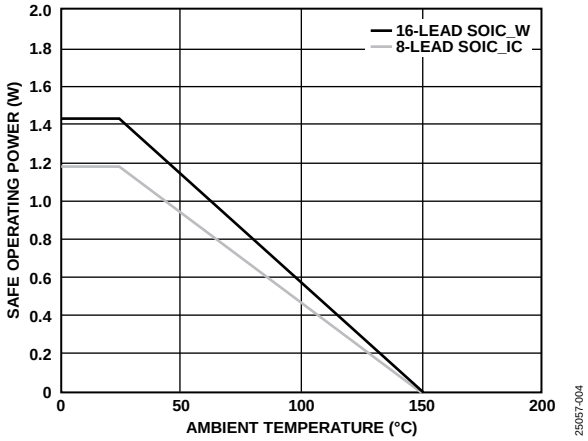


Figure 4. Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN V VDE V 0884-11

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective GND_x.

Table 8.

Parameter	Rating
V_{DD1} to GND_1	−0.3 V to +23 V
V_{DD2} to GND_2	−0.3 V to +6 V
Analog Input Voltage to GND_1	−1 V to +4.3 V
Digital Input Voltage to GND_2	−0.5 V to V_{DD2} + 0.5 V
Digital Output Voltage to GND_2	−0.5 V to V_{DD2} + 0.5 V
Input Current to Any Pin Except Supplies[1]	±10 mA
Output Current from Any Pin Except Supplies	±10 mA
Temperature	
Operating Range	−40°C to +125°C
Storage Range	−65°C to +150°C
Junction	150°C
Pb-Free, Soldering Reflow	260°C

[1] Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) to latch up.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 9. Thermal Resistance

Package Type[1]	θ_{JA}[2]	Unit
RI-8-1	105	°C/W
RW-16	87.25	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board. See JEDEC JESD-51.
[2] θ_{JA} was calculated using the total power and maximum junction temperature.

INSULATION RATINGS

The maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

Table 10. Maximum Continuous Working Voltage

Parameter	Insulation Rating[1]	Lifetime Conditions
Basic Insulation		
AC Voltage		
Bipolar Waveform	1129 V_{PEAK}	20 years to 1000 ppm failure at 1129 V_{PEAK} (798 V rms, 50 Hz/60 Hz sine wave)
Reinforced Insulation		
AC Voltage		
Bipolar Waveform	1060 V_{PEAK}	20 years to 1 ppm failure at 1060 V_{PEAK} (750 V rms, 50 Hz/60 Hz sine wave)

[1] Insulation capability without regard to creepage limitations. Working voltage may be limited by the PCB creepage when considering rms voltages for components soldered to a PCB (assumes Material Group I up to 1270 V rms), or package: RI-8-1 package creepage of 8.3 mm, and RW-16 package creepage of 7.8 mm, when considering rms voltages for Material Group I.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADuM7704

Table 11. ADuM7704, 16-Lead SOIC_W and 8-Lead SOIC_IC

ESD Model	Withstand Threshold (V)	Class
HBM[1]	±3500	3A
FICDM[2]	±1500	C4

[1] JESD22-C101, RC network, 1 Ω, and package capacitance.
[2] ESDA/JEDEC JS-001-2011, RC network: 1.5 kΩ and 100 pF.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

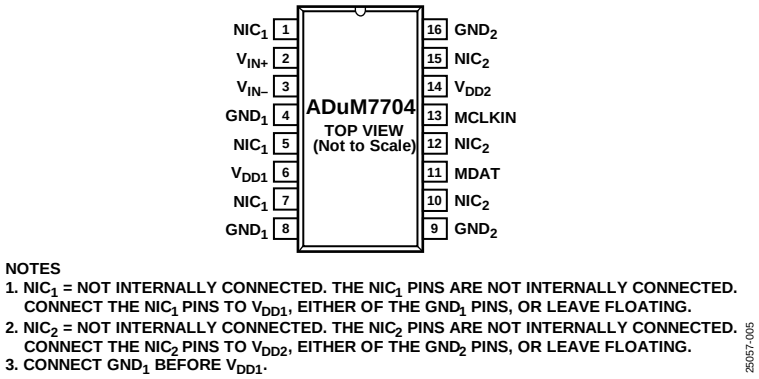


Figure 5. 16-Lead SOIC_W Pin Configuration

Table 12. 16-Lead SOIC_W Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 5, 7	NIC_1	Not Internally Connected. The NIC_1 pins are not internally connected. Connect the NIC_1 pins to V_{DD1}, either of the GND_1 pins, or leave floating.
2	V_{IN+}	Positive Analog Input.
3	V_{IN-}	Negative Analog Input.
4, 8	GND_1	Ground 1. The GND_1 pins are the ground reference point for all circuitry on the isolated side.
6	V_{DD1}	Supply Voltage, 4.5 V to 20 V. V_{DD1} is the supply voltage for the isolated side of the ADuM7704 and is relative to the GND_1 pins. For device operation, connect the supply voltage to NIC_1 (Pin 7). Decouple the supply pin to either of the GND_1 pins with a 10 µF capacitor in parallel with a 100 nF capacitor as close to the pin as possible.
9, 16	GND_2	Ground 2. The GND_2 pins are the ground reference point for all circuitry on the nonisolated side.
10, 12, 15	NIC_2	Not Internally Connected. The NIC_2 pins are not internally connected. Connect the NIC_2 pins to V_{DD2}, either of the GND_2 pins, or leave floating.
11	MDAT	Serial Data Output. The single-bit modulator output is supplied to MDAT as a serial data stream. MDAT is clocked out on the rising edge of the MCLKIN input and is valid on the following MCLKIN rising edge.
13	MCLKIN	Master Clock Logic Input. 5 MHz to 21 MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN.
14	V_{DD2}	Supply Voltage, 3 V to 5.5 V. V_{DD2} is the supply voltage for the nonisolated side and is relative to the GND_2 pins. Decouple this supply to either of the GND_2 pins with a 10 µF capacitor in parallel with a 100 nF capacitor as close to the pin as possible.

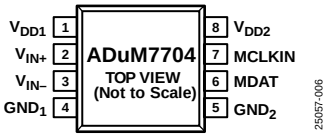


Figure 6. 8-Lead SOIC_IC Pin Configuration

Table 13. 8-Lead SOIC_IC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage, 4.5 V to 20 V. V_{DD1} is the supply voltage for the isolated side of the ADuM7704 and is relative to GND_1. For device operation, connect the supply voltage to V_{DD1}. Decouple the supply pin to GND_1 with a 10 µF capacitor in parallel with a 100 nF capacitor as close to the GND_1 pin and V_{DD1} pin as possible.
2	V_{IN+}	Positive Analog Input.
3	V_{IN-}	Negative Analog Input.
4	GND_1	Ground 1. GND_1 is the ground reference point for all circuitry on the isolated side.
5	GND_2	Ground 2. GND_2 is the ground reference point for all circuitry on the nonisolated side.
6	MDAT	Serial Data Output. The single-bit modulator output is supplied to MDAT as a serial data stream. MDAT is clocked out on the rising edge of the MCLKIN input and is valid on the following MCLKIN rising edge.
7	MCLKIN	Master Clock Logic Input. 5 MHz to 21 MHz frequency range. The bit stream from the modulator is propagated on the rising edge of the MCLKIN.
8	V_{DD2}	Supply Voltage, 3 V to 5.5 V. V_{DD2} is the supply voltage for the nonisolated side and is relative to GND_2. Decouple this supply to GND_2 with a 10 µF capacitor in parallel with a 100 nF capacitor as close to the GND_2 pin and V_{DD2} pin as possible.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD1} = 5 V, V_{DD2} = 5 V, V_{IN+} = −50 mV to +50 mV, V_{IN-} = 0 V, and f_{MCLKIN} = 20 MHz, using a sinc3 filter with a 256 oversampling ratio (OSR), unless otherwise noted.

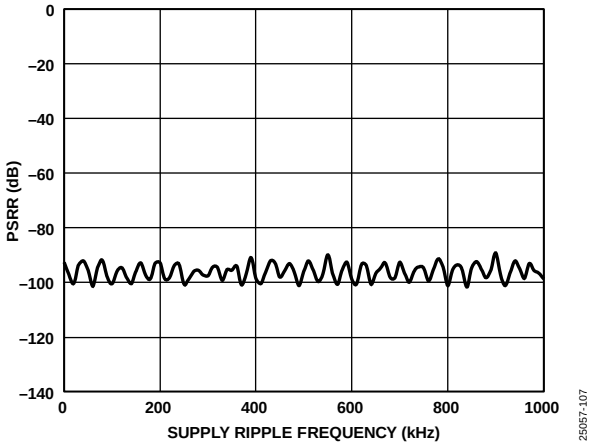


Figure 7. Power Supply Rejection Ratio (PSRR) vs. Supply Ripple Frequency

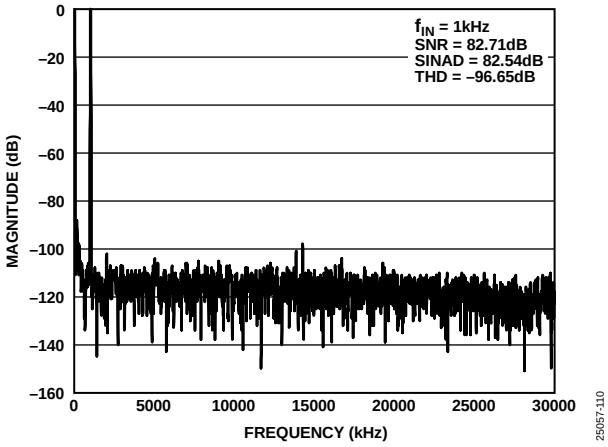


Figure 10. Typical Fast Fourier Transform (FFT)

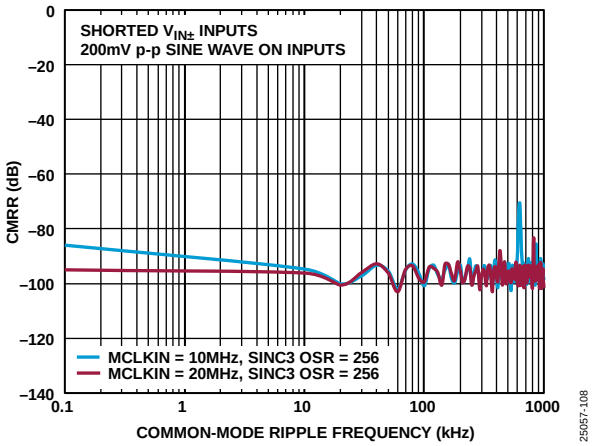


Figure 8. Common-Mode Rejection Ratio (CMRR) vs. Common-Mode Ripple Frequency

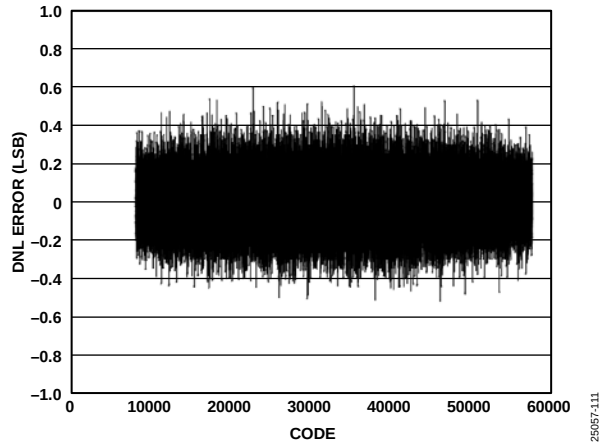


Figure 11. Typical DNL Error

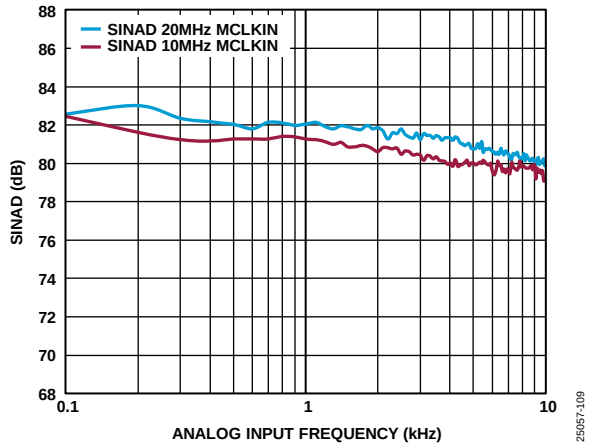


Figure 9. SINAD vs. Analog Input Frequency

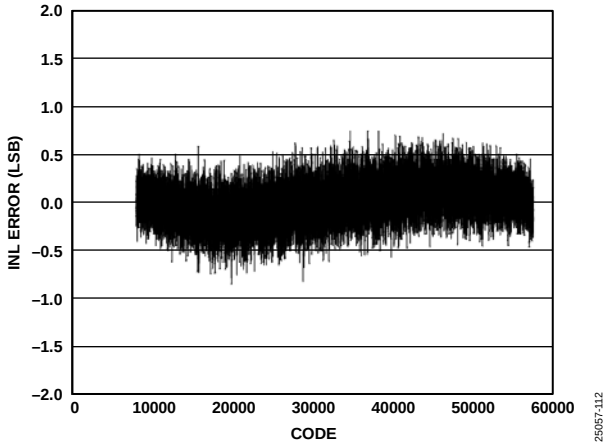


Figure 12. Typical INL Error

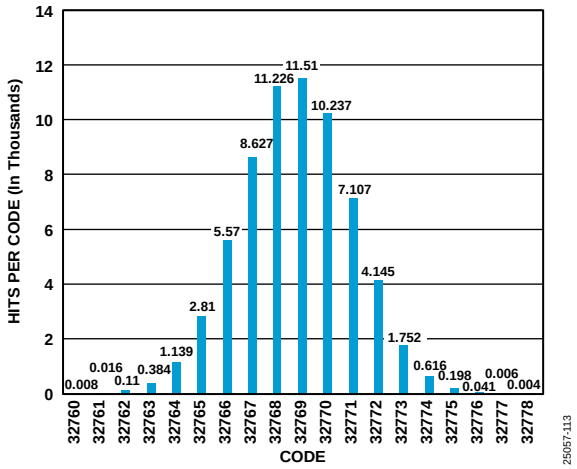


Figure 13. Histogram of Codes at the Code Center

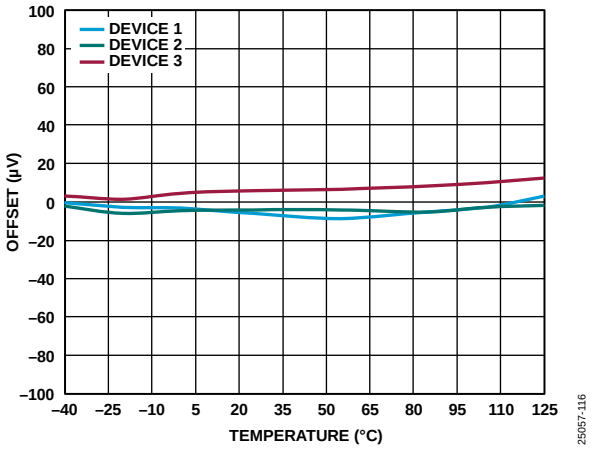


Figure 16. Offset vs. Temperature

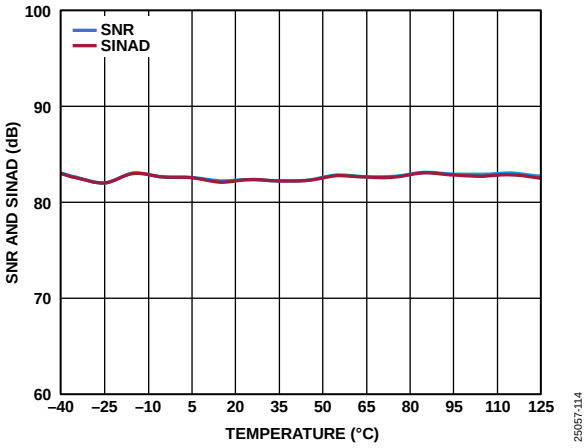


Figure 14. SNR and SINAD vs. Temperature

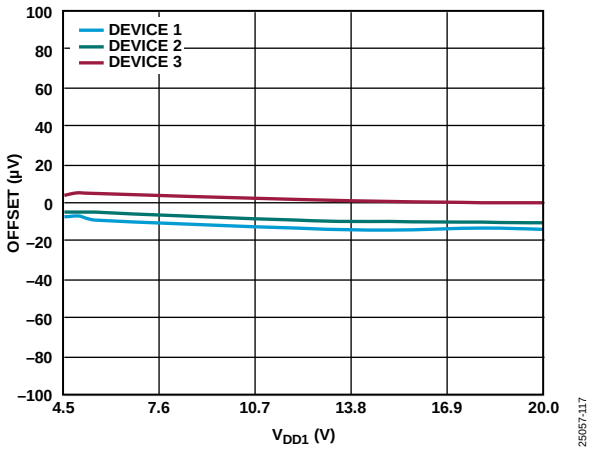


Figure 17. Offset vs. V_{DD1}

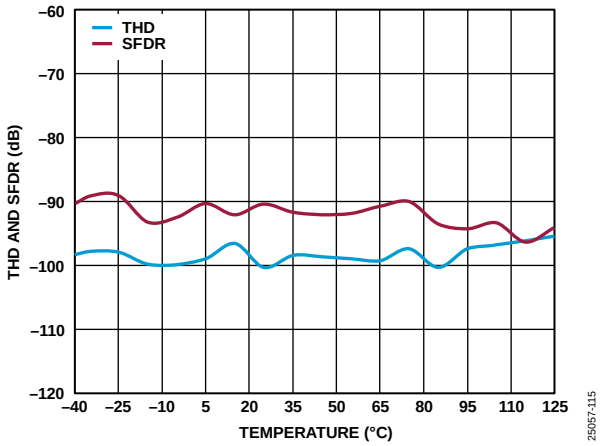


Figure 15. THD and SFDR vs. Temperature

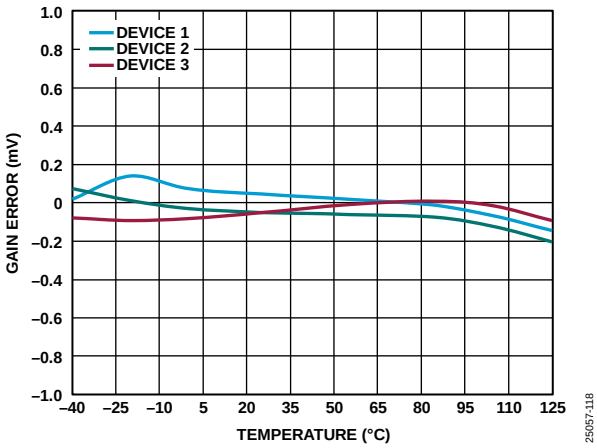


Figure 18. Gain Error vs. Temperature

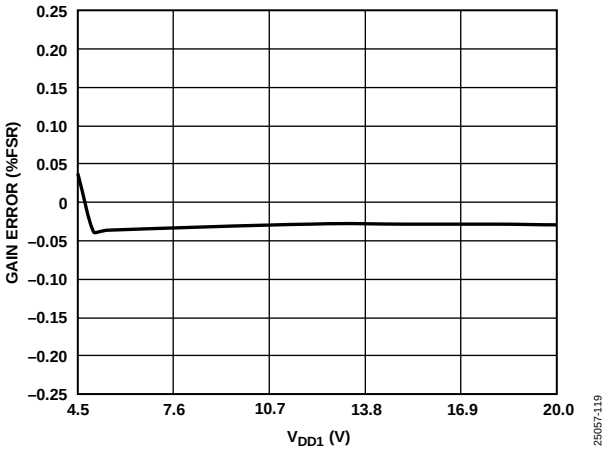


Figure 19. Gain Error vs. V_{DD1}

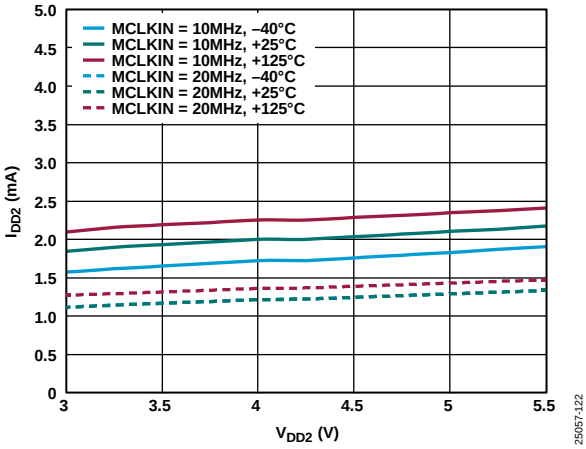


Figure 22. I_{DD2} vs. V_{DD2} at Various Temperatures and Clock Rates

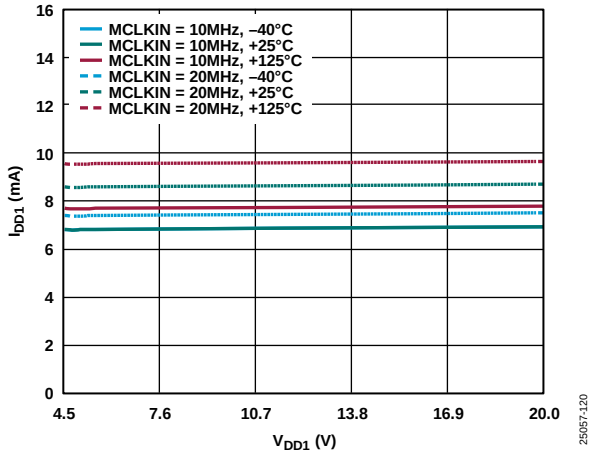


Figure 20. I_{DD1} vs. V_{DD1} at Various Temperatures and Clock Rates

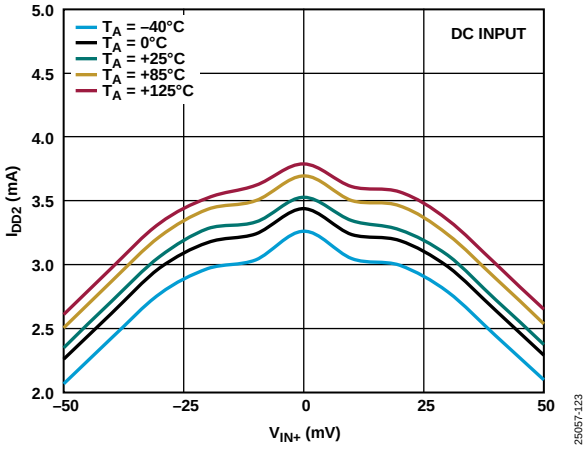


Figure 23. I_{DD2} vs. V_{IN+} DC Input at Various Temperatures

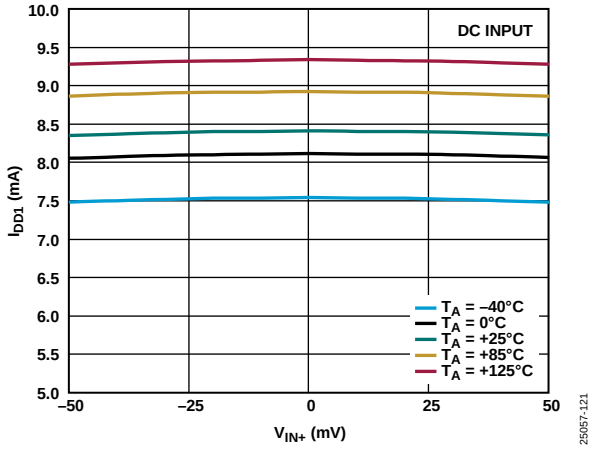


Figure 21. I_{DD1} vs. V_{IN+} DC Input at Various Temperatures

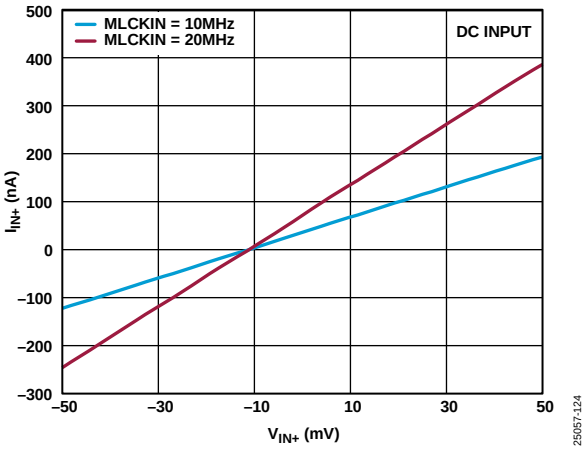


Figure 24. V_{IN+} Current (I_{IN+}) vs. V_{IN+} DC Input

TERMINOLOGY

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the analog-to-digital converter (ADC).

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are specified negative full scale, −50 mV ($V_{IN+} - V_{IN-}$), Code 7168 for the 16-bit level, and specified positive full scale, +50 mV ($V_{IN+} - V_{IN-}$), Code 58,368 for the 16-bit level.

Offset Error
Offset error is the deviation of the midscale code (32,768 for the 16-bit level) from the ideal $V_{IN+} - V_{IN-}$ (that is, 0 V).

Offset Drift vs. Temperature
The offset drift is calculated using the box method, as shown by the following equation:

$$Offset\ Drift = ((Voltage_{MAX} - Voltage_{MIN})/T_{\Delta})$$

where:
$Voltage_{MAX}$ is the maximum offset error point recorded.
$Voltage_{MIN}$ is the minimum offset error point recorded.
T_{Δ} is the difference in temperature between the maximum and minimum operating range.

Gain Error
The gain error includes both positive full-scale gain error and negative full-scale gain error. Positive full-scale gain error is the deviation of the specified positive full-scale code (58,368 for the 16-bit level) from the ideal $V_{IN+} - V_{IN-}$ (50 mV) after the offset error is adjusted out. Negative full-scale gain error is the deviation of the specified negative full-scale code (7168 for the 16-bit level) from the ideal $V_{IN+} - V_{IN-}$ (−50 mV) after the offset error is adjusted out.

Gain Error Drift vs. Temperature
The gain error drift (GED) is calculated using the box method, as shown by the following equation:

$$GED\ (\text{ppm}) = ((Voltage_{MAX} - Voltage_{MIN})/(VoltageFS \times T_{\Delta})) \times 10^6$$

where:
$Voltage_{MAX}$ is the maximum gain error point recorded.
$Voltage_{MIN}$ is the minimum gain error point recorded.
$VoltageFS$ is the analog input range full scale.
T_{Δ} is the difference in temperature between the maximum and minimum operating range.

Signal-to-Noise-and-Distortion Ratio (SINAD)
SINAD is the measured ratio of signal to noise and distortion at the output of the ADC. The signal is the rms value of the sine wave, and noise is the rms sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), including harmonics, but excluding dc.

Signal-to-Noise Ratio (SNR)
SNR is the measured ratio of signal to noise at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ($f_S/2$), excluding dc.

The ratio is dependent on the number of quantization levels in the digitization process, that is, the greater the number of levels, the smaller the quantization noise. The theoretical SNR for an ideal N-bit converter with a sine wave input is given by

$$SNR = (6.02N + 1.76)\ \text{dB}$$

Therefore, for a 12-bit converter, the SNR is 74 dB.

Isolation Common-Mode Transient Immunity (CMTI)
The isolation CMTI specifies the rate of the rise and fall of a transient pulse applied across the isolation boundary, beyond which clock or data is corrupted. Both the rate of change and the absolute common-mode voltage of the pulse are recorded. The ADuM7704 is tested under both static and dynamic CMTI conditions. Static testing detects single-bit errors from the device. Dynamic testing monitors the filtered data output for variations in noise performance to a randomized application of the CMTI pulse.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the harmonics to the fundamental. It is defined as

$$THD\ (\text{dB}) = 20\log\frac{\sqrt{V2^2+V3^2+V4^2+V5^2+V6^2}}{V1}$$

where:
V2, *V3*, *V4*, *V5,* and *V6* are the rms amplitudes of the second through the sixth harmonics.
V1 is the rms amplitude of the fundamental.

Peak Harmonic or Spurious-Free Dynamic Range (SFDR) Noise
Peak harmonic or SFDR noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is a noise peak.

Effective Number of Bits (ENOB)
ENOB is defined by

$$ENOB = (SINAD - 1.76)/6.02\ \text{bits}$$

Noise Free Code Resolution

Noise free code resolution represents the resolution in bits for which there is no code flicker. The noise free code resolution for an N-bit converter is defined as

$$\textit{Noise Free Code Resolution} \text{ (Bits)} = \log_2(2^N/\textit{Peak-to-Peak Noise})$$

The peak-to-peak noise in LSBs is measured with $V_{IN+} = V_{IN-} = 0$ V.

Common-Mode Rejection Ratio (CMRR)

CMRR is the ratio of the power in the ADC output at ±50 mV frequency, f, to the power of a +50 mV p-p sine wave applied to the common-mode voltage of V_{IN+} and V_{IN-} of frequency, f_S, as

$$\textit{CMRR} \text{ (dB)} = 10 \log(Pf/Pf_S)$$

where:

Pf is the power at frequency, f, in the ADC output.

Pf_S is the power at frequency, f_S, in the ADC output.

Power Supply Rejection Ratio (PSRR)

Variations in power supply affect the full-scale transition but not the linearity of the converter. PSRR is the maximum change in the specified full-scale (±50 mV) transition point due to a change in power supply voltage from the nominal value.

THEORY OF OPERATION

CIRCUIT INFORMATION

The ADuM7704 isolated Σ-Δ modulator converts an analog input signal to a high speed (21 MHz maximum), single-bit data stream. The time average single-bit data from the modulator is directly proportional to the input signal. Figure 25 shows a typical application circuit where the ADuM7704 provides isolation between the analog input, a current sensing resistor or shunt, and the digital output, which is then processed by a digital filter to provide an N-bit word.

ANALOG INPUT

The pseudo differential analog input of the ADuM7704 is implemented with a switched capacitor circuit. This circuit implements a second-order modulator stage that digitizes the input signal to a single-bit output stream. The sample clock (MCLKIN) provides the clock signal for the conversion process as well as the output data framing clock. This clock source is externally supplied to the ADuM7704. The analog input signal is continuously sampled by the modulator and compared to an internal voltage reference. A digital stream that accurately represents the analog input over time appears at the output of the converter (see Figure 26).

A differential signal of 0 V ideally results in a stream of alternating 1s and 0s at the MDAT output pin. This output is high 50% of the time and low 50% of the time. A differential input of 50 mV produces a stream of 1s and 0s that are high 89.06% of the time. A differential input of −50 mV produces a stream of 1s and 0s that are high 10.94% of the time.

A differential input of 64 mV ideally results in a stream of all 1s. A differential input of −64 mV ideally results in a stream of all 0s. The ADuM7704 absolute full-scale range is ±64 mV, and the specified full-scale performance range is ±50 mV, as shown in Table 14.

Table 14. Analog Input Range

Analog Input	Voltage Input (mV)
Positive Full-Scale (+FS) Value	+64
Positive Specified Performance	+50
Zero	0
Negative Specified Performance	−50
Negative Full-Scale (−FS) Value	−64

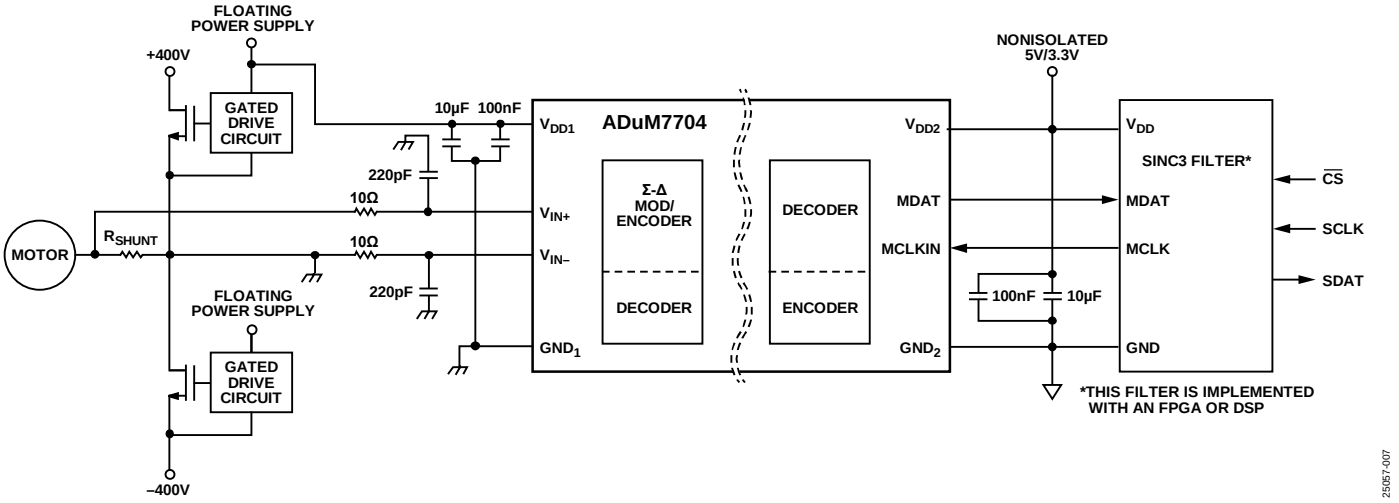


Figure 25. Typical Application Circuit

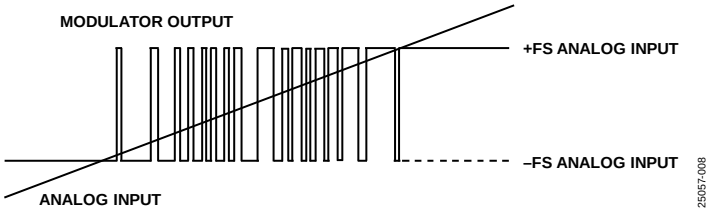


Figure 26. Analog Input vs. Modulator Output

To reconstruct the original information, this output must be digitally filtered and decimated. A sinc3 filter is recommended because this filter is one order higher than that of the ADuM7704 modulator, which is a second-order modulator. When a 256 decimation rate is used, the resulting 16-bit word rate is 78.1 kSPS, assuming a 20 MHz external clock frequency. See the Digital Filter section for more detailed information on the sinc filter implementation. Figure 27 shows the transfer function of the ADuM7704 relative to the 16-bit output.

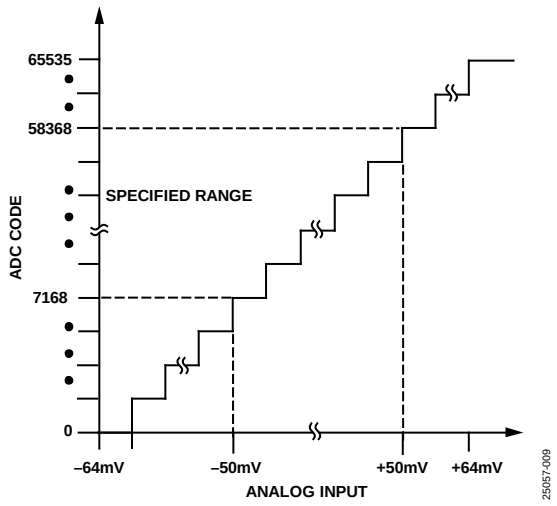


Figure 27. Filtered and Decimated 16-Bit Transfer Function

APPLICATIONS INFORMATION

CURRENT SENSING APPLICATIONS

The ADuM7704 is ideally suited for current sensing applications where the voltage across a shunt resistor (R_{SHUNT}) is monitored. The load current flowing through an external shunt resistor produces a voltage at the input terminals of the ADuM7704. The ADuM7704 provides isolation between the analog input from the current sensing resistor and the digital outputs. By selecting the appropriate shunt resistor value, a variety of current ranges can be monitored.

Choosing R_{SHUNT}

The R_{SHUNT} values used in conjunction with the ADuM7704 are determined by the specific application requirements in terms of voltage, current, and power. Small resistors minimize power dissipation, whereas low inductance resistors prevent any induced voltage spikes, and high tolerance devices reduce current variations. The final values chosen are a compromise between low power dissipation and accuracy. Higher value resistors use the full performance input range of the ADC, thus achieving maximum SNR performance. Low value resistors dissipate less power but do not use the full performance input range. The ADuM7704, however, delivers excellent performance, even with lower input signal levels, allowing low value shunt resistors to be used while maintaining system performance.

To choose a suitable shunt resistor, first determine the current through the shunt. Calculate the shunt current for a 3-phase induction motor as

$$I_{RMS} = PW/(1.73 \times V \times EF \times PF)$$

where:
I_{RMS} is the motor phase current (A rms).
PW is the motor power (W).
V is the motor supply voltage (V ac).
EF is the motor efficiency (%).
PF is the power efficiency (%).

To determine the shunt peak sense current (I_{SENSE}), consider the motor phase current and any overload that may be possible in the system. When the peak sense current is known, divide the voltage range of the ADuM7704 (±50 mV) by the peak sense current to yield a maximum shunt value.

If the power dissipation in the shunt resistor is too large, the shunt resistor can be reduced, and less of the ADC input range can be used. Figure 28 shows the SINAD performance characteristics and the ENOB of resolution for the ADuM7704 for different input signal amplitudes. The performance of the ADuM7704 at lower input signal ranges allows smaller shunt values to be used while still maintaining a high level of performance and overall system efficiency.

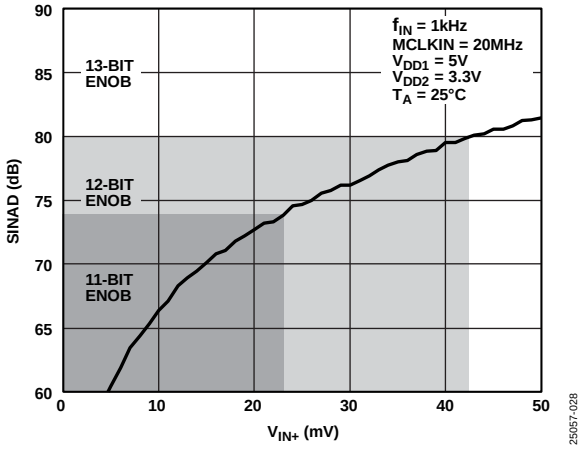


Figure 28. SINAD vs. V_{IN+} AC Input Signal Amplitude

R_{SHUNT} must dissipate the current^2 × resistance (I^2R) power losses. If the power dissipation rating of the resistor is exceeded, the value may drift, or the resistor may be damaged, resulting in an open circuit. This open circuit can result in a differential voltage across the terminals of the ADuM7704, in excess of the absolute maximum ratings. If I_{SENSE} has a large high frequency component, choose a resistor with low inductance.

VOLTAGE SENSING APPLICATIONS

The ADuM7704 can also be used for isolated voltage monitoring. For example, in motor control applications, the device can be used to sense the bus voltage. In applications where the voltage being monitored exceeds the specified analog input range of the ADuM7704, a voltage divider network can be used to reduce the voltage being monitored to the required range.

INPUT FILTER

In a typical use case for directly measuring the voltage across a shunt resistor, the ADuM7704 can be connected directly across the shunt resistor with a simple RC low-pass filter on each input.

The recommended circuit configuration for driving the differential inputs to achieve best performance is shown in Figure 29. An RC low-pass filter is placed on both the analog input pins. Recommended values for the resistors and capacitors are 10 Ω and 220 pF, respectively. If possible, equalize the source impedance on each analog input to minimize offset.

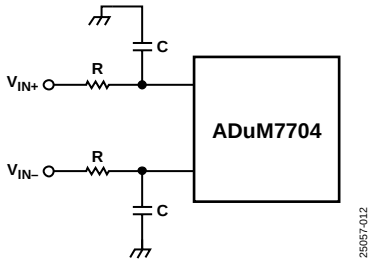


Figure 29. RC Low-Pass Filter Input Network

The input filter configuration for the ADuM7704 is not limited to the low-pass structure shown in Figure 29. The differential RC filter configuration shown in Figure 30 also achieves excellent performance. Recommended values for the resistors and capacitor are 22 Ω and 47 pF, respectively.

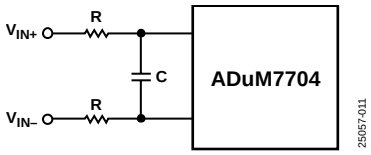


Figure 30. Differential RC Filter Network

DIGITAL FILTER

The output of the ADuM7704 is a continuous digital bit stream. To reconstruct the original input signal information, this output bit stream must be digitally filtered and decimated. A sinc filter is recommended due to simplicity of the filter. A sinc3 filter is recommended because the filter is one order higher than that of the ADuM7704 modulator, which is a second-order modulator. The type of filter selected, the decimation rate, and the modulator clock used determines the overall system resolution and throughput rate. The higher the decimation rate, the greater the system accuracy, as shown in Figure 31. However, there is a trade-off between accuracy and throughput rate and, therefore, higher decimation rates result in lower throughput solutions. Note that for a given bandwidth requirement, a higher MCLKIN frequency can allow higher decimation rates to be used, resulting in higher SNR performance.

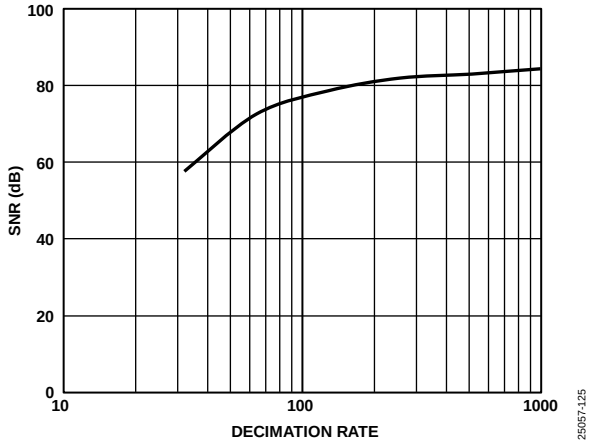


Figure 31. SNR vs. Decimation Rate of Sinc3 Filter Order

A sinc3 filter is recommended for the ADuM7704. This filter can be implemented on a field programmable gate array (FPGA) or a digital signal processor (DSP). Equation 1 describes the transfer function of a sinc filter.

$$H(Z) = \left(\frac{1}{DR} \frac{\left(1 - Z^{-\mathrm{DR}}\right)}{\left(1 - Z^{-1}\right)} \right)^{N} \quad (1)$$

where:
Z is the sample.
DR is the decimation rate.
N is the sinc filter order.

The throughput rate of the sinc filter is determined by the modulator clock and the decimation rate selected.

$$Throughput = MCLK/DR \quad (2)$$

where *MCLK* is the modulator clock frequency

As the decimation rate increases, the data output size from the sinc filter increases. The output data size is expressed in Equation 3. The 16 most significant bits are used to return a 16-bit result.

$$Data\ Size = N \times \log_2 DR \quad (3)$$

For a sinc3 filter, the −3 dB filter response point can be derived from the filter transfer function, Equation 1, and is 0.262 times the throughput rate. The filter characteristics for a third-order sinc filter are summarized in Table 15.

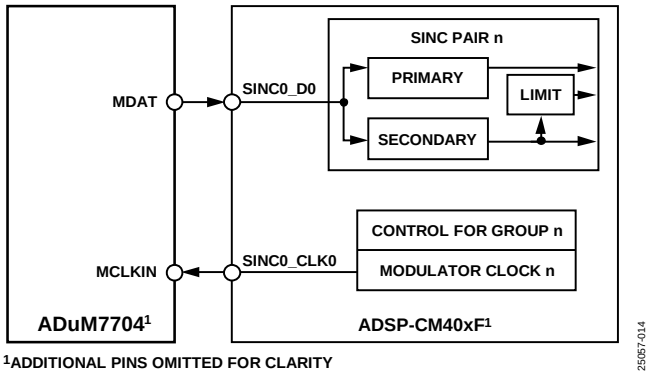
Table 15. Sinc3 Filter Characteristics for 20 MHz MCLKIN

Decimation Ratio (DR)	Throughput Rate (kHz)	Output Data Size (Bits)	Filter Response (kHz)
32	625	15	163.7
64	312.5	18	81.8
128	156.2	21	40.9
256	78.1	24	20.4
512	39.1	27	10.2

INTERFACING TO ADSP-CM4xx

The ADSP-CM4xx family of mixed-signal control processors contains an on-chip sinc filter and clock generation modules for direct connection to the ADuM7704 MCLKIN and MDAT pins. The ADSP-CM4xx can process bit streams from four ADuM7704 devices using a pair of configurable sinc filters for each bit stream. The primary sinc filter of each pair produces the filtered and decimated output for the pair. The output can be decimated to any integer rate between 8 times and 256 times lower than the input rate. The four secondary sinc filters are low latency filters with programmable positive and negative overrange detection comparators that can detect system fault conditions

Figure 32 shows the typical interface between the ADuM7704 and the ADSP-CM4xx. Additional information on the configuration of the sinc filter modules in the ADSP-CM4xx can be found in the AN-1265 Application Note.



[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 32. Interfacing the ADuM7704 to the ADSP-CM4xx

GROUNDING AND LAYOUT

It is recommended to decouple the V_{DD1} supply with a 10 µF capacitor in parallel with a 100 nF capacitor to any GND_1 pin. Decouple the V_{DD2} supply with a 10 µF capacitor in parallel with a 100 nF capacitor to any GND_2 pin. In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout so that any coupling that occurs equally affects all pins on a given component side. Failure to ensure equal coupling can cause voltage differentials between pins to exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage. Place any decoupling capacitors used as close to the supply pins as possible.

Minimize series resistance in the analog inputs to avoid any distortion effects, especially at high temperatures. If possible, equalize the source impedance on each analog input to minimize offset. Check for mismatch and thermocouple effects on the analog input PCB tracks to reduce offset drift.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM7704.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 10 summarize the peak voltage for 37.5 years of (reinforced) service life for a bipolar, ac operating condition and the maximum VDE approved working voltages.

These tests subjected the ADuM7704 to continuous cross isolation voltages. To accelerate the occurrence of failures, the selected test voltages were values exceeding those of normal use. The time to failure values of these units were recorded and used to calculate the acceleration factors. These factors were then used to calculate the time to failure under the normal operating conditions. The values shown in Table 10 are the lesser of the following two values:

- The value that ensures at least a 37.5 year lifetime of continuous (reinforced) use.
- The maximum VDE approved working voltage.

The lifetime of the ADuM7704 is guaranteed using a bipolar ac waveform, as shown in Figure 33.

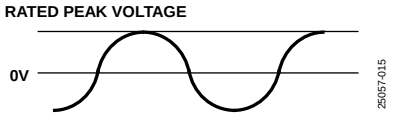


Figure 33. Bipolar AC Waveform, 50 Hz or 60 Hz

OUTLINE DIMENSIONS

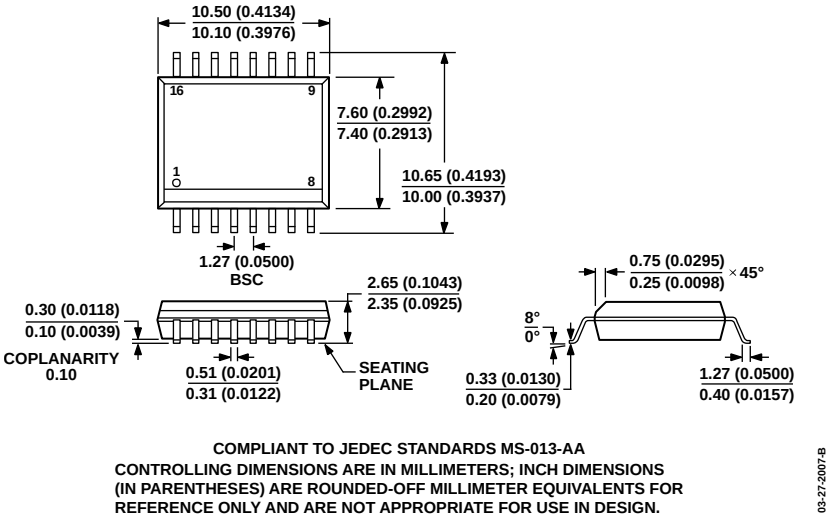


Figure 34. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

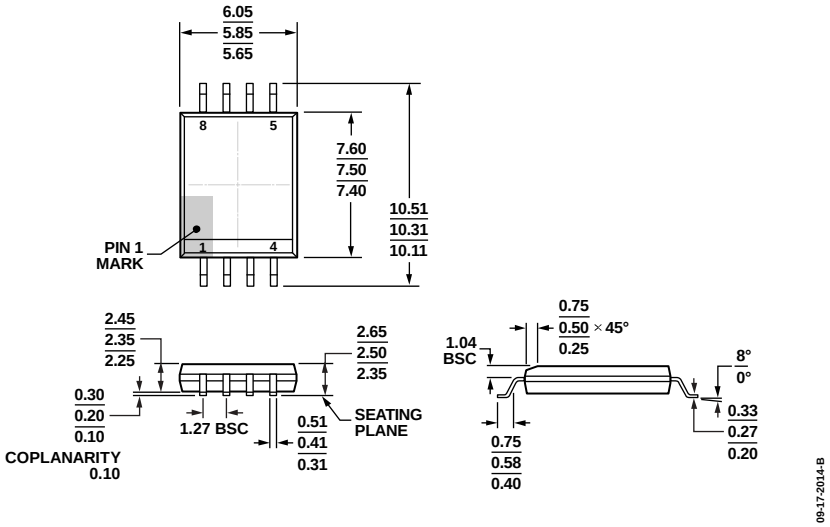


Figure 35. 8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]
Wide Body
(RI-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADuM7704BRWZ	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADuM7704BRWZ-RL	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADuM7704BRWZ-RL7	−40°C to +125°C	16-Lead Standard Small Outline Package [SOIC_W]	RW-16
ADuM7704-8BRIZ	−40°C to +105°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1
ADuM7704-8BRIZ-RL	−40°C to +105°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1
ADuM7704-8BRIZ-RL7	−40°C to +105°C	8-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC]	RI-8-1
EV-ADuM7704-8FMCZ		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] The EV-ADuM7704-8FMCZ is compatible with the EVAL-SDP-CH1Z high speed controller board.

D25057-8/20(0)

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