



SN74HC76/HCT76(LX) Dual JK Flip-Flop with Set and Reset; Negative-Edge Trigger

Product Specification

Specification Revision History:

Version	Date	Description
2024-05-A0	2024-05	New
2024-09-A1	2024-09	Modify the parameters



Contents

1、 General Description.....	1
2、 Block Diagram And Pin Description	2
2.1、 Block Diagram	2
2.2、 Pin Configurations.....	2
2.3、 Pin Description.....	3
2.4、 Function Table.....	3
3、 Electrical Parameter	4
3.1、 Absolute Maximum Ratings.....	4
3.2、 Recommended Operating Conditions.....	4
3.3、 Electrical Characteristics	5
3.3.1、 DC Characteristics 1	5
3.3.2、 DC Characteristics 2	6
3.3.3、 AC Characteristics 1	7
3.3.4、 AC Characteristics 2	8
4、 Testing Circuit	9
4.1、 AC Testing Circuit	9
4.2、 Test Data	9
4.3、 AC Testing Waveforms.....	10
4.4、 Measurement Points	11
5、 Package Information	12
5.1、 DIP16	12
5.2、 SOP16	13
6、 Statements And Notes	14



1、 General Description

The SN74HC/HCT76 is dual J-K Flip-Flops (with Preset and Clear).

Features:

- Supply voltage range:
SN74HC76: 2V to 6V
SN74HCT76: 4.5V to 5.5V
- Input levels:
SN74HC76: CMOS level
SN74HCT76: TTL level
- Temperature range: -40°C to +125°C
- Packaging information: DIP16/SOP16



Ordering Information:

Tube packing specifications:

Part number	Packaging form	Marking code	Tube quantity	Boxed tube quantity	Boxed quantity	Notes
SN74HC76N(LX)	DIP16	SN74HC76N	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm
SN74HCT76N(LX)	DIP16	SN74HCT76N	25 PCS/tube	40 tube/box	1000 PCS/box	Dimensions of plastic enclosure: 19.0mm×6.4mm Pin spacing: 2.54mm

Reel packing specifications:

Part number	Packaging form	Marking code	Reel quantity	Boxed reel quantity	Notes
SN74HC76DR(LX)	SOP16	SN74HC76	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
SN74HCT76DR(LX)	SOP16	SN74HCT76	4000 PCS/reel	8000 PCS/box	Dimensions of plastic enclosure: 10.0mm×3.9mm Pin spacing:1.27mm
SN74HC76PW(LX)	TSSOP16	HC76	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm
SN74HCT76PW(LX)	TSSOP16	HCT76	5000 PCS/reel	10000 PCS/box	Dimensions of plastic enclosure: 5.0mm×4.4mm Pin spacing:0.65mm

Note: If the physical information is inconsistent with the ordering information, please refer to the actual product.

2、Block Diagram And Pin Description

2.1、Block Diagram

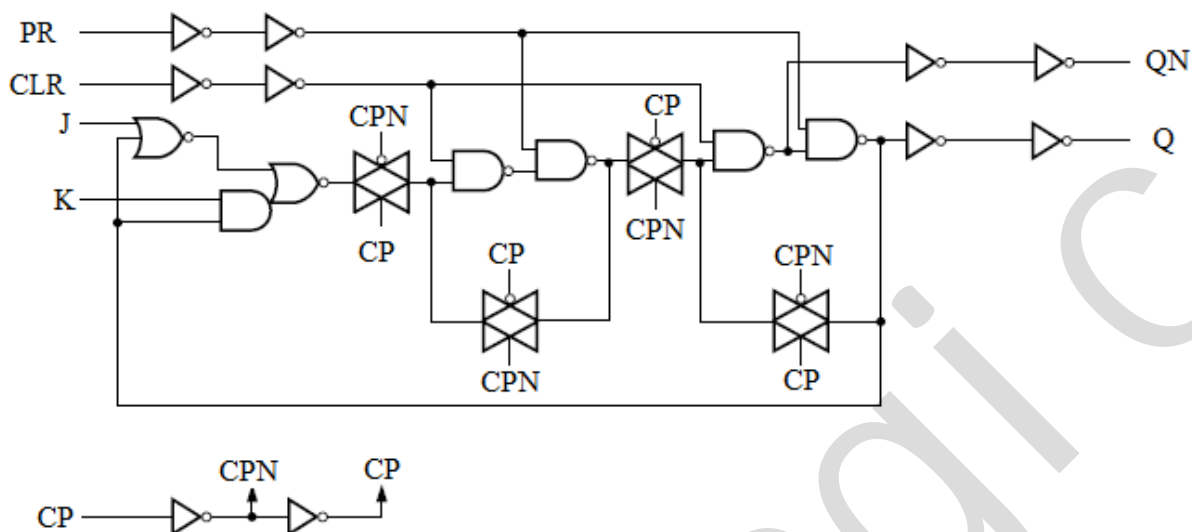
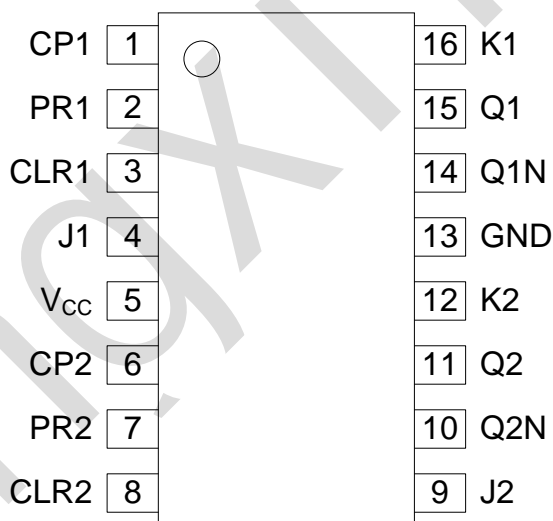


Figure 1. Block Diagram

2.2、Pin Configurations





2.3、Pin Description

Pin No.	Pin Name	Description
1	CP1	clock input (HIGH-to-LOW, edge-triggered)
2	PR1	asynchronous master preset input
3	CLR1	asynchronous master reset input
4	J1	synchronous J input
5	V _{CC}	supply voltage
6	CP2	clock input (HIGH-to-LOW, edge-triggered)
7	PR2	asynchronous master preset input
8	CLR2	asynchronous master reset input
9	J2	synchronous J input
10	Q2N	complement flip-flop output
11	Q2	true flip-flop output
12	K2	Synchronous K input
13	GND	ground (0 V)
14	Q1N	flip-flop output
15	Q1	true flip-flop output
16	K1	Synchronous K input

2.4、Function Table

PR	CLR	CP	J	K	Q	QN
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H ^[1]	H ^[1]
H	H	↓	L	L	No change	
H	H	↓	L	H	L	H
H	H	↓	H	L	H	L
H	H	↓	H	H	Toggle	
H	H	L	X	X	No change	
H	H	H	X	X	No change	
H	H	↑	X	X	No change	

Note:

H=HIGH voltage level; L=LOW voltage level. X=Irrelevant

[1] Q and QN will remain High as long as Preset and Clear are Low, but Q and QN are unpredictable, if Preset and Clear go High simultaneously.



3、Electrical Parameter

3.1、Absolute Maximum Ratings

(Voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions	Min.	Max.	Unit
supply voltage	V_{CC}	-	-0.5	+7	V
supply current	I_{CC}	-	-	50	mA
ground current	I_{GND}	-	-50	-	mA
input clamping current	I_{IK}	$V_I < -0.5V$ or $V_I > V_{CC}+0.5V$	-	± 20	mA
output clamping current	I_{OK}	$V_O < -0.5V$ or $V_O > V_{CC}+0.5V$	-	± 20	mA
output current	I_O	$-0.5V < V_O < V_{CC}+0.5V$	-	± 25	mA
storage temperature	T_{stg}	-	-65	+150	$^{\circ}C$
soldering temperature	T_L	10s	DIP		$^{\circ}C$
			SOP/TSSOP		

3.2、Recommended Operating Conditions

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
SN74HC76						
supply voltage	V_{CC}	-	2.0	5.0	6.0	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	$^{\circ}C$
SN74HCT76						
supply voltage	V_{CC}	-	4.5	5.0	5.5	V
input voltage	V_I	-	0	-	V_{CC}	V
output voltage	V_O	-	0	-	V_{CC}	V
ambient temperature	T_{amb}	-	-40	-	+125	$^{\circ}C$



3.3、Electrical Characteristics

3.3.1、DC Characteristics 1

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V _{CC}	Conditions	Min.	Typ.	Max.	Unit
SN74HC76							
HIGH-level input voltage	V _{IH}	2.0V	-	1.5	1.2	-	V
		4.5V	-	3.15	2.4	-	V
		6.0V	-	4.2	3.2	-	V
LOW-level input voltage	V _{IL}	2.0V	-	-	0.8	0.5	V
		4.5V	-	-	2.1	1.35	V
		6.0V	-	-	2.8	1.8	V
HIGH-level output voltage	V _{OH}	2.0V	I _O = -20uA	1.9	2.0	-	V
		4.5V	I _O = -20uA	4.4	4.5	-	V
		6.0V	I _O = -20uA	5.9	6.0	-	V
		4.5V	I _O = -4.0mA	3.84	4.32	-	V
		6.0V	I _O = -5.2mA	5.34	5.81	-	V
LOW-level output voltage	V _{OL}	2.0V	I _O = 20uA	-	0	0.1	V
		4.5V	I _O = 20uA	-	0	0.1	V
		6.0V	I _O = 20uA	-	0	0.1	V
		4.5V	I _O = 4.0mA	-	0.15	0.33	V
		6.0V	I _O = 5.2mA	-	0.16	0.33	V
input leakage current	I _I	6.0V	V _I = V _{CC} or GND	-	-	±2	uA
supply current	I _{CC}	6.0V	V _I = V _{CC} or GND; I _O = 0A	-	-	2	uA
SN74HCT76							
HIGH-level input voltage	V _{IH}	4.5~5.5V	-	2.0	1.6	-	V
LOW-level input voltage	V _{IL}	4.5~5.5V	-	-	1.2	0.8	V
HIGH-level output voltage	V _{OH}	4.5V	I _O = -20uA	4.4	4.5	-	V
			I _O = -4.0mA	3.84	4.32	-	V
LOW-level output voltage	V _{OL}	4.5V	I _O = 20uA	-	0	0.1	V
			I _O = 4.0mA	-	0.15	0.33	V
input leakage current	I _I	5.5V	V _I = V _{CC} or GND	-	-	±2	uA
supply current	I _{CC}	6.0V	V _I = V _{CC} or GND; I _O = 0A	-	-	2	uA
additional supply current	ΔI _{CC}	4.5~5.5V	One input at V _I = V _{CC} - 2.1V; Other inputs at V _{CC} or GND; I _O = 0A	-	-	135	uA



.3.2、DC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V _{CC}	Conditions	Min.	Typ.	Max.	Unit
SN74HC76							
HIGH-level input voltage	V _{IH}	2.0V	-	1.5	-	-	V
		4.5V	-	3.15	-	-	V
		6.0V	-	4.2	-	-	V
LOW-level input voltage	V _{IL}	2.0V	-	-	-	0.5	V
		4.5V	-	-	-	1.35	V
		6.0V	-	-	-	1.8	V
HIGH-level output voltage	V _{OH}	2.0V	I _O =-20uA	1.9	-	-	V
		4.5V	I _O =-20uA	4.4	-	-	V
		6.0V	I _O =-20uA	5.9	-	-	V
		4.5V	I _O =-4.0mA	3.7	-	-	V
		6.0V	I _O =-5.2mA	5.2	-	-	V
LOW-level output voltage	V _{OL}	2.0V	I _O =20uA	-	-	0.1	V
		4.5V	I _O =20uA	-	-	0.1	V
		6.0V	I _O =20uA	-	-	0.1	V
		4.5V	I _O =4.0mA	-	-	0.4	V
		6.0V	I _O =5.2mA	-	-	0.4	V
input leakage current	I _I	6.0V	V _I =V _{CC} or GND	-	-	±4	uA
supply current	I _{CC}	6.0V	V _I =V _{CC} or GND; I _O =0A	-	-	4	uA
SN74HCT76							
HIGH-level input voltage	V _{IH}	4.5~5.5V	-	2.0	-	-	V
LOW-level input voltage	V _{IL}	4.5~5.5V	-	-	-	0.8	V
HIGH-level output voltage	V _{OH}	4.5V	I _O =-20uA	4.4	-	-	V
			I _O =-4.0mA	3.7	-	-	V
LOW-level output voltage	V _{OL}	4.5V	I _O =20uA	-	-	0.1	V
			I _O =4.0mA	-	-	0.4	V
input leakage current	I _I	5.5V	V _I =V _{CC} or GND	-	-	±4	uA
supply current	I _{CC}	6.0V	V _I =V _{CC} or GND; I _O =0A	-	-	4	uA
additional supply current	ΔI _{CC}	4.5~5.5V	One input at V _I =V _{CC} -2.1V; Other inputs at V _{CC} or GND; I _O =0A	-	-	147	uA



3.3.3、AC Characteristics 1

($T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V _{CC}	Conditions	Min.	Typ.	Max.	Unit	
SN74HC76								
CP to Q or QN propagation delay	t _{PLH} , t _{PHL}	2.0V	C _L =50pF	see Figure 3	-	-	190	ns
		4.5V	C _L =50pF		-	21	38	ns
		6.0V	C _L =50pF		-	-	33	ns
CLR to Q or QN propagation delay	t _{PHL}	2.0V	C _L =50pF	see Figure 4	-	-	175	ns
		4.5V	C _L =50pF		-	17	35	ns
		6.0V	C _L =50pF		-	-	30	ns
PR to Q or QN propagation delay	t _{PHL}	2.0V	C _L =50pF	see Figure 4	-	-	175	ns
		4.5V	C _L =50pF		-	19	35	ns
		6.0V	C _L =50pF		-	-	30	ns
transition time	t _{THL} , t _{TLH}	2.0V	C _L =50pF	see Figure 3	-	-	95	ns
		4.5V	C _L =50pF		-	5	19	ns
		6.0V	C _L =50pF		-	-	16	ns
CP HIGH or LOW pulse width	tw	2.0V	C _L =50pF	see Figure 3	100	-	-	ns
		4.5V	C _L =50pF		20	6	-	ns
		6.0V	C _L =50pF		17	-	-	ns
CLR HIGH pulse width	tw	2.0V	C _L =50pF	see Figure 4	100	-	-	ns
		4.5V	C _L =50pF		20	6	-	ns
		6.0V	C _L =50pF		17	-	-	ns
PR HIGH Pulse width	tw	2.0V	C _L =50pF	see Figure 4	100	-	-	ns
		4.5V	C _L =50pF		20	6	-	ns
		6.0V	C _L =50pF		17	-	-	ns
J or K to CP set up time	tsu	2.0V	C _L =50pF	see Figure 3	125	-	-	ns
		4.5V	C _L =50pF		25	4	-	ns
		6.0V	C _L =50pF		21	-	-	ns
J or K to CP hold time	th	2.0V	C _L =50pF	see Figure 3	0	-	-	ns
		4.5V	C _L =50pF		0	-3	-	ns
		6.0V	C _L =50pF		0	-	-	ns
CLR to CPN recovery time	trec	2.0V	C _L =50pF	see Figure 4	125	-	-	ns
		4.5V	C _L =50pF		25	-	-	ns
		6.0V	C _L =50pF		21	-	-	ns
Maximum clock frequency	fmax	2.0V	C _L =50pF	see Figure 3	-	-	5	MHz
		4.5V	C _L =50pF		-	-	24	MHz
		6.0V	C _L =50pF		-	-	28	MHz



3.3.4、AC Characteristics 2

($T_{amb} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, voltages are referenced to GND (ground=0V), unless otherwise specified.)

Parameter	Symbol	V _{CC}	Conditions	Min.	Typ.	Max.	Unit	
SN74HC76								
CP to Q or QN propagation delay	t _{PLH} , t _{PHL}	2.0V	C _L =50pF	see Figure 3	-	-	228	ns
		4.5V	C _L =50pF		-	-	46	ns
		6.0V	C _L =50pF		-	-	40	ns
CLR to Q or QN propagation delay	t _{PHL}	2.0V	C _L =50pF	see Figure 4	-	-	210	ns
		4.5V	C _L =50pF		-	-	42	ns
		6.0V	C _L =50pF		-	-	36	ns
PR to Q or QN propagation delay	t _{PHL}	2.0V	C _L =50pF	see Figure 4	-	-	210	ns
		4.5V	C _L =50pF		-	-	42	ns
		6.0V	C _L =50pF		-	-	36	ns
transition time	t _{THL} , t _{TLH}	2.0V	C _L =50pF	see Figure 3	-	-	114	ns
		4.5V	C _L =50pF		-	-	23	ns
		6.0V	C _L =50pF		-	-	19	ns
CP HIGH or LOW pulse width	tw	2.0V	C _L =50pF	see Figure 3	120	-	-	ns
		4.5V	C _L =50pF		24	-	-	ns
		6.0V	C _L =50pF		20	-	-	ns
CLR HIGH pulse width	tw	2.0V	C _L =50pF	see Figure 4	120	-	-	ns
		4.5V	C _L =50pF		24	-	-	ns
		6.0V	C _L =50pF		20	-	-	ns
PR HIGH Pulse width	tw	2.0V	C _L =50pF	see Figure 4	120	-	-	ns
		4.5V	C _L =50pF		20	-	-	ns
		6.0V	C _L =50pF		17	-	-	ns
J or K to CP set up time	tsu	2.0V	C _L =50pF	see Figure 3	150	-	-	ns
		4.5V	C _L =50pF		30	-	-	ns
		6.0V	C _L =50pF		25	-	-	ns
J or K to CP hold time	th	2.0V	C _L =50pF	see Figure 3	0	-	-	ns
		4.5V	C _L =50pF		0	-	-	ns
		6.0V	C _L =50pF		0	-	-	ns
CLR to CPN recovery time	trec	2.0V	C _L =50pF	see Figure 4	150	-	-	ns
		4.5V	C _L =50pF		30	-	-	ns
		6.0V	C _L =50pF		25	-	-	ns
Maximum clock frequency	fmax	2.0V	C _L =50pF	see Figure 3	-	-	4	MHz
		4.5V	C _L =50pF		-	-	20	MHz
		6.0V	C _L =50pF		-	-	23	MHz

4、Testing Circuit

4.1、AC Testing Circuit

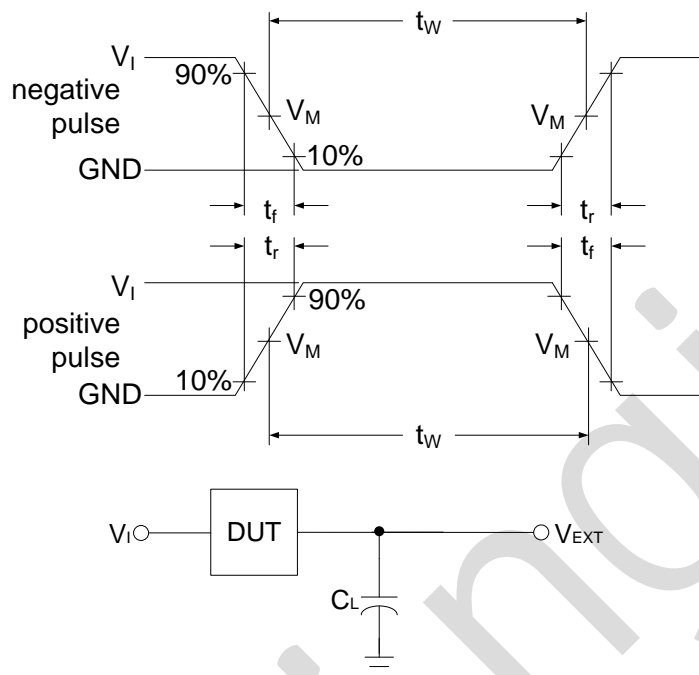


Figure 2. Test circuit for measuring switching times

C_L includes probe and jig capacitance.

4.2、Test Data

Type	Input		Load	V_{EXT}		
	V_I	$t_r = t_f$	C_L	t_{PLH}/t_{PHL}	t_{PLZ}/t_{PZL}	t_{PHZ}/t_{PZH}
SN74HC76	V_{CC}	6.0ns	15pF, 50pF	Open	V_{CC}	GND
SN74HCT76	3.0V	6.0ns	15pF, 50pF	Open	V_{CC}	GND

4.3、AC Testing Waveforms

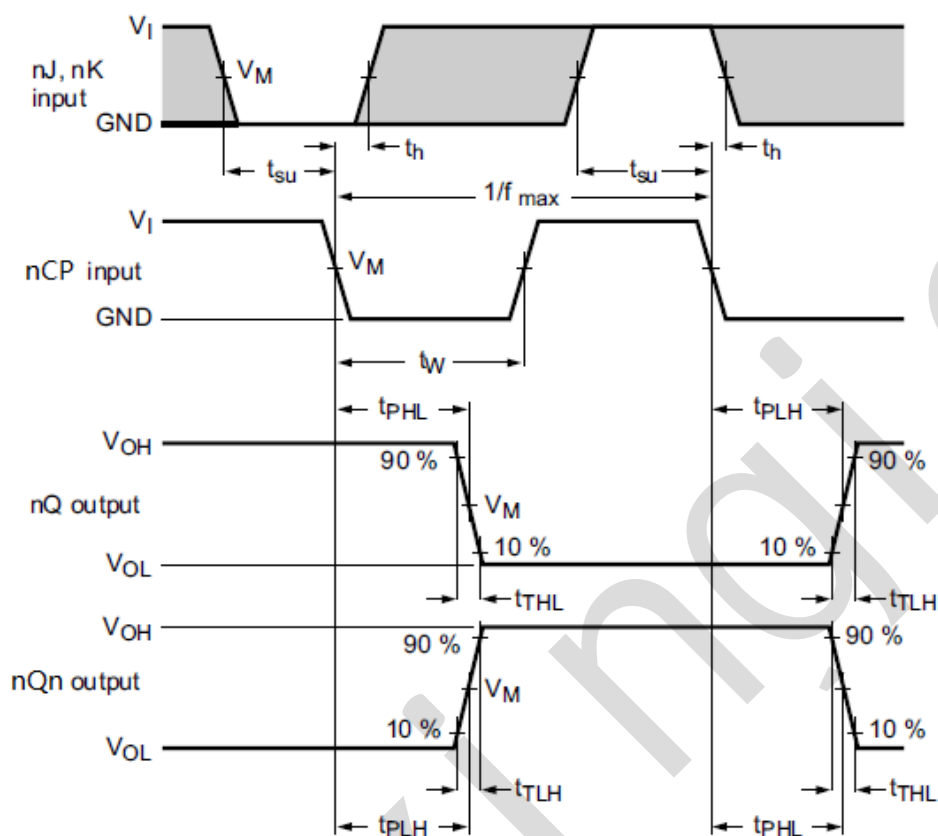


Figure 3. Clock propagation delays, pulse width, set-up and hold times, output transition times and the maximum frequency

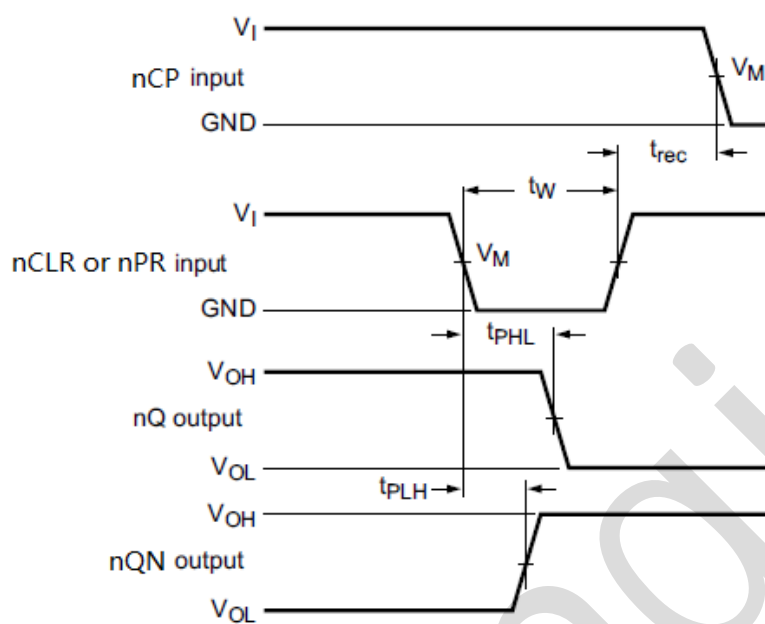


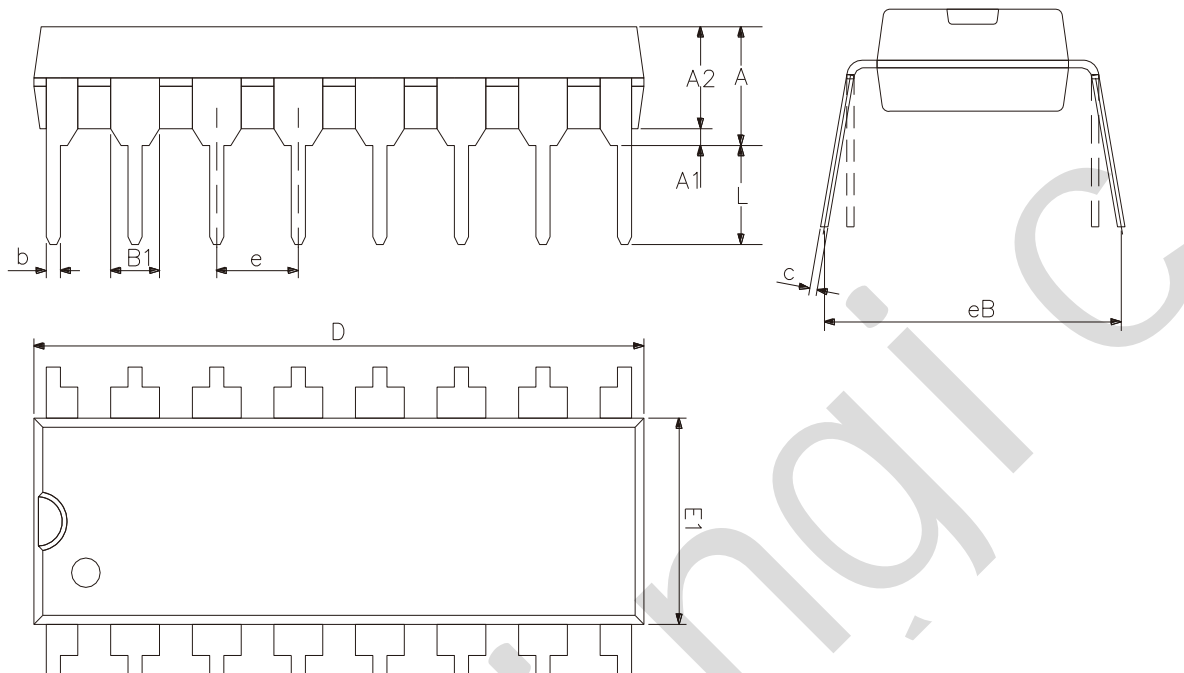
Figure 4. Reset or present propagation delays, pulse width and recovery time

4.4. Measurement Points

Type	Input	Output
	V_M	V_M
SN74HC76	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
SN74HCT76	1.3V	1.3V

5、Package Information

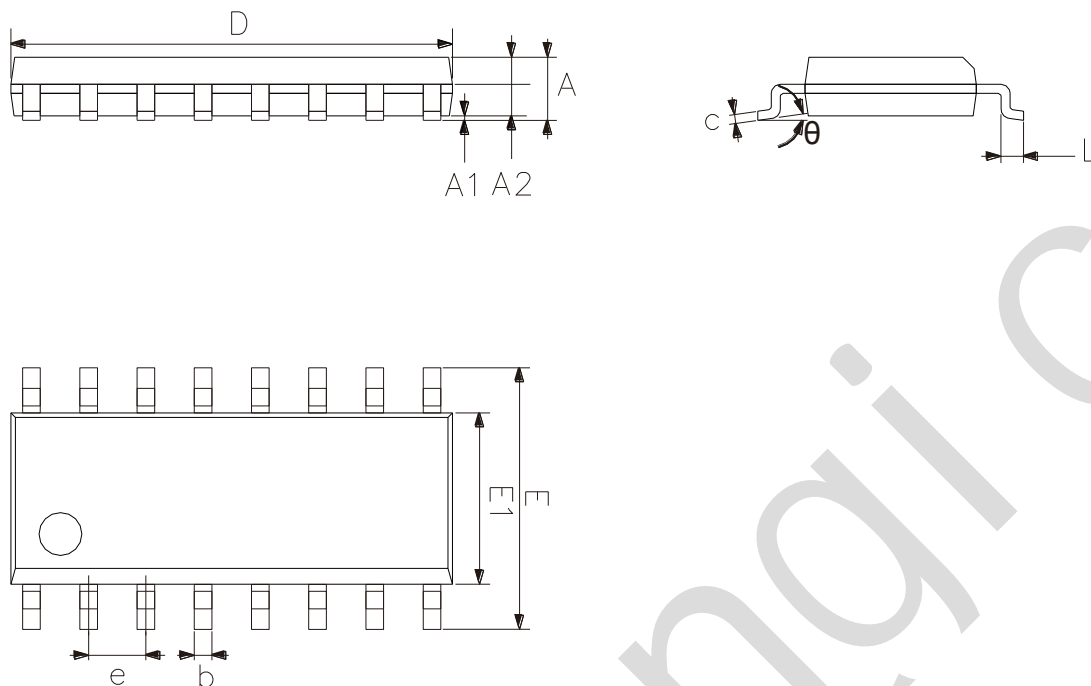
5.1、DIP16



2023/12/A	Dimensions In Millimeters	
Symbol	Min	Max
A2	3.00	3.60
A1	0.51	—
A	3.60	5.33
L	3.00	3.60
b	0.36	0.56
B1	1.52	
D	18.80	19.94
E1	6.20	6.60
e	2.54	
c	0.20	0.36
eB	7.62	9.30



5.2、SOP16



2023/12/A	Dimensions In Millimeters	
Symbol	Min.	Max.
A	1.35	1.80
A1	0.10	0.25
A2	1.25	1.55
b	0.33	0.51
c	0.19	0.25
D	9.50	10.10
E	5.80	6.30
E1	3.70	4.10
e	1.27	
L	0.35	0.89
θ	0°	8°



6、Statements And Notes

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