Embedded Multi Chip Package
eMCP

e•MMC™5.1 HS400 + LPDDR3

04EM04-N3GM627-GA06U

Datasheet
v1.1

Kingston Digital Inc.

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Contents

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Section 1

Product Overview & Packaging

Product Features

- Embedded Multi-Media storage and LPDDR3 DRAM combined into a single Multi-Chip package
- Package: JEDEC 221 ball FBGA Type –11.5 mm x 13.0 mm x (Max 1.0 mm)
- Operating temperature range: –25°C to +85°C

Introduction

The eMCP device is a Multi-Chip Package Memory device which combines JEDEC, JESD84-B51, embedded MultiMediaCard (e•MMC™) and Low Power DDR3 Synchronous Dynamic RAM (JESD209-3B). The e•MMC™ part is an embedded flash memory storage solution with an e•MMC™ interface. The e•MMC™ controller directly manages NAND flash, including error control, wear-leveling, IOPS optimization and read sensing.

The device is suitable for use in data memory of mobile communication systems to reduce not only PCB size but also power consumption. This device is available in 221-ball FBGA Type.

Table 1-1 Device Summary

Product Part number	NAND Density	DRAM Density	CH & CS DRAM	Package	Nominal Operating voltage
04EM04-N3GM627-GA06U	04GB	04Gb	1CH, 1CS	FBGA 221	VCC=3.3V, VCCQ=1.8V/3.3V VDD1 = 1.8V, VDD2, VDDQ = 1.2V

Device Block Diagram

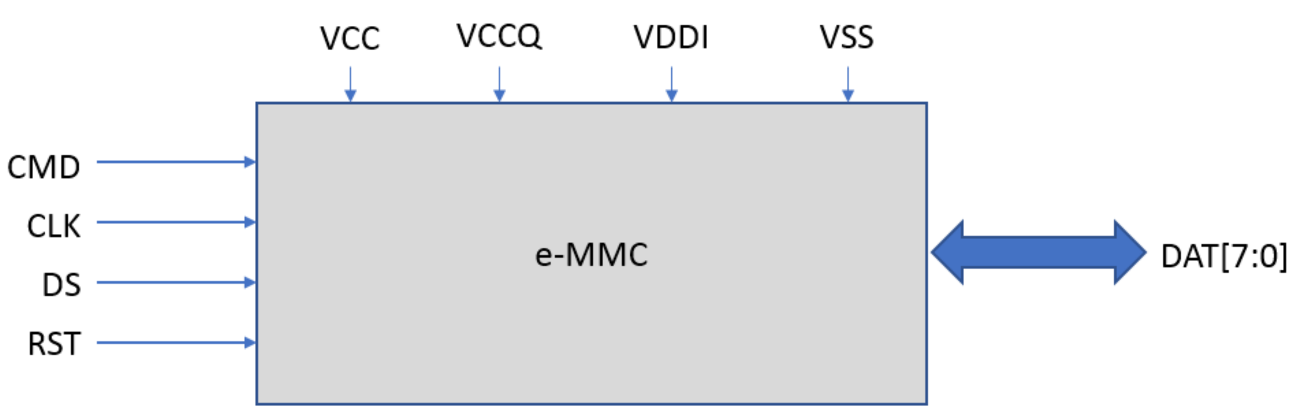

Figure 1-1 Device Block Diagram

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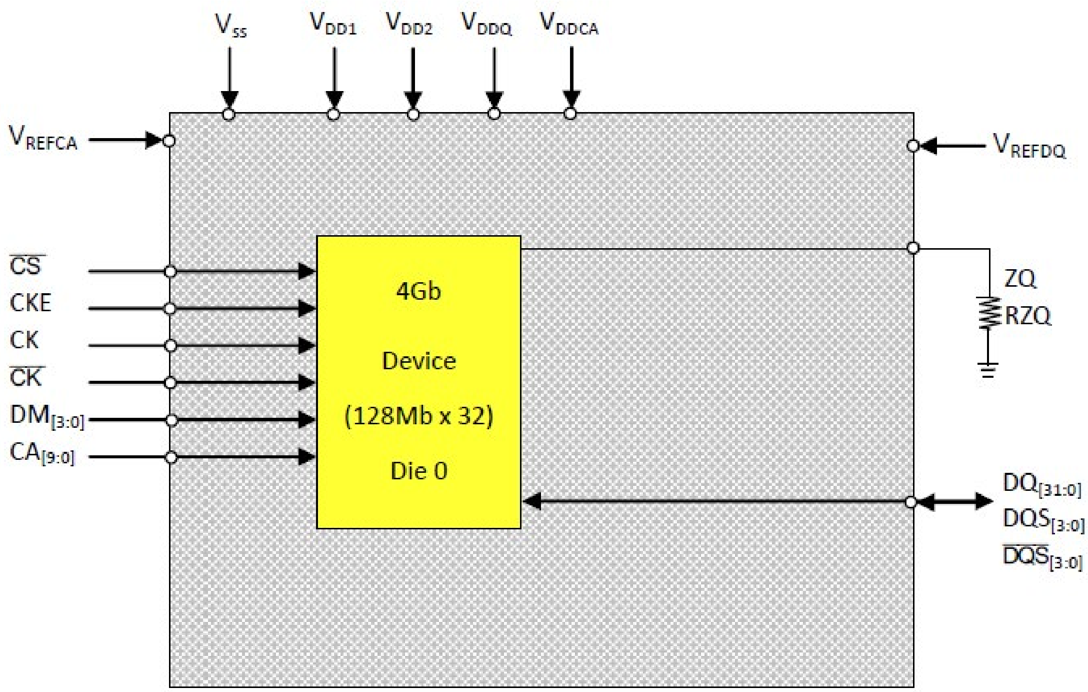

Figure 1-2 LPDDR3 Block Diagram

Operating Temperature Range

Table 1-2 Device Operating Temperature

Parameter	Rating	Unit	Note
Operating temperature	-25 ~ +85	℃	

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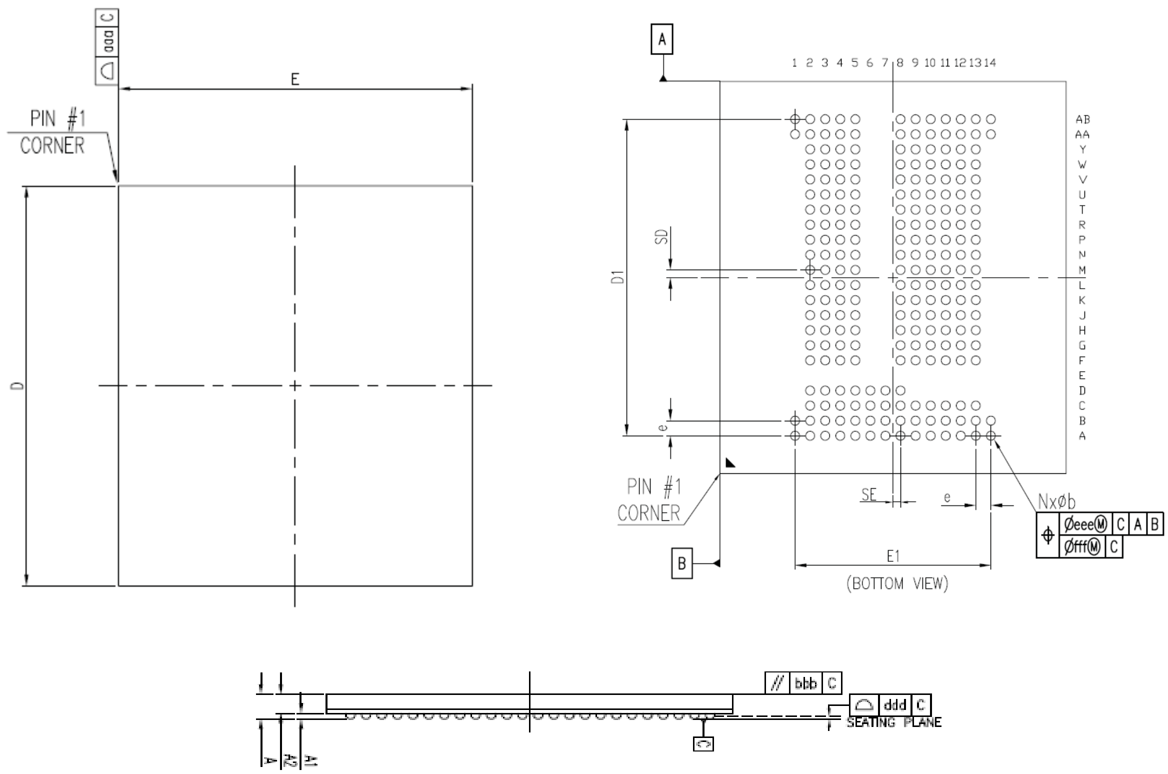
Package Mechanical

11.5 x 13.0 x (Max 1.0 mm)

Table 1-3 Device Package Dimensions



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.86	0.93	1.00	0.034	0.037	0.039
A1	0.16	0.21	0.26	0.006	0.008	0.010
A2	0.66	0.72	0.78	0.026	0.028	0.031
b	0.25	0.30	0.35	0.010	0.012	0.014
D	12.90	13.00	13.10	0.508	0.512	0.516
E	11.40	11.50	11.60	0.449	0.453	0.457
e	0.50 BSC.			0.020 BSC.		
JEDEC	MO-276(REF.)/MM					
aaa	0.15					
bbb	0.20					
ddd	0.08					
eee	0.15					
fff	0.05					

N	SE (mm)	SD (mm)	E1 (mm)	D1 (mm)
221	0.25 BSC.	0.25 BSC.	6.50 BSC.	10.50 BSC.

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Ball Assignment (221 ball)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	DNU	NC	VSSm	VCCQ	DAT6	CMD	DS	VSSm	DAT0	DAT5	VDDI	VSSm	NC	DNU	A
B	NC	VSSm	VCC	DAT7	DAT3	VCCQ	VSSm	CLK	VCCQ	DAT1	VSSm	VCC	VCC	NC	B
C		RST_n	VSSm	VCC	VSSm	DAT2	VCCQ	VSSm	DAT4	VSSm	VCCQ	VSSm	VSSm		C
D		NC	NC	NC	NC	NC	VSSm	VCC							D
E															E
F		VSS	VDD1	VDD1	VDD2			VDD2	VDD1	DQ29	DQ30	DQ31	VSS		F
G		ZQ0	ZQ1	VSS	VDD1			VSS	VDDQ	DQ26	VSS	DQ27	DQ28		G
H		CA9	VSS	VSS	VSS			VDDQ	DQS3_t	VSS	DQ24	VDDQ	DQ25		H
J		CA8	CA7	VSS	VDD2			VSS	DQS3_c	DM3	VDDQ	DQ15	VSS		J
K		VDDCA	CA6	VSS	VDD2			VSS	VSS	VDDQ	DQ13	VDDQ	DQ14		K
L		VDD2	CA5	VSS	VDD2			VDDQ	VDDQ	VSS	DQ12	VSS	DQ11		L
M		VREF (CA)	VSS	VSS	VDD2			VSS	DQS1_t	VDDQ	DQ10	VDDQ	DQ9		M
N		VDDCA	CK_c	VSS	VDD2			VSS	DQS1_c	DM1	VDDQ	DQ8	VSS		N
P		VSS	CK_t	VSS	VDD2			VDD2	VSS	ODT	VDD2	VSS	VREF (DQ)		P
R		CKE1	VSS	VSS	VDD2			VSS	DQS0_c	DM0	VDDQ	DQ7	VSS		R
T		CKE0	CS1_n	VSS	VDD2			VSS	DQS0_t	VDDQ	DQ5	VDDQ	DQ6		T
U		VDDCA	CS0_n	VSS	VDD2			VDDQ	VDDQ	VSS	DQ3	VSS	DQ4		U
V		VDDCA	CA4	VSS	VDD2			VSS	VSS	VDDQ	DQ1	VDDQ	DQ2		V
W		CA2	CA3	VSS	VDD2			VSS	DQS2_c	DM2	VDDQ	DQ0	VSS		W
Y		CA0	CA1	VSS	VSS			VDDQ	DQS2_t	VSS	DQ23	VDDQ	DQ22		Y
AA	DNU	VSS	VDD1	VSS	VDD1			VSS	VDDQ	DQ21	VSS	DQ20	DQ19	DNU	AA
AB	DNU	DNU	VDD1	VDD1	VDD2			VDD2	VDD1	DQ18	DQ17	DQ16	DNU	DNU	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

ASSIGNMENT (TOP VIEW)

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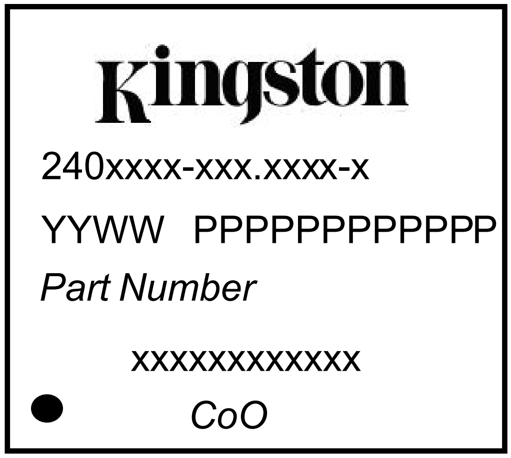
Device Marking



Line 1: Kingston logo
Line 2: 240xxxx-xxx.xxxx-x: Internal control number
Line 3: YYWW: Date code (YY– Last 2 digital of year, WW- Work week) PPPPPPPPPPPP Internal control number (within 12 digits)
Line 4: Part Number: xxxxxx-xxxxxxx
Line 5: xxxxxxxxxxxx: Internal control number (within 12 digits)
Line 6: Country of Origin (CoO): TAIWAN *or* CHINA

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Section 2

Embedded Multi-Media Card (e•MMC 5.1)

Product Features

- Packaged managed NAND flash memory with *e*•MMC™ 5.1 interface
- Backward compatible with all prior *e*•MMC™ specification revisions
- Operating voltage range:
    - VCCQ = 3.3V / 1.8 V
    - VCC = 3.3 V
- Operating Temperature (T_{case}) - 25C to +85C
- Storage Temperature -40C to +85C
- Compliant with e•MMC™ 5.1 JEDEC Standard Number JESD84-B51

e•MMC™ Specific Feature Support

- High-speed *e*•MMC™ protocol
- Variable clock frequencies of 0-200MHz
- Ten-wire bus interface (clock, 1 bit command, 8 bit data bus) with an optional hardware reset
- Supports three different data bus widths: 1 bit(default), 4 bits, 8 bits
- Bus Modes:
    - Single data transfer rate: up to 52MB/s (using 8 parallel data lines at 52MHz)
    - Dual data rate mode (DDR-104) : up to 104MB/s @ 52MHz
    - High speed, single data rate mode (HS-200) : up to 200MB/s @ 200MHz
    - High speed, dual data rate mode (HS-400) : up to 400MB/s @ 200MHz
- Supports alternate boot operation mode to provide a simple boot sequence method
- Supports SLEEP/AWAKE (CMD5)
- Host initiated explicit sleep mode for power saving
- Enhanced write protection with permanent and partial write protection options
- Multiple user data partition with enhanced attribute for increased reliability
- Error free memory access
    - Cyclic Redundancy Code (CRC) for reliable command and data communication
    - Internal error correction code (ECC) for improved data storage integrity
    - Internal enhanced data management algorithm
    - Data protection for sudden power failure during program operations
- Security
    - Secure block erase commands
    - Enhanced write protection with permanent and partial protection options
- Power off notification
- Field firmware update (FFU)
- Production state awareness
- Device health report
- Background operation control & High Priority Interrupt (HPI)
- Pre EOL information
- Optimal size

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Product Description

Kingston's e•MMC™ products conform to the JEDEC e•MMC™ 5.1 standard. These devices are an ideal universal storage solution for many commercial and industrial applications. In a single integrated packaged device, e•MMC™ combines multi-level cell (MLC) NAND flash memory with an onboard e•MMC™ controller, providing an industry standard interface to the host system. The integrated e•MMC™ controller directly manages NAND flash media which relieves the host processor of these tasks, including flash media error control, wear-leveling, NAND flash management and performance optimization. Future revision to the JEDEC e•MMC™ standard will always maintain backward compatibility. The industry standard interface to the host processor ensures compatibility across future NAND flash generations as well, easing product sustainment throughout the product life cycle.

Device Performance

Table 2-1 below provides sequential read and write speeds for all capacities. Performance numbers can vary under different operating conditions. Values are given at HS400 bus mode.

Product	Typical value	
	Read Sequential (MB/s)	Write Sequential (MB/s)
04EM04-N3GM627-GA06U	250	25

Note 1: Values given for an 8-bit bus width, running HS400 mode from KSI proprietary tool, V_{CC}=3.3V,V_{CCQ}=1.8V.
Note 2: For performance numbers under other test conditions, please contact KSI representatives.
Note 3: Performance numbers might be subject to changes without notice.

Table 2-1 - Sequential Read / Write Performance

Power Consumption

Device current consumption for various device configurations is defined in the power class fields of the EXT_CSD register. Power consumption values are summarized in Table 2-2 below.

Products	Read(mA)		Write(mA)		Standby(mA)
	$V_{CCQ(1.8V)}$	$V_{CC(3.3V)}$	$V_{CCQ(1.8V)}$	$V_{CC(3.3V)}$	
04EM04-N3GM627-GA06U	85.7	37.3	34.9	22.6	0.13

Note 1: Values given for an 8-bit bus width, a clock frequency of 200MHz DDR mode, V_{CC}= 3.3V±5%, V_{CCQ}=1.8V±5%
Note 2: Standby current is measured at Vcc=3.3V±5% ,8-bit bus width without clock frequency.
Note 3: Current numbers might be subject to changes without notice.

Table 2-2 - Device Power Consumption

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Device and Partition Capacity

The device NAND flash capacity is divided across two boot partitions (2048 KB each), a Replay Protected Memory Block (RPMB) partition (512 KB), and the main user storage area. Four additional general purpose storage partitions can be created from the user partition. These partitions can be factory preconfigured or configured in-field by following the procedure outlined in section 6.2 of the JEDEC e•MMC™ specification JESD84-B51. A small portion of the NAND storage capacity is used for the storage of the onboard controller firmware and mapping tables. Additionally, several NAND blocks are held in reserve to boost performance and extend the life of the e•MMC™ device. Table 2-3dentifies the specific capacity of each partition. This information is reported in the device EXT_CSD register. The contents of this register are also listed in the Appendix.

User density	Boot partition 1	Boot partition 2	RPMB
3,791,650,816 Bytes	2048 KB	2048 KB	512 KB

Table 2-3 - Partition Capacity

Table 2-4 - e•MMC™ Operating Voltage

Parameter	Symbol	Min	Nom	Max	Unit
Supply voltage (NAND)	V_{CC}	2.7	3.3	3.6	V
Supply voltage (I/O)	V_{CCQ} (1)	2.7	3.3	3.6	V
		1.7	1.8	1.95	V
Supply power-up for 3.3V	t_{PRUH}			35	ms
Supply power-up for 1.8V	t_{PRUL}			25	ms
Note 1：V_{CCQ} (I/O) 3.3 volt range is not supported while operating in HS200 & HS400 modes					

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e•MMC™ Bus Modes

Kingston e•MMC™ devices support all bus modes defined in the JEDEC e•MMC™ 5.1 specification. These modes are summarized in Table 2-5 below.

Table 2-5 - e•MMC™ Bus Modes

Mode	Data Rate	IO Voltage	Bus Width	CLK Frequency	Maximum Data Bus Throughput
Legacy MMC	Single	3.3V / 1.8V	1, 4, 8	0 – 26 MHz	26 MB/s
High Speed SDR	Single	3.3V / 1.8V	4, 8	0 – 52 MHz	52 MB/s
High Speed DDR	Dual	3.3V / 1.8V	4, 8	0 – 52 MHz	104 MB/s
HS200	Single	1.8V	4, 8	0 – 200 MHz	200 MB/s
HS400	Dual	1.8V	8	0 – 200 MHz	400 MB/s

Signal Description

Table 2-6a - e•MMC™ Signals

Name	Type	Description
CLK	I	Clock: Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency.
DAT[7:0]	I/O/PP	Data: These are bidirectional data channels. The DAT signals operate in push-pull mode. These bidirectional signals are driven by either the e•MMC™ device or the host controller. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the e•MMC™ host controller. The e•MMC™ device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode, the device disconnects the internal pull-ups of lines DAT1–DAT7.

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Table 2-6b - e•MMC™ Signals (continued)

Name	Type	Description
CMD	I/O/PP/OD	Command: This signal is a bidirectional command channel used for device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the e•MMC™ host controller to the e•MMC™ device and responses are sent from the device to the host.
DS	O	This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status and CMD Response are latched on the positive edge only, and don't care on the negative edge.
RST_n	I	Hardware Reset: By default, hardware reset is disabled and must be enabled in the EXT_CSD register if used. Otherwise, it can be left un-connected.
RFU	-	Reserved for future use: These pins are not internally connected. Leave floating
NC	-	Not Connected: These pins are not internally connected. Signals can be routed through these balls to ease printed circuit board design. See Kingston's Design Guidelines for further details.
VSF	-	Vendor Specific Function: These pins are not internally connected
Vddi	-	Internal Voltage Node: Note that this is not a power supply input. This pin provides access to the output of an internal voltage regulator to allow for the connection of an external Creg capacitor. See Kingston's Design Guidelines for further details.
Vcc	S	Supply voltage for core
Vccq	S	Supply voltage for I/O
Vss	S	Supply ground for core
Vssq	S	Supply ground for I/O
Note: I=Input; O=Ouput; PP=Push-Pull; OD=Open_Drain; NC=Not Connected(or logical high); S=Power Supply		

Design Guidelines

Design guidelines are outlined in a separate document. Contact your KSI Representative for more information.

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Card Identification Register (CID)

The Card Identification (CID) register is a 128-bit register that contains device identification information used during the *e*•MMC™ protocol device identification phase. Refer to JEDEC Standard Specification No.JESD84-B51 for details.

Field	Bits	Value
MID	[127:120]	0x70
reserved	[119:114]	0x00
CBX	[113:112]	0x01
OID	[111:104]	0x00
PNM	[103:56]	EE4MD4
PRV	[55:48]	0x06
PSN	[47:16]	Random
MDT	[15:8]	month, year
CRC	[7:1]	Follows JEDEC Standard
reserved	[0:0]	0x01

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Card Specific Data Register [CSD]

The Card-Specific Data (CSD) register provides information on how to access the contents stored in *e*•MMC™. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

Field	Bits	Value
CSD_Structure	[127:126]	0x03 (V2.0)
SPEC_VER	[125:122]	0x04 (V4.0~4.2)
reserved	[121:120]	0x00
TAAC	[119:112]	0x4F (40ms)
NSAC	[111:104]	0x01
TRAN_SPEED	[103:96]	0x32 (26Mbit/s)
CCC	[95:84]	0x8F5
READ_BL_LEN	[83:80]	0x09 (512 Bytes)
READ_BL_PARTIAL	[79:79]	0x00
WRITE_BLK_MISALIGN	[78:78]	0x00
READ_BLK_MISALIGN	[77:77]	0x00
DSR_IMP	[76:76]	0x00
reserved	[75:74]	0x00
C_SIZE	[73:62]	0xFFF
VDD_R_CURR_MIN	[61:59]	0x07 (100mA)
VDD_R_CURR_MAX	[58:56]	0x07 (200mA)
VDD_W_CURR_MIN	[55:53]	0x07 (100mA)
VDD_W_CURR_MAX	[52:50]	0x07 (200mA)
C_SIZE_MULT	[49:47]	0x07 (512 Bytes)
ERASE_GRP_SIZE	[46:42]	0x1F
ERASE_GRP_MULT	[41:37]	0x1F
WP_GRP_SIZE	[36:32]	0x07
WP_GRP_ENABLE	[31:31]	0x01
DEFAULT_ECC	[30:29]	0x00

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Field	Bits	Value
R2W_FACTOR	[28:26]	0x02
WRITE_BL_LEN	[25:22]	0x09 (512 Bytes)
WRITE_BL_PARTIAL	[21:21]	0x00
reserved	[20:17]	0x00
CONTENT_PROT_APP	[16:16]	0x00
FILE_FORMAT_GRP	[15:15]	0x00
COPY	[14:14]	0x00
PERM_WRITE_PROTECT	[13:13]	0x00
TMP_WRITE_PROTECT	[12:12]	0x00
FILE_FORMAT	[11:10]	0x00
ECC	[9:8]	0x00
CRC	[7:1]	Follow JEDEC Standard
reserved	[0:0]	0x01

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Extended Card Specific Data Register [EXT_CSD]

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to section 7.4 of the JEDEC Standard Specification No.JESD84-B51.

Field	Byte	Value
Reserved	[511:506]	0
EXT_SECURITY_ERR	[505:505]	0x00
S_CMD_SET	[504:504]	0x01
HPI_FEATURES	[503:503]	0x01
BKOPS_SUPPORT	[502:502]	0x01
MAX_PACKED_READS	[501:501]	0x3C
MAX_PACKED_WRITES	[500:500]	0x3C
DATA_TAG_SUPPORT	[499:499]	0x01
TAG_UNIT_SIZE	[498:498]	0x03
TAG_RES_SIZE	[497:497]	0x00
CONTEXT_CAPABILITIES	[496:496]	0x05
LARGE_UNIT_SIZE_M1	[495:495]	0x03
EXT_SUPPORT	[494:494]	0x03
SUPPORTED_MODES	[493:493]	0x01
FFU_FEATURES	[492:492]	0x00
OPERATION_CODE_TIMEOUT	[491:491]	0x00
FFU_ARG	[490:487]	65535
BARRIER_SUPPORT	[486:486]	0x01
Reserved	[485:309]	0
CMDQ_SUPPORT	[308:308]	0x00
CMDQ_DEPTH	[307:307]	0x00
Reserved	[306:306]	0x00

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Field	Byte	Value
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	0
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	0
DEVICE_LIFE_TIME_EST_TYP_B	[269:269]	0x01
DEVICE_LIFE_TIME_EST_TYP_A	[268:268]	0x01
PRE_EOL_INFO	[267:267]	0x01
OPTIMAL_READ_SIZE	[266:266]	0x01
OPTIMAL_WRITE_SIZE	[265:265]	0x04
OPTIMAL_TRIM_UNIT_SIZE	[264:264]	0x01
DEVICE_VERSION	[263:262]	0
FIRMWARE_VERSION	[261:254]	0x06
PWR_CL_DDR_200_360	[253:253]	0x00
CACHE_SIZE	[252:249]	512
GENERIC_CMD6_TIME	[248:248]	0x19
POWER_OFF_LONG_TIME	[247:247]	0xFF
BKOPS_STATUS	[246:246]	0x00
CORRECTLY_PRG_SECTORS_NUM	[245:242]	0
INI_TIMEOUT_AP	[241:241]	0x64
CACHE_FLUSH_POLICY	[240:240]	0x01
PWR_CL_DDR_52_360	[239:239]	0x00
PWR_CL_DDR_52_195	[238:238]	0x00
PWR_CL_200_195	[237:237]	0x00
PWR_CL_200_130	[236:236]	0x00
MIN_PERF_DDR_W_8_52	[235:235]	0x00
MIN_PERF_DDR_R_8_52	[234:234]	0x00
Reserved	[233:233]	0x00
TRIM_MULT	[232:232]	0x11
SEC_FEATURE_SUPPORT	[231:231]	0x55
SEC_ERASE_MULT	[230:230]	0x1E
SEC_TRIM_MULT	[229:229]	0x1E

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Field	Byte	Value
BOOT_INFO	[228:228]	0x07
Reserved	[227:227]	0x00
BOOT_SIZE_MULT	[226:226]	0x10
ACC_SIZE	[225:225]	0x06
HC_ERASE_GRP_SIZE	[224:224]	0x01
ERASE_TIMEOUT_MULT	[223:223]	0x11
REL_WR_SEC_C	[222:222]	0x01
HC_WP_GRP_SIZE	[221:221]	0x08
S_C_VCC	[220:220]	0x08
S_C_VCCQ	[219:219]	0x08
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218:218]	0x14
S_A_TIMEOUT	[217:217]	0x13
SLEEP_NOTIFICATION_TIME	[216:216]	0x0F
SEC_COUNT	[215:212]	7405568
SECURE_WP_INFO	[211:211]	0x01
MIN_PERF_W_8_52	[210:210]	0x08
MIN_PERF_R_8_52	[209:209]	0x08
MIN_PERF_W_8_26_4_52	[208:208]	0x08
MIN_PERF_R_8_26_4_52	[207:207]	0x08
MIN_PERF_W_4_26	[206:206]	0x08
MIN_PERF_R_4_26	[205:205]	0x08
Reserved	[204:204]	0x00
PWR_CL_26_360	[203:203]	0x00
PWR_CL_52_360	[202:202]	0x00
PWR_CL_26_195	[201:201]	0x00
PWR_CL_52_195	[200:200]	0x00
PARTITION_SWITCH_TIME	[199:199]	0x03
OUT_OF_INTERRUPT_TIME	[198:198]	0x04
DRIVER_STRENGTH	[197:197]	0x1F

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Field	Byte	Value
DEVICE_TYPE	[196:196]	0x57
Reserved	[195:195]	0x00
CSD_STRUCTURE	[194:194]	0x02
Reserved	[193:193]	0x00
EXT_CSD_REV	[192:192]	0x08
CMD_SET	[191:191]	0x00
Reserved	[190:190]	0x00
CMD_SET_REV	[189:189]	0x00
Reserved	[188:188]	0x00
POWER_CLASS	[187:187]	0x00
Reserved	[186:186]	0x00
HS_TIMING	[185:185]	0x01
STROBE_SUPPORT	[184:184]	0x01
BUS_WIDTH	[183:183]	0x02
Reserved	[182:182]	0x00
ERASED_MEM_CONT	[181:181]	0x00
Reserved	[180:180]	0x00
PARTITION_CONFIG	[179:179]	0x00
BOOT_CONFIG_PROT	[178:178]	0x00
BOOT_BUS_CONDITIONS	[177:177]	0x00
Reserved	[176:176]	0x00
ERASE_GROUP_DEF	[175:175]	0x00
BOOT_WP_STATUS	[174:174]	0x00
BOOT_WP	[173:173]	0x00
Reserved	[172:172]	0x00
USER_WP	[171:171]	0x00
Reserved	[170:170]	0x00
FW_CONFIG	[169:169]	0x00
RPMB_SIZE_MULT	[168:168]	0x04

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Field	Byte	Value
WR_REL_SET	[167:167]	0x00
WR_REL_PARAM	[166:166]	0x15
SANITIZE_START	[165:165]	0x00
BKOPS_START	[164:164]	0x00
BKOPS_EN	[163:163]	0x00
RST_n_FUNCTION	[162:162]	0x00
HPI_MGMT	[161:161]	0x00
PARTITIONING_SUPPORT	[160:160]	0x07
MAX_ENH_SIZE_MULT	[159:157]	452
PARTITIONS_ATTRIBUTE	[156:156]	0x00
PARTITION_SETTING_COMPLETED	[155:155]	0x00
GP_SIZE_MULT_4	[154:152]	0
GP_SIZE_MULT_3	[151:149]	0
GP_SIZE_MULT_2	[148:146]	0
GP_SIZE_MULT_1	[145:143]	0
ENH_SIZE_MULT	[142:140]	0
ENH_START_ADDR	[139:136]	0
Reserved	[135:135]	0x00
SEC_BAD_BLK_MGMNT	[134:134]	0x00
PRODUCTION_STATE_AWARENESS	[133:133]	0x00
TCASE_SUPPORT	[132:132]	0x00
PERIODIC_WAKEUP	[131:131]	0x00
PROGRAM _CID_CSD_DDR_SUPPORT	[130:130]	0x01
Reserved	[129:128]	0
VENDOR_SPECIFIC_FIELD	[127:67]	N/A
ERROR_CODE	[66:65]	0
ERROR_TYPE	[64:64]	0x00
NATIVE_SECTOR_SIZE	[63:63]	0x00
USE_NATIVE_SECTOR	[62:62]	0x00

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Field	Byte	Value
DATA_SECTOR_SIZE	[61:61]	0x00
INI_TIMEOUT_EMU	[60:60]	0x00
CLASS_6_CTRL	[59:59]	0x00
DYNCAP_NEEDED	[58:58]	0x00
EXCEPTION_EVENTS_CTRL	[57:56]	0
EXCEPTION_EVENTS_STATUS	[55:54]	0
EXT_PARTITIONS_ATTRIBUTE	[53:52]	0
CONTEXT_CONF	[51:37]	0
PACKED_COMMAND_STATUS	[36:36]	0x00
PACKED_FAILURE_INDEX	[35:35]	0x00
POWER_OFF_NOTIFICATION	[34:34]	0x00
CACHE_CTRL	[33:33]	0x00
FLUSH_CACHE	[32:32]	0x00
BARRIER_CTRL	[31:31]	0x00
MODE_CONFIG	[30:30]	0x00
MODE_OPERATION_CODES	[29:29]	0x00
Reserved	[28:27]	0
FFU_STATUS	[26:26]	0x00
PRE_LOADING_DATA_SIZE	[25:22]	0
MAX_PRE_LOADING_DATA_SIZE	[21:18]	3670016
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17:17]	0x01
SECURE_REMOVAL_TYPE	[16:16]	0x09
CMDQ_MODE_EN	[15:15]	0x00
Reserved	[14:0]	0

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Section 3

Low Power Double Data Rate 3

(LPDDR3 SDRAM)

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4Gb(4Gbx1) SDP LPDDR3 SDRAM

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Product Features

LPDDR3

- Ultra-low voltage core and I/O power supplies
  - – VDD1 = 1.70–1.95V; 1.8V nominal
  - – VDD2 = 1.14–1.30V; 1.2V nominal
  - – VDDQ = 1.14–1.30V; 1.2V nominal

- Organization
  - – 16M words × 32 bits × 8 banks

- JEDEC LPDDR3-compliant
- 4KB page size (×32 bits)
  - – Row address: R0 to R13 (×32 bits)
  - – Column address: C0 to C9
- Frequency range
  - – 1600Mbps Max
- 8n prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD/ADR entry
- Bidirectional/differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =8)
- Directed per-bank refresh for concurrent bank operation and ease for command scheduling
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- Operating temperature range
  - – TC = –25°C to +85°C

Product Description

The LPDDR3 portion of the device is fully compatible with the JEDEC Standard Specification No.JESD209-3B. This datasheet describes the key and specific features of the LPDDR3. Any additional information required to interface the device to a host system and all the practical methods for device detection and access can be found in the proper sections of the JEDEC Standard Specification.

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LPDDR3 Interface

Pin Function and Descriptions

Table 3-1 – Pin Function and Descriptions

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See Command Truth Table for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. See Command Truth Table for command code descriptions. CS_n is sampled at the positive Clock edge.
CA0 – CA9	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See Command Truth Table for command code descriptions.
DQ0 – DQ15 (x16) DQ0 – DQ31(x32)	I/O	Data Inputs/Output: Bi-directional data bus
DQS0_t,DQS0_c, DQS1_t,DQS1_c(x16) DQS0_t- DQS3_t, DQS0_c -DQS3_c (x32)	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7; DQS1_t and DQS1_c to the data on DQ8 - DQ15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0 - DQ7, DQS1_t and DQS1_c to the data on DQ8 - DQ15, DQS2_t and DQS2_c to the data on DQ16 - DQ23, DQS3_t and DQS3_c to the data on DQ24 - DQ31.
DM0-DM1 (x16) DM0 - DM3 (x32)	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS_t (or DQS_c). For x16 and x32 devices, DM0 is the input data mask signal for the data on DQ0-7. DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
ODT	Input	**On-Die Termination**: This signal enables and disables termination on the DRAM DQ bus according to the specified mode register settings.
VDD1	Supply	**Core Power Supply 1**
VDD2	Supply	**Core Power Supply 2**
VDDCA	Supply	**Input Receiver Power Supply:** Power supply for CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
VDDQ	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
VREF(CA)	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA0-9, CKE, CS_n, CK_t, and CK_c input buffers.
VREF(DQ)	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
VSS	Supply	**Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

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Simplified State Diagram

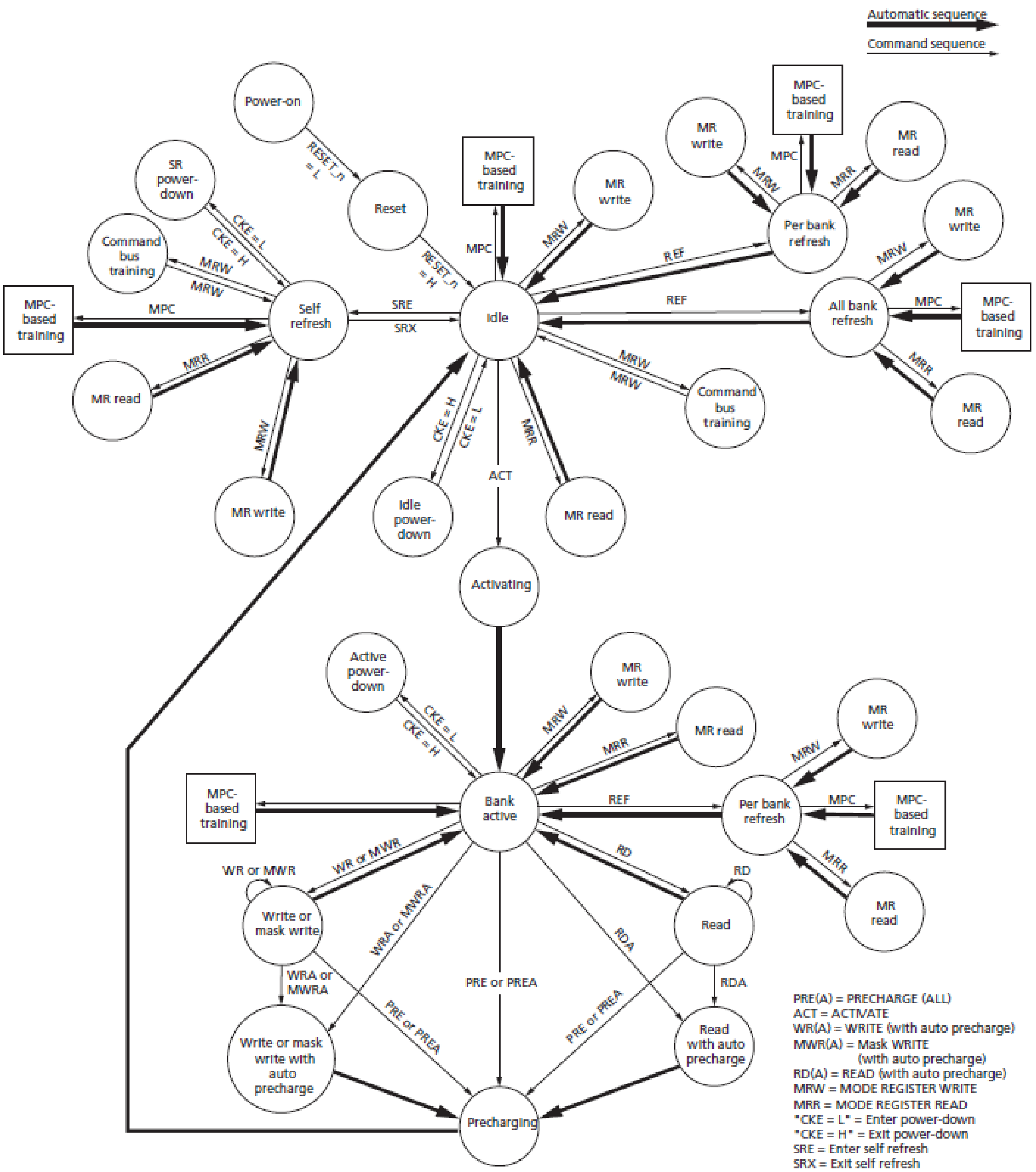

Figure 3-1 — Simplified Bus Interface State Diagram

Notes:

1. From the self-refresh state, the device can enter power-down, MRR, MRW, or any of the training modes initiated with the MPC command. See the Self Refresh section.
2. All banks are pre-charged in the idle state.
3. In the case of using an MRW command to enter a training mode, the state machine will not automatically return to the idle state at the conclusion of training.
4. In the case of an MPC command to enter a training mode, the state machine may not automatically return to the idle state at the conclusion of training. See the applicable training section for more information.
5. This diagram is intended to provide an overview of the possible state transitions and commands to control

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them; however, it does not contain the details necessary to operate the device. In particular, situations involving more than one bank are not captured in complete detail.
6. States that have an "automatic return" and can be accessed from more than one prior state (that is, MRW from either idle or active states) will return to the state where they were initiated (that is, MRW from idle will return to idle).
7. The RESET pin can be asserted from any state and will cause the device to enter the reset state. The diagram shows RESET applied from the power-on and idle states as an example, but this should not be construed as a restriction on RESET.
8. MRW commands from the active state cannot change operating parameters of the device that affect timing. Mode register fields which may be changed via MRW from the active state include: MR1-OP[3:0], MR1-OP[7], MR3-OP[7:6], MR10-OP[7:0], MR11-OP[7:0], MR13-OP[5], MR15-OP[7:0], MR16-OP[7:0], MR17-OP[7:0], MR20-OP[7:0], and MR22-OP[4:0].

Electrical Conditions

All voltages are referenced to VSS (GND)

- Execute power-up and Initialization sequence before proper device operation is achieved.
- Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the DDR2 Mobile RAM Device must be powered down and then restarted through the specialized initialization sequence before normal operation can continue.

Absolute Maximum Ratings

Table 3-2 Absolute Maximum Ratings

Parameter	Symbol	min.	max.	Unit	Note
VDD1 supply voltage relative to VSS	VDD1	-0.4	2.3	V	2
VDD2 supply voltage relative to VSS	VDD2	-0.4	1.6	V	2
VDDCA supply voltage relative to VSSCA	VDDCA	-0.4	1.6	V	2, 3
VDDQ supply voltage relative to VSSQ	VDDQ	-0.4	1.6	V	2, 4
Voltage on any ball relative to VSS	VIN, VOUT	-0.4	1.6	V	
Storage Temperature	TSTG	-55	125	°C	5

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Refer “Power-up, initialization and Power-Off “for relationship between power supplies
3. VREFCA ≤ 0.6 x VDDCA; however, VREFCA may be ≥ VDDCA provided that VREFCA ≤ 300mV.
4. VREFDQ ≤ 0.7 × VDDQ; however, VREFDQ may be ≥ VDDQ provided that VREFDQ ≤ 300mV.
5. Storage Temperature is the case surface temperature on the center/top side of the DDR3 Mobile RAM Device.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

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Recommended DC Operating Conditions

Table 3-3 Recommended DC Operating Conditions (TC = -25°C to +85°C)

Parameter	Symbol	min.	Typ.	max.	Unit	Note
Core Power1	VDD1	1.7	1.8	1.95	V	1
Core Power2,	VDD2	1.14	1.2	1.3	V	1,2
Input Buffer Power	VDDCA	1.14	1.2	1.3	V	1,2
I/O Buffer Power	VDDQ	1.14	1.2	1.3	V	2

Notes: 1. VDD1 uses significantly less power than VDD2.
2. The voltage range is for DC voltage only. DC voltage is the voltage supplied at the DRAM and is inclusive of all noise up to 1 MHz at the DRAM package ball.

AC and DC Input Levels for Single-Ended CA/CS Signals

Table 3-4 Single-Ended AC and DC Input Levels for CA/CS Inputs

Parameter	Symbol	Speed	min.	max.	Unit	Note
AC input logic high	VIHCA(AC)	1333 / 1600	VREF + 0.150	Note 2	V	1, 2
AC input logic low	VILCA(AC)	1333 / 1600	Note 2	VREF – 0.150	V	1, 2
DC input logic high	VIHCA(DC)	1333 / 1600	VREF + 0.100	VDDCA	V	1
DC input logic low	VILCA(DC)	1333 / 1600	VSS	VREF – 0.100	V	1
Reference Voltage for CA/CS inputs	VREFCA(DC)	1333 / 1600	0.49 ×VDDCA	0.51 ×VDDCA	V	3, 4

Notes: 1. For CA/CS input only pins. VREF = VREFCA(DC).
2. Refer "Overshoot and Undershoot Specifications".
3. The ac peak noise on VREFCA may not allow VREFCA to deviate from VREFCA(DC) by more than ± 1% VDDCA (for reference: 43dditio. ± 12 mV).
4. For reference: 43dditio. VDDCA/2 ± 12 mV.

AC and DC Input Levels for CKE

Table 3-5 Single-Ended AC and DC Input Levels for CKE

Parameter	Symbol	min.	max.	Unit	Note
CKE Input High Level	VIHCKE	0.65 × VDDCA	Note 1	V	1
CKE Input Low Level	VILCKE	Note 1	0.35 × VDDCA	V	1

Notes: 1. Refer "Overshoot and Undershoot Specifications".

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AC and DC Input Levels for Single-Ended Data Signals

Table 3-6 Single-Ended AC and DC Input Levels for DQ and DM

Parameter	Symbol	Speed	min.	max.	Unit	Note
AC input logic high	VIHDQ(AC)	1333/1600	VREF + 0.150	Note 2	V	1, 2 ,5
AC input logic low	VILDQ(AC)	1333/1600	Note 2	VREF – 0.150	V	1, 2 ,5
DC input logic high	VIHDQ(DC)	1333/1600	VREF + 0.100	VDDQ	V	1
DC input logic low	VILDQ(DC)	1333/1600	VSSQ	VREF – 0.100	V	1
Reference Voltage for DQ, DM inputs	VREFDQ(DC) (DQ ODT disable)	1333/1600	0.49 × VDDQ	0.51 × VDDQ	V	3, 4
Reference Voltage for DQ, DM inputs	VREFDQ(DC) (DQ ODT enable)	1333/1600	VODTR/2 – 0.01 * VDDQ	VODTR/2 + 0.01 * VDDQ	V	3,5,6

1. For DQ input only pins. VREF = VREFDQ(DC).
2. Refer "Overshoot and Undershoot Specifications".
3. The ac peak noise on VREFDQ may not allow VREFDQ to deviate from VREFDQ(DC) by more than ± 1% VDDQ (for reference: dditio. ± 12 mV).
4. For reference: 7alibra. VDDQ/2 +/- 12 mV.
5. For reference: 7alibra. VODTR/2 +/- 12 mV.
6. The nominal mode register programmed value for RODT and the nominal controller output impedance RON are used for the calculation of VODTR. For testing purposes a controller RON value of 50 Ω is used.

$$V_{ODTR} = \frac{2R_{ON} + R_{TT}}{R_{ON} + R_{TT}} \times V_{DDQ}$$

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VREF Tolerances

The dc-tolerance limits and ac-noise limits for the reference voltages VREFCA and VREFDQ are illustrated in Figure 3-2. It shows a valid reference voltage VREF(t) as a function of time. (VREF stands for VREFCA and VREFDQ likewise).

VDD stands for VDD2 for VREFCA and VDDQ for VREFDQ. VREF(DC) is the linear average of VREF(t) over a very long period of time (e.g. 1 sec) and is specified as a fraction of the linear average of VDDQ or VDD2 also over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table 3-5. Furthermore VREF(t) may temporarily deviate from VREF(DC) by no more than ± 1% VDD. VREF(t) cannot track noise on VDDQ or VDD2 if this would send VREF outside these specification.

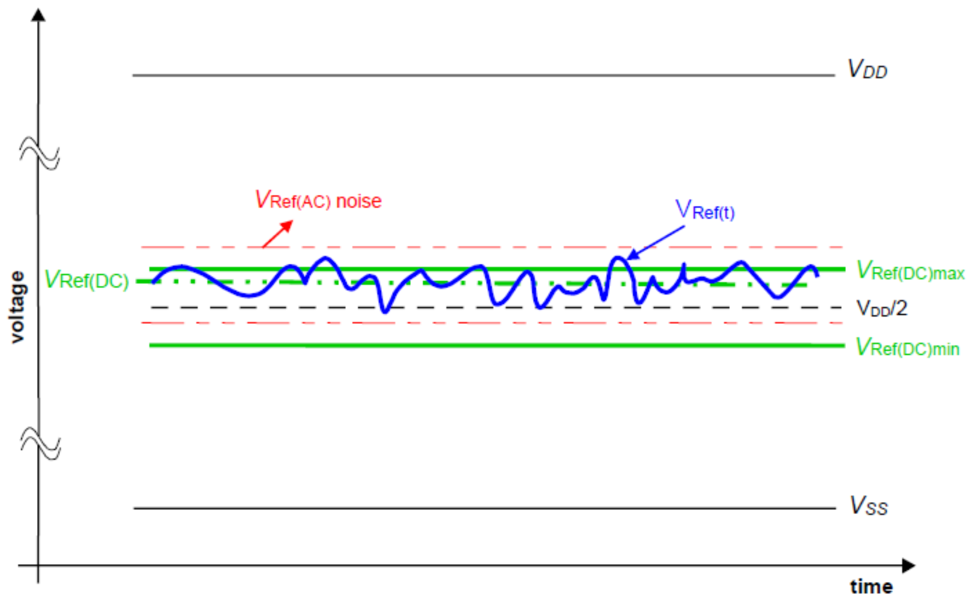

Figure 3-2 — Illustration of VREF(DC) Tolerance and VREF AC-noise Limits

The voltage levels for setup and hold time measurements VIH(AC), VIH(DC), VIL(AC) and VIL(DC) are dependent on VREF."VREF " shall be understood as VREF(DC), as defined in Figure 3-2.

This clarifies that dc-variations of VREF affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. Devices will function correctly with appropriate timing deratings with VREF outside these specified levels so long as VREF is maintained between 0.44 × VDDQ (or VDD2) and 0.56 × VDDQ (or VDD2) and so long as the controller achieves the required single-ended AC and DC input levels from instantaneous VREF . Therefore, system timing and voltage budgets need to account for VREF deviations outside of this range.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with VREF AC-noise. Timing and voltage effects due to AC-noise on VREF up to the specified limit (± 1% of VDD) are included in DRAM timings and their associated deratings.

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Input Signal

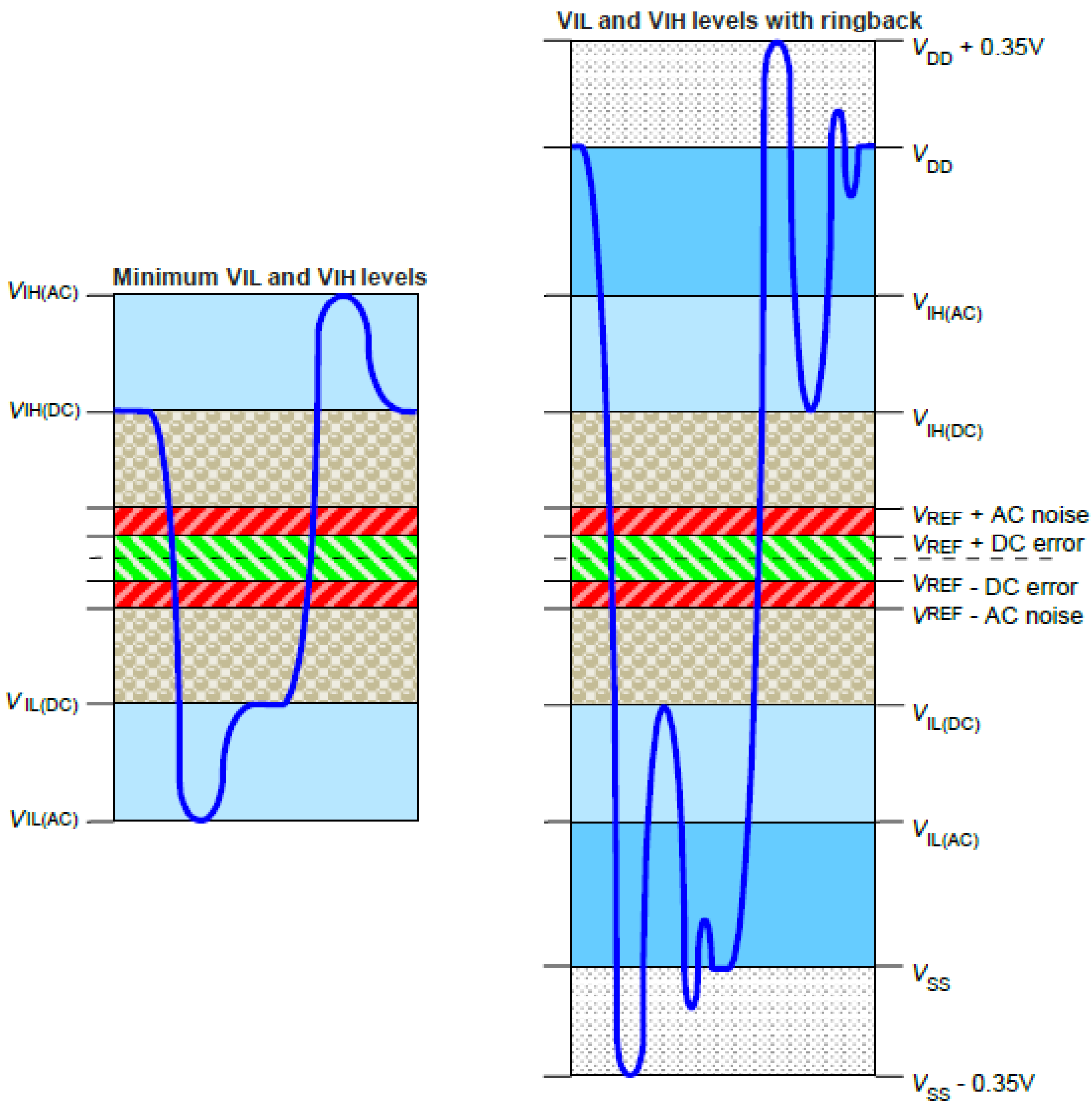

Figure 3-3 — LPDDR3 Input Signal

Notes: 1. Numbers reflect nominal values.
2. For CA0-9, CK_t, CK_c,and CS_n, VDD stands for VDDCA. For DQ, DM, DQS_t, DQS_c and ODT, VDD stands for VDDQ.
3. For CA0-9, CK_t, CK_c, and CS_n, VSS stands for VSSCA. For DQ, DM, DQS_t, DQS_c and ODT VSS stands for VSS.

AC and DC Logic Input Levels for Differential Signals

Differential Signal Definition

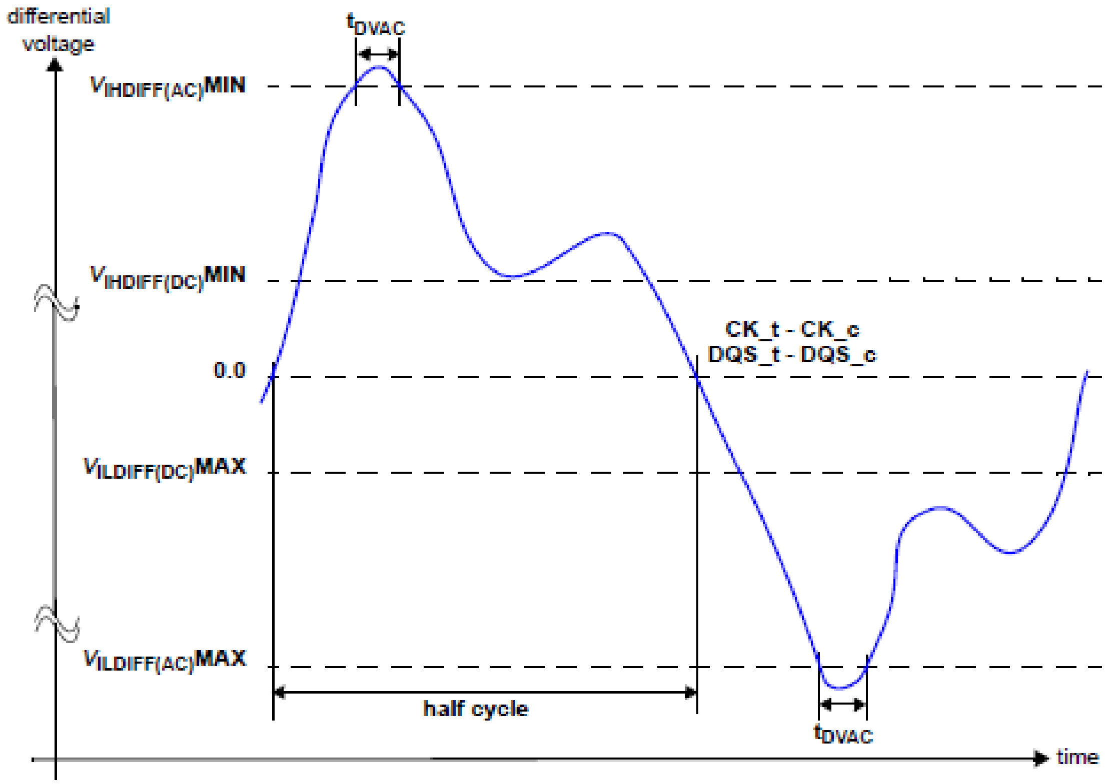

Figure 3-4 Definition of Differential AC-swing and "Time above AC-level" tDVAC

Differential Swing Requirements for Clock (CK_t – CK_c) and Strobe (DQS_t – DQS_c)

Table 3-7 Differential AC and DC Input Levels

Parameter	Symbol	min.	max.	Unit	Note
Differential input high	VIHdiff(DC)	2 × (VIH(DC) – VREF)	Note 3	V	1
Differential input low	VILdiff(DC)	Note 3	2 × (VIL(DC) – VREF)	V	1
Differential input high AC	VIHdiff(AC)	2 × (VIH(AC) – VREF)	Note 3	V	2
Differential input low AC	VILdiff(AC)	Note 3	2 × (VIL(AC) – VREF)	V	2

Notes:

1. Used to define a differential signal slew-rate. For CK_t – CK_c use VIH/VIL(dc) of CA and VREFCA; for DQS_t – DQS_c, use VIH/VIL(dc) of DQs and VREFDQ; if a reduced dc-high or dc-low level is used for a signal group, then the reduced level applies also here.
2. For CK_t – CK_c use VIH/VIL(ac) of CA and VREFCA; for DQS_t – DQS_c, use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS_t, and DQS_c need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single-ended signals as well as the limitations for overshoot and undershoot

   For CK_t and CK_c, Vref = VrefCA(DC). For DQS_t and DQS_c, Vref = VrefDQ(DC)

Table 3-8 Allowed Time Before Ringback (tDVAC) for CK_t – CK_c and DQS_t – DQS_c

Slew Rate [V/ns]	**tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV 1333Mbps**	**tDVAC [ps] @ |VIH/Ldiff(ac)| = 300mV 1600Mbp**
	min.	min.
> 4.0	58	48
8.0	58	48
7.0	56	46
6.0	53	43
5.0	50	40
4.0	45	35
3.0	37	27
< 3.0	37	27

Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK_t, DQS_t, CK_c, or DQS_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle.

DQS_t, DQS_c shall meet VSEH(ac)min / VSEL(ac)max in every half-cycle preceeding and following a valid transition. Note that the applicable ac-levels for CA and DQ's are different per speed-bin.

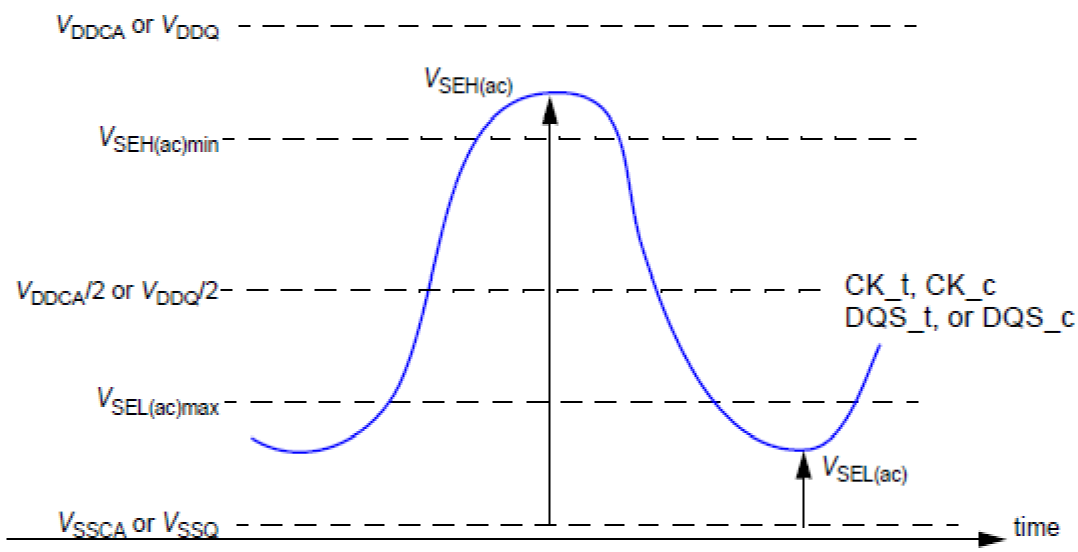

Figure 3-5 Single-ended Requirement for Differential Signals.

Note that while CA and DQ signal requirements are with respect to VREF, the single-ended components of differential signals have a requirement with respect to VDDQ/2 for DQS_t, DQS_c and VDDCA/2 for CK_t, CK_c; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSEL(AC)max, VSEH(AC)min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 3-9 Single-ended Levels for CK_t, DQS_t, CK_c, DQS_c

Parameter	Symbol	min.	max.	Unit	Note
Single-ended high-level for strobes	VSEH(AC150)	(VDDQ / 2) + 0.150	Note 3	V	1, 2
Single-ended high-level for CK_t, CK_c		(VDDCA / 2) + 0.150	Note 3	V	1, 2
Single-ended low-level for strobes	VSEL(AC150)	Note 3	(VDDQ / 2) – 0.150	V	1, 2
Single-ended low-level for CK_t, CK_c		Note 3	(VDDCA / 2) – 0.150	V	1, 2
Single-ended high-level for strobes	VSEH(AC135)	(VDDQ / 2) + 0.135	Note 3	V	1, 2
Single-ended high-level for CK_t, CK_c		(VDDCA / 2) + 0.135	Note 3	V	1, 2
Single-ended low-level for strobes	VSEL(AC135)	Note 3	(VDDQ / 2) – 0.135	V	1, 2
Single-ended low-level for CK_t, CK_c		Note 3	(VDDCA / 2) – 0.135	V	1, 2

Notes: 1. For CK_t, CK_c use VSEH/VSEL(AC) of CA; for strobes (DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c) use VIH/VIL(AC) of DQs.
2. VIH(AC)/VIL(AC) for DQs is based on VREFDQ; VSEH(AC)/VSEL(AC) for CA is based on VREFCA; if a reduced Achigh or AC-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however the single-ended signals CK_t, CK_c, DQS0_t, DQS0_c, DQS1_t, DQS1_c, DQS2_t, DQS2_c, DQS3_t, DQS3_c need to be within the respective limits (VIH(DC) max, VIL(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specifications".

Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK_t, CK_c and DQS_t, DQS_c) must meet the requirements in Table 3-10. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

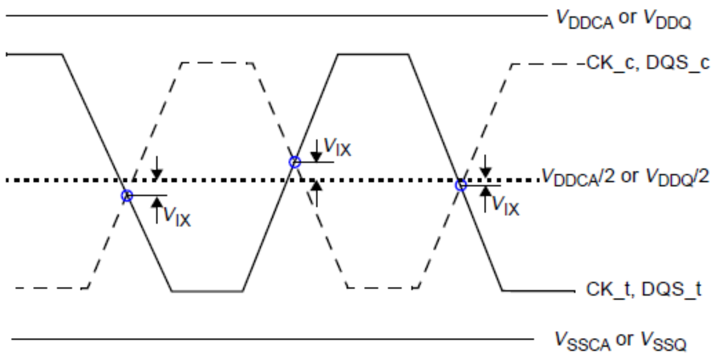

Figure 3-6 VIX Definition

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Table 3-10 Cross Point Voltage for Differential Input Signals (CK, DQS)

Parameter	Symbol	min.	max.	Unit	Note
Differential Input Cross Point Voltage relative to VDDCA/2 for CK_t, CK_c	VIXCA	-120	120	mV	1, 2
Differential Input Cross Point Voltage relative to VDDQ/2 for DQS_t, DQS_c	VIXDQ	-120	120	mV	1, 2

Notes:

1. The typical value of VIX(AC) is expected to be about 0.5 × VDD of the transmitting device, and VIX(AC) is expected to track variations in VDD. VIX(AC) indicates the voltage at which differential input signals must cross.
2. For CK_t and CK_c, VREF = VREFCA(DC). For DQS_t and DQS_c, VREF = VREFDQ(DC).

Slew Rate Definitions for Single-Ended Input Signals

See "CA and CS_c Setup, Hold and Derating" for single-ended slew rate definitions for address and command signals.
See "Data Setup, Hold and Slew Rate Derating" for single-ended slew rate definitions for data signals.

Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK_t, CK_c and DQS_t, DQS_c) are defined and measured as shown in Table 3-11 and Figure 3-7.

Table 3-11 Differential Input Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential input slew rate for rising edge (CK_t – CK_c and DQS_t – DQS_c).	VILdiffmax	VIHdiffmin	[VIHdiffmin – VILdiffmax] / DeltaTRdiff
Differential input slew rate for falling edge (CK_t – CK_c and DQS_t – DQS_c).	VIHdiffmin	VILdiffmax	[VIHdiffmin – VILdiffmax] / DeltaTFdiff

Note: 1. The differential signal (i.e. CK_t – CK_c and DQS_t – DQS_c) must be linear between these thresholds.

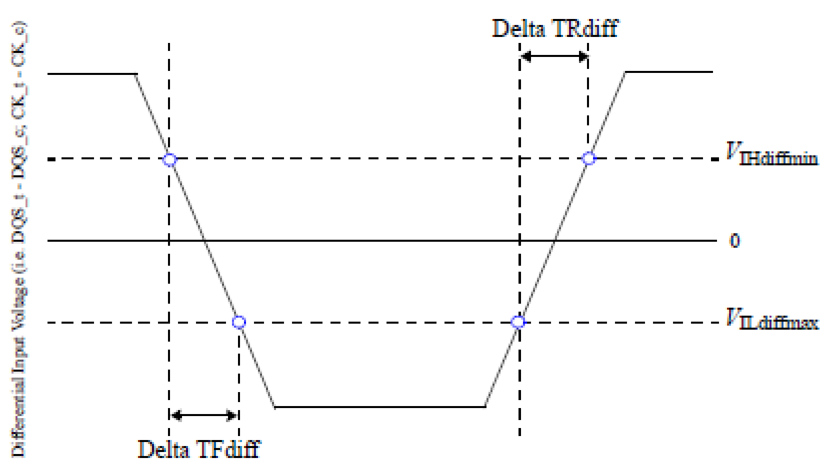

Figure 3-7 — Differential Input Slew Rate Definition for DQS_t, DQS_c and CK_t, CK_c

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Single Ended AC and DC Output Levels

Table 3-12 shows the output levels used for measurements of single ended signals.

Table 3-12 Single-ended AC and DC Output Levels

Parameter	Symbol		Value	Unit	Note
DC output high measurement level (for IV curve linearity)	VOH(DC)		0.9 × VDDQ	V	1
DC output low measurement level (for IV curve linearity)	VOL(DC)		0.1 × VDDQ	V	2
DC output low measurement level (for IV curve linearity)	VOL(DC) ODT enabled		VDDQ x [0.1 + 0.9 x (RON / (RTT + RON))]	V	3
AC output high measurement level (for output slew rate)	VOH(AC)		VREFDQ + 0.12	V	
AC output low measurement level (for output slew rate)	VOL(AC)		VREFDQ – 0.12	V	
Output Leakage current (DQ, DM, DQS_t, DQS_c) (DQ, DQS_t, DQS_c are disabled; 0V . VOUT . VDDQ)	IOZ	min.	-5	µA	
		max.	5	µA	
Delta RON between pull-up and pull-down for DQ/DM	MMPUPD	min.	-15	%	
		max.	15	%	

Notes:
1. IOH = -0.1mA.
2. IOL = 0.1mA
3. The min value is derived when using RTT, min and RON,max (+/- 30% uncalibrated, +/-15% calibrated).

Differential AC and DC Output Levels

Table 3-13 shows the output levels used for measurements of differential signals.

Table 3-13 Differential AC and DC Output Levels

Parameter	Symbol	Value	Unit	Note
AC differential output high measurement level (for output SR)	VOHdiff(AC)	+0.2 × VDDQ	V	1
AC differential output low measurement level (for output SR)	VOLdiff(AC)	-0.2 × VDDQ	V	2

Notes:
1. IOH = -0.1mA
2. IOL = 0.1mA

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Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table 3-14 and Figure 3-8.

Table 3-14 Single-ended Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) – VOL(AC)] / DeltaTRse
Single-ended output slew rate for falling edge	VOH(AC)	VOL(AC)	[VOH(AC) – VOL(AC)] / DeltaTFse

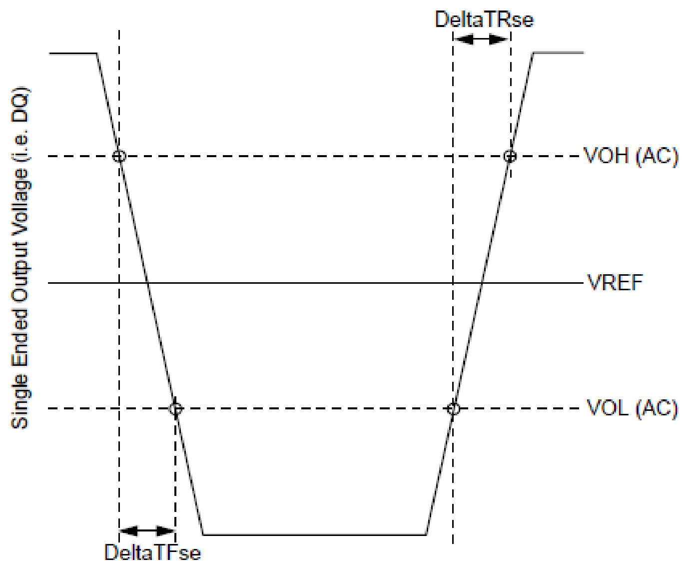

Figure 3-8 — Single Ended Output Slew Rate Definition

Table 3-15 Output Slew Rate (single-ended)

Parameter	Symbol	min.	max.	Unit
Single-ended Output Slew Rate (RON = 40Ω ± 30%)	SRQse	1.5	3.5	V/ns
Output slew-rate matching Ratio (Pull-up to Pull-down)		0.7	1.4	

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), se: Single-ended Signals

Notes: 1. Measured with output reference load.
2. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pulldown drivers due to process variation.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
4. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

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Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 3-16 and Figure 3-9.

Table 3-16 Differential Output Slew Rate Definition

Description	Measured		Defined by
	from	to	
Differential output slew rate for rising edge	VOLdiff(AC)	VOHdiff(AC)	[VOHdiff(AC) – VOLdiff(AC)] / DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff(AC)	VOLdiff(AC)	[VOHdiff(AC) – VOLdiff(AC)] / DeltaTFdiff

Note: 1. Output slew rate is verified by design and characterization, and may not be subject to production test.

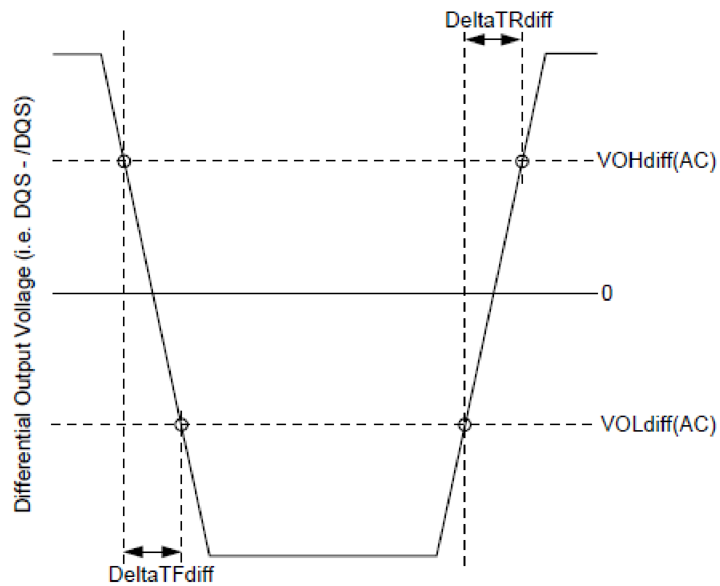

Figure 3-9 Differential Output Slew Rate Definition

Table 3-17 Differential Output Slew Rate

Parameter	Symbol	min.	max.	Unit
Differential Output Slew Rate (RON = 40Ω ± 30%)	SRQdiff	3.0	8.0	V/ns

Remark: SR: Slew Rate, Q: Query Output (like in DQ, which stands for Data-in, Query-Output), diff: Differential Signals

Notes: 1. Measured with output reference load.
2. The output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC).
3. Slew rates are measured under normal SSO conditions, with 1/2 of DQ signals per data byte driving logic high and 1/2 of DQ signals per data byte driving logic low.

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Overshoot and Undershoot Specifications

Table 3-18 AC Overshoot/Undershoot Specification

Parameter		1333	1600	Unit
Maximum peak amplitude allowed for overshoot area.	Max.	0.35		V
Maximum peak amplitude allowed for undershoot area.	Max.	0.35		V
Maximum overshoot area above VDD*1 .	max.	0.12	0.10	V-ns
Maximum undershoot area below VSS*2	max.	0.12	0.10	V-ns

Notes:

1. For CA0 – CA9, CK_t, CK_c, CS_c, and CKE, VDD stands for VDDQ. For DQ, DM, ODT DQS_t, and DQS_c, VDD stands for VDDCA
2. For CA0 – CA9, CK_t, CK_c, CS_c, and CKE, VSS stands for VSS. For DQ, DM, ODT, DQS_t, and DQS_c, VSS stands for VSS
3. Values are referenced from actual VDD, VSS levels.

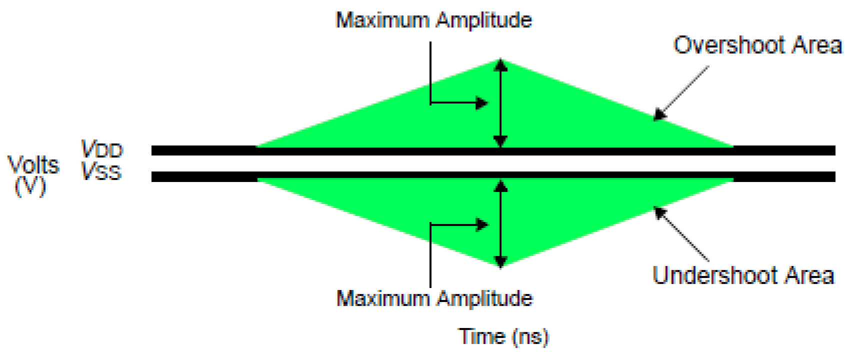

Figure 3-10 Overshoot and Undershoot Definition

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RONPU and RONPD Resistor Definition

$$RONPU = \frac{(VDDQ - Vout)}{ABS(Iout)}$$

Note 1: This is under the condition that RONPD is turned off

$$RONPD = \frac{Vout}{ABS(Iout)}$$

Note 1: This is under the condition that RONPU is turned off

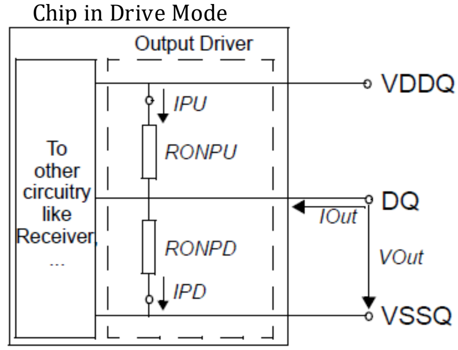

Figure 3-11 Output Driver: Definition of Voltages and Currents

RONPU and RONPD Characteristics with ZQ Calibration

Output driver impedance RON is defined by the value of the external reference resistor RZQ. Nominal RZQ is 240Ω.

Table 3-19 Output Driver DC Electrical Characteristics with ZQ Calibration

RONNOM	Resistor	Vout	min.	nom.	Max.	Unit	Note
34.3Ω	RON34PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/7	1, 2, 3, 4
	RON34PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/7	1, 2, 3, 4
40.0Ω	RON40PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/6	1, 2, 3, 4
	RON40PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/6	1, 2, 3, 4
48.0Ω	RON48PD	0.5 × VDDQ	0.85	1.00	1.15	RZQ/5	1, 2, 3, 4
	RON48PU	0.5 × VDDQ	0.85	1.00	1.15	RZQ/5	1, 2, 3, 4
Mismatch between pull-up and pull-down	MMPUPD		-15.00		15.00	%	1, 2, 3, 4, 5

Notes:

1. Across entire operating temperature range, after calibration.
2. RZQ = 240Ω
3. The tolerance limits are specified after calibration with fixed voltage and temperature. For behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
4. Pull-down and pull-up output driver impedances are recommended to be calibrated at 0.5 × VDDQ.
5. Measurement definition for mismatch between pull-up and pull-down,
   MMPUPD: Measure RONPU and RONPD, both at 0.5 × VDDQ:

$$MMPUPD = \frac{RONPU - RONPD}{RONNOM} \times 100$$

   For example, with MMPUPD max.= 15% and RONPD = 0.85, RONPU must be less than 1.0.
6. Output driver strength measured without ODT.

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Output Driver Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Tables shown below.

Table 3-20 Output Driver Sensitivity Definition

Resistor	Vout	min.	max.	Unit	LPDDR3 Interface
RONPD RONPU	0.5 × VDDQ	85 – (dRONdT × |ΔT|) – (dRONdV × |ΔV|)	115 + (dRONdT × |ΔT|) + (dRONdV × |ΔV|)	%	1, 2
RTT	0.5 × VDDQ	85 – (dRTTdT × |ΔT|) – (dRTTdV × |ΔV|)	115 + (dRTTdT × |ΔT|) + (dRTTdV × |ΔV|)	%	1, 2

Notes:
1. ΔT = T – T(@ calibration), ΔV = V – V(@ calibration)
2. dRONdT, dRONdV, dRTTdV and dRTTdT are not subject to production test but are verified by design and characterization

Table 3-21 Output Driver Temperature and Voltage Sensitivity

Parameter	Symbol	min.	max.	Unit
RON Temperature Sensitivity	dRONdT	0	0.75	%/°C
RON Voltage Sensitivity	dRONdV	0	0.20	%/mV
RTT Temperature Sensitivity	dRTTdT	0	0.75	%/°C
RTT Voltage Sensitivity	dRTTdV	0	0.20	%/mV

RONPU and RONPD Characteristics without ZQ Calibration

Output driver impedance RON is defined by design and characterization as default setting.

Table 3-22 Output Driver DC Electrical Characteristics Without ZQ Calibration

RONNOM	Resistor	Vout	min.	nom.	Max.	Unit	Note
34.3Ω	RON34PD	0.5 × VDDQ	24	34.3	44.6	Ω	1
	RON34PU	0.5 × VDDQ	24	34.3	44.6	Ω	1
40.0Ω	RON40PD	0.5 × VDDQ	28	40	52	Ω	1
	RON40PU	0.5 × VDDQ	28	40	52	Ω	1
48.0Ω	RON48PD	0.5 × VDDQ	33.6	48	62.4	Ω	1
	RON48PU	0.5 × VDDQ	33.6	48	62.4	Ω	1
60.0Ω (optional)	RON60PD	0.5 × VDDQ	42	60	78	Ω	1
	RON60PU	0.5 × VDDQ	42	60	78	Ω	1
80.0Ω (optional)	RON80PD	0.5 × VDDQ	56	80	104	Ω	1
	RON80PU	0.5 × VDDQ	56	80	104	Ω	1

Note: 1. Across entire operating temperature range, without calibration.

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RZQ I-V Curve

Table 3-23 RZQ I-V Curve

Voltage[V]	R_{ON} = 240 Ω (R_{ZQ})							
	Pull-Down				Pull-Up			
	Current [mA] / R_{ON} [Ohms]				Current [mA] / R_{ON} [Ohms]			
	default value after ZQReset		with Calibration		default value after ZQReset		with Calibration	
	Min [mA]	Max [mA]	Min [mA]	Max [mA]	Min [mA]	Max [mA]	Min [mA]	Max [mA]
0.00	0.00	0.00	n/a	n/a	0.00	0.00	n/a	n/a
0.05	0.17	0.35	n/a	n/a	-0.17	-0.35	n/a	n/a
0.10	0.34	0.70	n/a	n/a	-0.34	-0.70	n/a	n/a
0.15	0.50	1.03	n/a	n/a	-0.50	-1.03	n/a	n/a
0.20	0.67	1.39	n/a	n/a	-0.67	-1.39	n/a	n/a
0.25	0.83	1.73	n/a	n/a	-0.83	-1.73	n/a	n/a
0.30	0.97	2.05	n/a	n/a	-0.97	-2.05	n/a	n/a
0.35	1.13	2.39	n/a	n/a	-1.13	-2.39	n/a	n/a
0.40	1.26	2.71	n/a	n/a	-1.26	-2.71	n/a	n/a
0.45	1.39	3.01	n/a	n/a	-1.39	-3.01	n/a	n/a
0.50	1.51	3.32	n/a	n/a	-1.51	-3.32	n/a	n/a
0.55	1.63	3.63	n/a	n/a	-1.63	-3.63	n/a	n/a
0.60	1.73	3.93	2.17	2.94	-1.73	-3.93	-2.17	-2.94
0.65	1.82	4.21	n/a	n/a	-1.82	-4.21	n/a	n/a
0.70	1.90	4.49	n/a	n/a	-1.90	-4.49	n/a	n/a
0.75	1.97	4.74	n/a	n/a	-1.97	-4.74	n/a	n/a
0.80	2.03	4.99	n/a	n/a	-2.03	-4.99	n/a	n/a
0.85	2.07	5.21	n/a	n/a	-2.07	-5.21	n/a	n/a
0.90	2.11	5.41	n/a	n/a	-2.11	-5.41	n/a	n/a
0.95	2.13	5.59	n/a	n/a	-2.13	-5.59	n/a	n/a
1.00	2.17	5.72	n/a	n/a	-2.17	-5.72	n/a	n/a
1.05	2.19	5.84	n/a	n/a	-2.19	-5.84	n/a	n/a
1.10	2.21	5.95	n/a	n/a	-2.21	-5.95	n/a	n/a
1.15	2.23	6.03	n/a	n/a	-2.23	-6.03	n/a	n/a
1.20	2.25	6.11	n/a	n/a	-2.25	-6.11	n/a	n/a

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R_{ZQ} I-V Curve (cont'd)

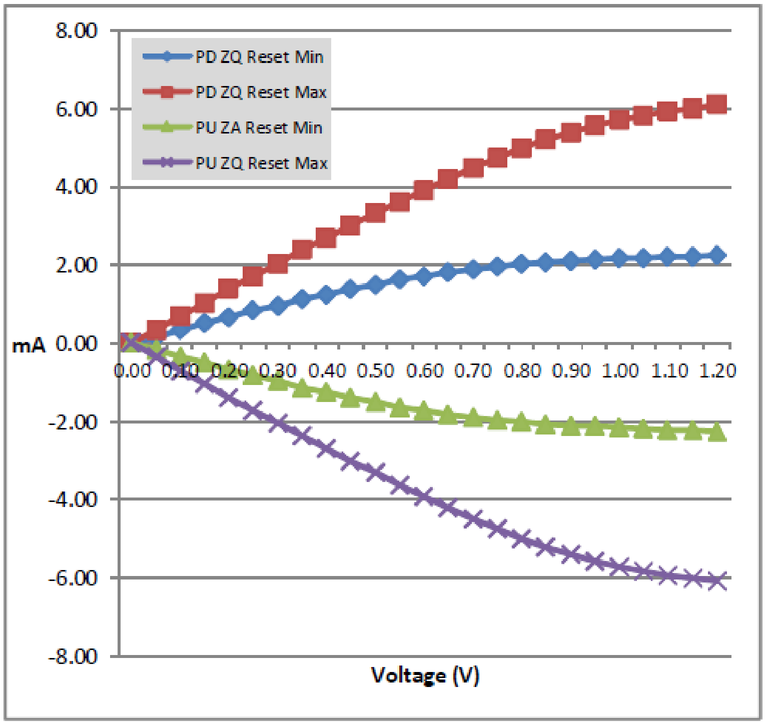

Figure 3-12 I-V Curve After ZQ Reset

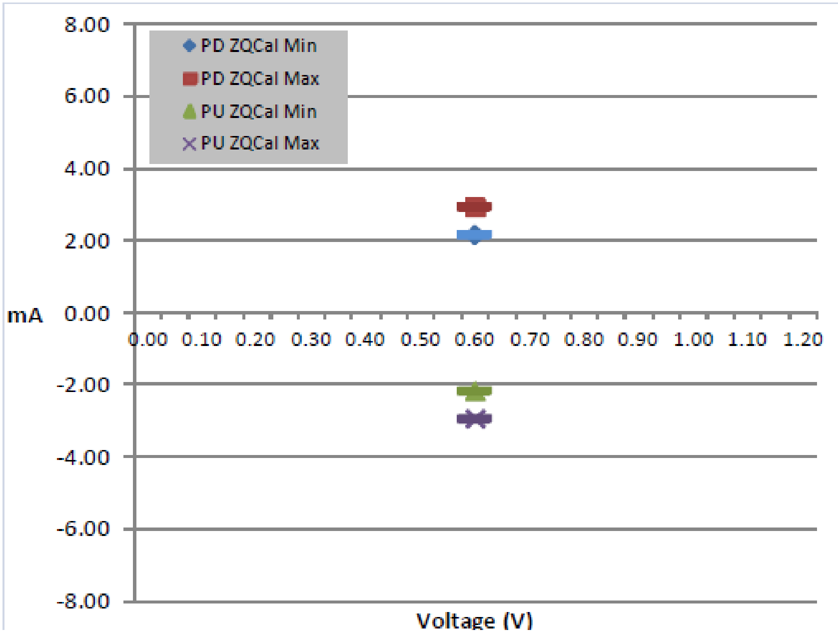

Figure 3-13 I-V Curve After Calibration

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ODT Levels and I-V Characteristics

On-Die Termination effective resistance, RTT, is defined by mode register MR11[1:0]. ODT is applied to the DQ, DM, and DQS_t/DQS_c pins. A functional representation of the on-die termination is shown Figure 3-14

RTT is defined by the following formula:
RTTPU = (VDDQ – Vout) / | Iout |

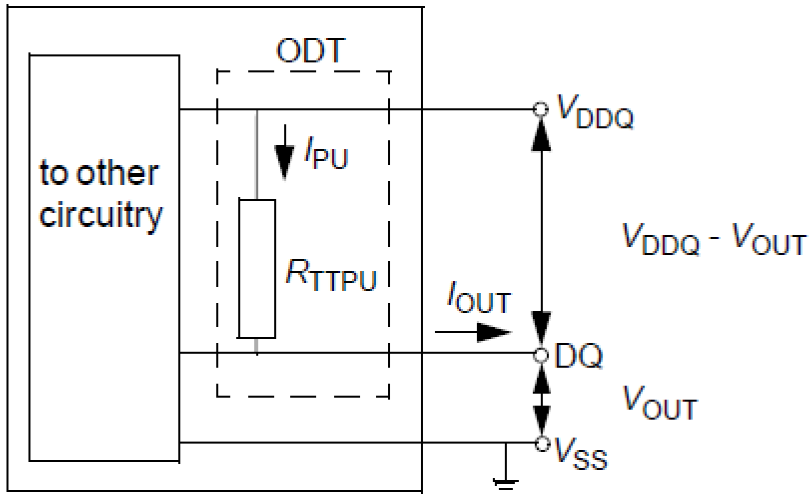

Figure 3-14 Functional representation of On-Die Termination

Table 3-24 –
ODT DC Electrical Characteristics, assuming RZQ = 240 ohm after proper ZQ calibration

R_{TT} (ohm)	V_{OUT} (V)	I_{OUT}	
		Min (mA)	Max (ma)
$R_{ZQ}/1$	0.6	-2.17	-2.94
$R_{ZQ}/2$	0.6	-4.34	-5.88
$R_{ZQ}/4$	0.6	-8.68	-11.76

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Electrical Specifications

IDD Measurement Conditions

The following definitions are used within the IDD measurement tables:
LOW: VIN ≤ VIL(DC) max.
HIGH: VIN ≥ VIH(DC) min.
STABLE: Inputs are stable at a HIGH or LOW level
SWITCHING: See Table 3-25, 3-26 and 3-27.

Table 3-25 Definition of Switching for CA Input Signals

Switching for CA								
	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)	CK_t (RISING) / CK_c (FALLING)	CK_t (FALLING) / CK_c (RISING)
Cycle	N		N + 1		N + 2		N + 3	
CS_n	HIGH		HIGH		HIGH		HIGH	
CA0	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA1	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA2	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA3	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA4	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA5	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA6	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA7	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH
CA8	HIGH	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH
CA9	HIGH	HIGH	HIGH	LOW	LOW	LOW	LOW	HIGH

Notes: 1. CS_n must always be driven HIGH.
2. 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.
3. The above pattern (N, N + 1, N + 2, N + 3...) is used continuously during IDD measurement for IDD values that require SWITCHING on the CA bus.

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Table 3-26 Definition of Switching for IDD4R

Clock	CKE	CS_n	Clock Cycle Number	Command	CA0 – CA2	CA3 – CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLH	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 3	NOP	HLH	HLHLLHL	L
Rising	HIGH	LOW	N + 4	Read_Rising	HLH	HLHLLHL	H
Falling	HIGH	LOW	N + 4	Read_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N + 5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N + 6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N + 6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N + 7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 7	NOP	HLH	LHLHLHL	L

Notes: 1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. The above pattern (N, N + 1...) is used continuously during IDD measurement for IDD4R.

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Table 3-27 Definition of Switching for IDD4W

Clock	CKE	/CS	Clock Cycle Number	Command	CA0 – CA2	CA3 – CA9	All DQ
Rising	HIGH	LOW	N	Read_Rising	HLL	LHLHLHL	L
Falling	HIGH	LOW	N	Read_Falling	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 1	NOP	LLL	LLLLLLL	L
Rising	HIGH	HIGH	N + 2	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 2	NOP	LLL	LLLLLLL	H
Rising	HIGH	HIGH	N + 3	NOP	LLL	LLLLLLL	H
Falling	HIGH	HIGH	N + 3	NOP	HLL	HLHLLHL	L
Rising	HIGH	LOW	N + 4	Read_Rising	HLL	HLHLLHL	H
Falling	HIGH	LOW	N + 4	Read_Falling	LHH	HHHHHHH	H
Rising	HIGH	HIGH	N + 5	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 5	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N + 6	NOP	HHH	HHHHHHH	L
Falling	HIGH	HIGH	N + 6	NOP	HHH	HHHHHHH	L
Rising	HIGH	HIGH	N + 7	NOP	HHH	HHHHHHH	H
Falling	HIGH	HIGH	N + 7	NOP	HLL	LHLHLHL	L

Notes: 1. Data strobe (DQS) is changing between HIGH and LOW every clock cycle.
2. Data masking (DM) must always be driven LOW.
3. The above pattern (N, N + 1...) is used continuously during IDD measurement for IDD4W.

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IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire extended temperature range

Table 3-28 — IDD Specification Parameters and Operating Conditions

Parameter/Condition	Symbol	Power Supply	Notes
Active power-down standby current with clock stop: CK = LOW, CK# = HIGH; CKE is LOW; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs	I_{DD3PS1}	V_{DD}	
	I_{DD3PS2}	V_{DD}	
	$I_{DD3PS,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are switching; Data bus inputs are stable	I_{DD3N}	V_{DD}	
	I_{DD3N}	V_{DD}	
	$I_{DD3N,in}$	V_{DDCA}, V_{DDQ}	4
Active non-power-down standby current with clock stopped: CK = LOW, CK# = HIGH CKE is HIGH; CS_n is HIGH; One bank is active; CA bus inputs are stable; Data bus inputs are stable	I_{DD3NS1}	V_{DD}	
	I_{DD3NS2}	V_{DD}	
	$I_{DD3NS,in}$	V_{DDCA}, V_{DDQ}	4
Operating burst READ current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands; One bank is active; BL = 8; RL = RL (MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled	I_{DD4R1}	V_{DD}	
	I_{DD4R2}	V_{DD}	
	$I_{DD4R,in}$	V_{DDCA}	
	I_{DD4RQ}	V_{DDQ}	5
Operating burst WRITE current: $t_{CK} = t_{CKmin}$; CS_n is HIGH between valid commands;	I_{DD4W1}	V_{DD} 1	

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One bank is active; BL = 8; WL = Wlmin; CA bus inputs are switching; 50% data change each burst transfer	I_{DD4W2}	V_{DD}	
	$I_{DD4W,in}$	V_{DDCA}, V_{DDQ}	4
All-bank REFRESH burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD51}	V_{DD1}	
	I_{DD52}	V_{DD2}	
	I_{DD5IN}	V_{DDCA}, V_{DDQ}	4

Table 3-29 — IDD Specification Parameters and Operating Conditions (cont'd)

Parameter/Condition	Symbol	Power Supply	Notes
All-bank REFRESH average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD5AB1}	V_{DD}	
	I_{DD5AB2}	V_{DD}	
	$I_{DD5AB,in}$	V_{DDCA}, V_{DDQ}	4
Per-bank REFRESH average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable ODT disabled	I_{DD5PB1}	V_{DD}	
	I_{DD5PB2}	V_{DD}	
	$I_{DD5PB,in}$	V_{DDCA}, V_{DDQ}	4
Self refresh current (–25°C to +85°C): CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable Maximum 1x self refresh rate ODT disabled	I_{DD61}	V_{DD1}	6, 7, 9
	I_{DD62}	V_{DD}	6, 7, 9
	I_{DD6IN}	V_{DDCA}, V_{DDQ}	4, 6, 7, 9
Self refresh current (+85°C to +105°C): CK_t = LOW, CK_c = HIGH;	I_{DD6ET1}	V_{DD}	7, 8, 9
	I_{DD6ET2}	V_{DD}	7, 8, 9

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CKE is LOW; CA bus inputs are stable; Data bus inputs are stable ODT disabled	$I_{DD6ET,in}$	V_{DDCA}, V_{DDQ}	4, 7, 8, 9
Deep power-down current: CK_t = LOW, CK_c = HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable ODT disabled	I_{DD81}	V_{DD}	
	I_{DD82}	V_{DD}	
	I_{DD8IN}	V_{DDCA}, V_{DDQ}	4

NOTE:

1. Published I_{DD} values are the maximum of the distribution of the arithmetic mean.
2. ODT disabled: MR11[2:0] = 000B.
3. I_{DD} current specifications are tested after the device is properly initialized.
4. Measured currents are the summation of V_{DDQ} and V_{DDCA}.
5. Guaranteed by design with output load = 5 pF and R_{ON} = 40 ohm.
6. The 1x self refresh rate is the rate at which the device is refreshed internally during self refresh, before going into the elevated temperature range.
7. This is the general definition that applies to full-array SELF REFRESH.
8. I_{DD6ET} is a typical value, is sampled only, and is not tested.
9. Supplier datasheets may contain additional Self-Refresh I_{DD} values for temperature subranges within the standard or elevated temperature ranges.
10. For all I_{DD} measurements, V_{IHCKE} = 0.8 x V_{DDCA}, V_{ILCKE} = 0.2 x V_{DDCA}.

IDD Specifications (cont'd)

Table 3-30 — IDD6 Partial Array Self-Refresh Current

Parameter		Unit
I_{DD6} Partial Array Self-Refresh Current	Full Array	µA
	1/2 Array	µA
	1/4 Array	µA
	1/8 Array	µA

NOTE:

1 IDD6 currents are measured using bank-masking only.
2 I_{DD} values published are the maximum of the distribution of the arithmetic mean.

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Characteristics 1 (For 4Gb)

(TC = -25 °C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 3-31 IDD Specification Parameters and Operating Conditions (cont'd)

Symbol	Power Supply	1600	Unit	Parameter/Condition
		max		
IDD0_1	VDD1	9	mA	**Operating one bank active-pecharge current:** tCK = tCK(avg)min; tRC = tRCmin; CKE is HIGH; CS_n is HIGH between valid commands; CA bus inputs are SWITCHING; Data bus inputs are STABLE ODT disable
IDD0_2	VDD2	56	mA	
IDD0_IN	VDDCA VDDQ	9.5	mA	
IDD2P_1	VDD1	0.95	mA	**Idle power-down standby current:** tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE ODT disable
IDD2P_2	VDD2	2.1	mA	
IDD2P_IN	VDDCA VDDQ	0.07	mA	
IDD2PS_1	VDD1	0.95	mA	**Idle power-down standby current with clock stop:** CK = LOW, /CK = HIGH; CKE is LOW; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE ODT disable
IDD2PS_2	VDD2	2.1	mA	
IDD2PS_IN	VDDCA VDDQ	0.07	mA	
IDD2N_1	VDD1	1.85	mA	**Idle non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are SWITCHING; Data bus inputs are STABLE ODT disable
IDD2N_2	VDD2	36	mA	
IDD2N_IN	VDDCA VDDQ	9	mA	
IDD2NS_1	VDD1	1.85	mA	**Idle non power-down standby current with clock stop:** CK _t= LOW, CK_c = HIGH; CKE is HIGH; CS_n is HIGH; All banks idle; CA bus inputs are STABLE; Data bus inputs are STABLE ODT disable
IDD2NS_2	VDD2	15.1	mA	
IDD2NS_IN	VDDCA VDDQ	4.8	mA	
IDD3P_1	VDD1	1.0	mA	**Active power-down standby current:** tCK = tCK(avg)min; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are SWITCHING; Data bus inputs are STABLE ODT disable
IDD3P_2	VDD2	15	mA	
IDD3P_IN	VDDCA VDDQ	0.2	mA	
IDD3PS_1	VDD1	1.3	mA	**Active power-down standby current with clock stop:** CK _t= LOW, CK_c = HIGH; CKE is LOW; CS_n is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE ODT disable
IDD3PS_2	VDD2	15	mA	
IDD3PS_IN	VDDCA VDDQ	0.2	mA	
IDD3N_1	VDD1	2.0	mA	**Active non power-down standby current:** tCK = tCK(avg)min; CKE is HIGH; CS_n is HIGH; One bank active;
IDD3N_2	VDD2	44	mA	

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IDD3N_IN	VDDCA VDDQ	9	mA	CA bus inputs are SWITCHING; Data bus inputs are STABLE ODT disable
IDD3NS_1	VDD1	2.0	mA	**Active non power-down standby current with clock stop:** CK_t = LOW, CK_c = HIGH; CKE is HIGH; /CS is HIGH; One bank active; CA bus inputs are STABLE; Data bus inputs are STABLE ODT disable
IDD3NS_2	VDD2	20	mA	
IDD3NS_IN	VDDCA VDDQ	4.9	mA	
IDD4R_1	VDD1	2	mA	**Operating burst read current:** tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank active; BL = 4; RL = Rlmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; ODT disable
IDD4R_2	VDD2	220	mA	
IDD4R_IN	VDDCA	9.1	mA	
IDD4W_1	VDD1	2	mA	**Operating burst write current:** tCK = tCK(avg)min; CS_n is HIGH between valid commands; One bank active; BL = 4; WL = Wlmin; CA bus inputs are SWITCHING; 50% data change each burst transfer; ODT disable;
IDD4W_2	VDD2	240	mA	
IDD4W_IN	VDDCA VDDQ	50	mA	

IDD5_1	VDD1	34	mA	**All Bank Auto Refresh Burst current:**
				tCK = tCK(avg)min; CKE is HIGH between valid commands;
				tRC = tRFCabmin; Burst refresh;
				CA bus inputs are SWITCHING;
				Data bus inputs are STABLE;
				ODT disable

IDD5_2	VDD2	130	mA	
IDD5_IN	VDDCA VDDQ	9.3	mA	

IDD5AB_1	VDD1	3.0	mA	**All Bank Auto Refresh Average current:**
				tCK = tCK(avg)min; CKE is HIGH between valid commands;
				tRC = tREFI;
				CA bus inputs are SWITCHING;
				Data bus inputs are STABLE;
				ODT disable

IDD5AB_2	VDD2	39	mA	
IDD5AB_IN	VDDCA VDDQ	9	mA	

IDD5PB_1	VDD1	3.0	mA	**Per Bank Auto Refresh Average current:**
				tCK = tCK(avg)min; CKE is HIGH between valid commands;
				tRC = tREFI/8;
				CA bus inputs are SWITCHING;
				Data bus inputs are STABLE;
				ODT disable

IDD5PB_2	VDD2	41	mA	
IDD5PB_IN	VDDCA VDDQ	9.1	mA	

Notes:
1. IDD values published are the maximum of the distribution of the arithmetic mean.
2. IDD current specifications are tested after the device is properly initialized.

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Table 3-32 IDD6 Full and Partial Array Self-Refresh Current

Parameter		Symbol	Value	Unit	Condition
Self-Refresh Current at TC≦+85°C	Full Array	IDD6_1	1660	μA	CK _t= LOW, CK_c = HIGH; CKE is LOW; us inputs are STABLE; Data bus inputs are STABLE;
		IDD6_2	4500	μA	
		IDD6_IN	68	μA	
	1/2 Array	IDD6_1	1250	μA	
		IDD6_2	3500	μA	
		IDD6_IN	68	μA	
	1/4 Array	IDD6_1	1000	μA	
		IDD6_2	3000	μA	
		IDD6_IN	68	μA	
	1/8 Array	IDD6_1	900	μA	
		IDD6_2	2600	μA	
		IDD6_IN	68	μA	

Note:
1. IDD6 85°C is the maximum and IDD6 25°C is typical of the distribution of the arithmetic mean.

DC Characteristics 2

(TC = -25°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 3-33 Electrical Characteristics and Operating Conditions

Symbol	min.	max.	Unit	Parameter/Condition	Note
IL	-2	2	μA	**Input leakage current:** For CA, CKE, CS_n, CK_t, CK_c Any input 0V <VIN < VDDCA (All other pins not under test = 0V)	2
IVREF	-1	1	μA	**VREF supply leakage current:** VREFDQ = VDDQ/2 or VREFCA = VDDCA/2 (All other pins not under test = 0V)	1

Notes:
1. The minimum limit requirement is for testing purposes. The leakage current on VREFCA and VREFDQ pins should be minimal.
2. Although DM is for input only, the DM leakage shall match the DQ and DQS_t, DQS_c output leakage specification.

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Pin Capacitance (For 4Gb)

(TA = +25°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 3-34 Input/Output Capacitance

Parameter	Symbol	min.	max.	Unit	Note
Input capacitance, CK_t and CK_c	CCK	0.5	1.2	pF	1, 2
Input capacitance delta, CK_t and CK_c	CDCK	0	0.15	pF	1, 2, 3
Input capacitance, all other input-only pins	CI	0.5	1.1	pF	1, 2, 4
Input capacitance delta, all other input-only pins	CDI	-0.25	0.2	pF	1, 2, 5
Input/output capacitance, DQ, DM, DQS_t, DQS_c	CIO	1.0	1.8	pF	1, 2, 6, 7
Input/output capacitance delta, DQS_t, DQS_c	CDDQS	0	0.2	pF	1, 2, 7, 8
Input/output capacitance delta, DQ, DM	CDIO	-0.25	0.25	pF	1, 2, 7, 9
Input/output capacitance ZQ Pin	CZQ	0	2.0	pF	1, 2

Notes:

1. This parameter applies to die device only (does not include package capacitance)
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating
3. Absolute value of CCK_t – CCK_c.
4. CI applies to CS_n, CKE, CA0 – CA9,ODT
5. CDI = CI – 0.5 × (CCK_t + CCK_c)
6. DM loading matches DQ and DQS
7. MR3 I/O configuration DS OP3-OP0 = 0001B (34.3 Ω typical)
8. Absolute value of CDQS_t and CDQS_c
9. CDIO = CIO – 0.5 × (CDQS_t + CDQS_c) in byte-lane.

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LPDDR3 Refresh Requirements by Device Density

Table 3-35 LPDDR3 Refresh Requirement Parameters (per density)

Parameter		Symbol	4 Gb	Unit
Number of Banks			8	-
Refresh Window : T_{case} ≤ 85°C		t_{REFW}	32	ms
Refresh Window 1/2-Rate Refresh		t_{REFW}	16	ms
Refresh Window 1/4-Rate Refresh		t_{REFW}	8	ms
Required number of REFRESH commands (min)		R	8,192	-
Average time between REFRESH commands (for reference only) Tcase ≤ 85°C	REFab	t_{REFI}	3.9	us
	REFpb	t_{REFIpb}	0.4875	us
Refresh Cycle time		t_{RFCab}	130	ns
Per Bank Refresh Cycle time		t_{RFCpb}	60	ns

Table 3-36 LPDDR3 Read and Write Latencies

Parameter	Value							Unit
Max. Clock Frequency	166	400	533	600	667	733	800	MHz
Max. Data Rate	333	800	1066	1200	1333	1466	1600	MT/s
Average Clock Period	6	2.5	1.875	1.667	1.5	1.364	1.25	ns
Read Latency	3[1]	6	8	9	10	11	12	t_{CK}(avg)
Write Latency (Set A)	1[1]	3	4	5	6	6	6	t_{CK}(avg)
Write Latency (Set B)[2]	1[1]	3	4	5	8	9	9	t_{CK}(avg)

NOTE:

1 RL=3/WL=1 setting is an optional feature. Refer to MR0 OP<7>.

2 Write Latency (Set B) support is an optional feature. Refer to MR0 OP<6>

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AC Characteristics

(TC = -25°C to +85°C, VDD1 = 1.70V to 1.95V, VDD2, VDDQ = 1.14V to 1.30V)

Table 3-37 AC Characteristics Table*6

Parameter	Symbol	Min/ Max	Data Rate		Unit
			1333	1600	
Maximum clock frequency	f_{CK}	–	667	800	MHz
Clock Timing					
Average clock period	$t_{CK(avg)}$	MIN	1.5	1.25	ns
		MAX	100		
Average HIGH pulse width	$t_{CH(avg)}$	MIN	0.45		$t_{CK(avg)}$
		MAX	0.55		
Average LOW pulse width	$t_{CL(avg)}$	MIN	0.45		$t_{CK(avg)}$
		MAX	0.55		
Absolute clock period	$t_{CK(abs)}$	MIN	$t_{CK(avg)}$ MIN + $t_{JIT(per)}$ MIN		ns
Absolute clock HIGH pulse width	$t_{CH(abs)}$	MIN	0.43		$t_{CK(avg)}$
		MAX	0.57		
Absolute clock LOW pulse width	$t_{CL(abs)}$	MIN	0.43		$t_{CK(avg)}$
		MAX	0.57		
Clock period jitter (with supported jitter)	$t_{JIT(per)}$, allowed	MIN	-80	-70	ps
		MAX	80	70	
Maximum Clock Jitter between two consecutive clock cycles (with allowed jitter)	$t_{JIT(cc)}$, allowed	MAX	160	140	ps
Duty cycle jitter (with supported jitter)	$t_{JIT(duty)}$, allowed	MIN	$min((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) \times t_{CK(avg)}$		ps
		MAX	$max((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) \times t_{CK(avg)}$		
Cumulative errors across 2 cycles	$t_{ERR(2per)}$, allowed	MIN	-118	-103	ps
		MAX	118	103	
Cumulative errors across 3 cycles	$t_{ERR(3per)}$, allowed	MIN	-140	-122	ps
		MAX	140	122	
Cumulative errors across 4 cycles	$t_{ERR(4per)}$, allowed	MIN	-155	-136	ps
		MAX	155	136	

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Cumulative errors across 5 cycles	tERR(5per), allowed	MIN	-168	-147	ps
		MAX	168	147	
Cumulative errors across 6 cycles	tERR(6per), allowed	MIN	-177	-155	ps
		MAX	177	155	
Cumulative errors across 7 cycles	tERR(7per), allowed	MIN	-186	-163	ps
		MAX	186	163	
Cumulative errors across 8 cycles	tERR(8per), allowed	MIN	-193	-169	ps
		MAX	193	169	
Cumulative errors across 9 cycles	tERR(9per), allowed	MIN	-200	-175	ps
		MAX	200	175	
Cumulative errors across 10 cycles	tERR(10per), allowed	MIN	-205	-180	ps
		MAX	205	180	
Cumulative errors across 11 cycles	tERR(11per), allowed	MIN	-210	-184	ps
		MAX	210	184	
Cumulative errors across 12 cycles	tERR(12per), allowed	MIN	-215	-188	ps
		MAX	215	188	
Cumulative errors across *n* = 13, 14, 15…, 19, 20 cycles	tERR(nper), allowed	MIN	tERR(nper),allowed MIN = (1 + 0.68ln(n)) × tJIT(per), allowed MIN		ps
		MAX	tERR (nper), allowed MAX = (1 + 0.68ln(n)) × tJIT(per), allowed MAX		
ZQ Calibration Parameters					
Initialization calibration time	tZQINIT	MIN	1		µs
Long calibration time	tZQCL	MIN	360		ns
Short calibration time	tZQCS	MIN	90		ns
Calibration RESET time	tZQRESET	MIN	max(50ns,3*n*CK)		ns
READ Parameters[5]					
QS output access time from CK_t/CK_c	tDQSCK	MIN	2500		ps
		MAX	5500		
DQSCK delta short[6]	tDQSCKDS	MAX	265	220	ps

DQSCK delta medium[7]	tDQSCKDM	MAX	593	511	ps
DQSCK delta long[8]	tDQSCKDL	MAX	733	614	ps
DQS-DQ skew	tDQSQ	MAX	165	135	ps
DQS output HIGH pulse width	tQSH	MIN	tCH(abs) – 0.05		tCK(avg)
DQS output LOW pulse width	tQSL	MIN	tCL(abs) – 0.05		tCK(avg)
DQ/DQS output hold time from DQS	tQH	MIN	min(tQSH, tQSL)		ps
READ preamble[9, 12]	tRPRE	MIN	0.9		tCK(avg)
READ postamble[9, 13]	tRPST	MIN	0.3		tCK(avg)
DQS Low-Z from clock[9]	tLZ(DQS)	MIN	tDQSCK (MIN) – 300		ps
DQ Low-Z from clock[9]	tLZ(DQ)	MIN	tDQSCK,(MIN) – 300		ps
DQS High-Z from clock[9]	tHZ(DQS)	MAX	tDQSCK,(MAX) – 100		ps
DQ high-Z from clock	tHZ(DQ)	MAX	tDQSCK(max) +(1.4 × tDQSQ(max))		ps
Write parameter					
DQ and DM input hold time (VREF based)	tDH	MIN	175	150	ps
DQ and DM input setup time (VREF based)	tDS	MIN	175	150	ps
DQ and DM input pulse width	tDIPW	MIN	0.35		tCK(avg)
Write command to 1st DQS latching transition	tDQSS	MIN	0.75		tCK(avg)
		MAX	1.25		
DQS input high-level width	tDQSH	MIN	0.4		tCK(avg)
DQS input low-level width	tDQSL	MIN	0.4		tCK(avg)
DQS falling edge to CK setup time	tDSS	MIN	0.2		tCK(avg)
DQS falling edge hold time from CK	tDSH	MIN	0.2		tCK(avg)
Write postamble	tWPST	MIN	0.4		tCK(avg)
Write preamble	tWPRE	MIN	0.8		tCK(avg)
Command Address Input Parameters					
Address and control input setup time	tISCA	MIN	175	150	ps
Address and control input hold time	tIHCA	MIN	175	150	ps
CS_n input setup time	tISCS	MIN	290	270	ps
CS_n input hold time	tIHCS	MIN	290	270	ps
Address and control input pulse width	tIPWCA	MIN	0.35		tCK(avg)

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CS_n input pulse width	tIPWCS	MIN	0.7		tCK(avg)
CKE Input Parameters					
CKE min. pulse width (high and low pulse width) tCKE	tCKE	MIN	MAX(7.5ns ,3nCK)		ns
CKE input setup time	tISCKE*1	MIN	0.25		tCK(avg)
CKE input hold time	tIHCKE*2	MIN	0.25		tCK(avg)
Command path disable delay	tCPDED	MIN	2		tCK(avg)
Boot Parameters (10 MHz – 55 MHz)					
Clock cycle time	tCKb	MAX	100		ns
		MIN	18		
CKE input setup time	tISCKEb	MIN	2.5		ns
CKE input hold time	tIHCKEb	MIN	2.5		ns
Address & control input setup time	tISb	MIN	1150		ps
Address & control input hold time	tIHb	MIN	1150		ps
DQS output data access time from CK_t, CK_c	tDQSCKb	MIN	2		ns
		MAX	10		
Data strobe edge to output data edge	tDQSQb	MAX	1.2		ns
Mode Register Parameters					
MODE REGISTER WRITE command period	tMRW	MIN	10		tCK(avg)
Mode register set command delay (MRW command to non-MRW command interval)	tMRD	MIN	MAX(14ns,10nCK)		ns
MODE REGISTER READ command period	tMRR	MIN	4		tCK(avg)
Additional time after tXP has expired until MRR command may be issued	tMRRI	MIN	tRCD (MIN)		ns
Core Parameters[20]					
READ latency	RL	MIN	10	12	tCK(avg)
WRITE latency (set A)	WL	MIN	6	6	tCK(avg)
WRITE latency (set B)	WL	MIN	8	9	tCK(avg)
ACTIVATE-to- ACTIVATE command period	tRC	MIN	tRAS + tRPab (with Per/all-bank precharge)		ns

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CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH)	tCKESR	MIN	MAX(15ns,3nCK)	ns
SELF REFRESH exit to next valid command delay	tXSR	MIN	Max(tRFCab + 10ns,2nCK)	ns
Exit power- down to next valid command delay	tXP	MIN	MAX(7.5,3nCK)	ns
CAS-to-CAS delay	tCCD	MIN	4	tCK(avg)
Internal READ to PRECHARGE command delay	tRTP	MIN	MAX(7.5ns,4nCK)	ns
RAS-to-CAS delay	tRCD (typ)	MIN	MAX(18ns,3nCK)	ns
Row precharge time (single bank)	tRPpb (typ)	MIN	MAX(18ns,3nCK)	ns
Row precharge time (all banks)	tRPpab (typ)	MIN	MAX(21ns,3nCK)	ns
Row active time	tRAS	MIN	MAX(42ns,3nCK)	ns
		MAX	70	µs
WRITE recovery time	tWR	MIN	MAX(15ns,4nCK)	ns
Internal WRITE-to- READ command delay	tWTR	MIN	MAX(7.5ns,4nCK)	ns
Active bank A to active bank B	tRRD	MIN	MAX(10ns,2nCK)	ns
Four-bank ACTIVATE window	tFAW	MIN	MAX(50ns,8nCK)	ns
Minimum deep power- down time	tDPD	MIN	500	µs
ODT Parameters				
Asynchronous RTT turn-on dely from ODT input	tODTon	MIN	1.75	ns
		MAX	3.5	
Asynchronous RTT turn-off delay from ODT input	tODToff	MIN	1.75	ns
		MAX	3.5	
Automatic RTT turn-on delay after READ data	tAODTon	MAX	tDQSCK + 1.4 × tDQSQ,max + tCK(avg,min)	ps
Automatic RTT turn-off delay after READ data	tAODToff	MIN	tDQSCK,min – 300	ps
RTT disable delay from power down, self- refresh, and deep power down	tODTd	MAX	12	ns
RTT enable delay from power down and self refresh exit	tODTe	MAX	12	ns
CA Training Parameters				
First CA calibration command after CA calibration mode is programmed	tCAMRD	MIN	20	tCK(avg)

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First CA calibration command after CKE is LOW	tCAENT	MIN	10		tCK(avg)
CA 39alibration exit command after CKE is HIGH	tCAEXT	MIN	10		tCK(avg)
CKE LOW after CA calibration mode is programmed	tCACKEL	MIN	10		tCK(avg)
CKE HIGH after the last CA calibration results are driven.	tCACKEH	MIN	10		tCK(avg)
Data out delay after CA training calibra-tion command is programmed	tADR	MAX	20		ns
MRW CA exit command to DQ tri-state	tMRZ	MIN	3		ns
CA calibration command to CA calibration command delay	tCACD	MIN	RU(tADR+2 x tCK)		tCK(avg)
Write Leveling Parameters					
DQS_t/DQS_c delay after write leveling mode is programmed	tWLDQSN	MIN	25		ns
		MAX	--		
First DQS_t/DQS_c edge after write level- ing mode is programmed	tWLMRD	MIN	40		ns
		MAX	--		
Write leveling output delay	tWLO	MIN	0		ns
		MAX	20		
Write leveling hold time	tWLH	MIN	205	175	ps
Write leveling setup time	tWLS	MIN	205	175	ps
Mode register set command delay	tMRD	MIN	Max(14ns, 10nCK)		ns
		MAX	--		

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Notes:

1.Frequency values are for reference only. Clock cycle time (t_{CK}) is used to determine device capabilities
2.All AC timings assume an input slew rate of 2 V/ns for single ended signals
3.Measured with 4 V/ns differential CK_t/CK_c slew rate and nominal VIX.
4.All timing and voltage measurements are defined 'at the ball',
5.READ, WRITE, and input setup and hold values are referenced to VREF.
6.tDQSCKDS is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a contig- uous sequence of bursts in a 160ns rolling window. tDQSCKDS is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter..
7.tDQSCKDM is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 1.6µs rolling window. tDQSCKDM is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter
8. tDQSCKDL is the absolute value of the difference between any two tDQSCK measurements (in a byte lane) within a 32ms rolling window. tDQSCKDL is not tested and is guaranteed by design. Temperature drift in the system is < 10 °C/s. Values do not include clock jitter.
9. For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the tran- sition threshold (VTT). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Figure 3-15 shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different volt- ages. The actual voltage measurement points are not critical as long as the calculation is consistent.
10. Output Transition Timing.

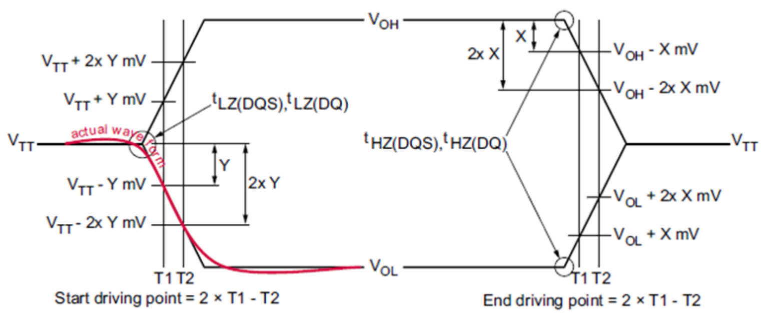

Figure 3-15 tLZ and tHZ Method for Calculating Transition and Endpoints

The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS-/DQS.

11. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS/DQS#.
12. Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driv- ing the first rising strobe edge.
13. Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
14. CKE input setup time is measured from CKE reaching a HIGH/LOW voltage level to CK_t/CK_c crossing.
15. CKE input hold time is measured from CK_t/CK_c crossing to CKE reaching a HIGH/LOW voltage level.
16. Input set-up/hold time for signal (CA[9:0], CS_n).
17. To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
18. The LPDDR3 device will set some mode register default values upon receiving a RESET (MRW) command as speci- fied in "Mode Register Definition".
19. The output skew parameters are measured with default output impedance settings using the reference load.
20. The minimum tCK column applies only when tCK is greater than 6ns.

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CA and CS_n Setup, Hold and Derating

For all input signals (CA and CS_n) the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS(base) and tIH(base) value to the ΔtIS and ΔtIH derating value respectively. Example: tIS (total setup time) = tIS(base) + ΔtIS.

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of VIH(ac)min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(dc) and the first crossing of Vil(ac)max. If the actual signal is always earlier than the nominal slew rate line between shaded 'VREF(dc) to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded 'VREF(dc) to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value.

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(dc)max and the first crossing of VREF(dc). Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(dc)min and the first crossing of VREF(dc). If the actual signal is always later than the nominal slew rate line between shaded 'dc to VREF(dc) region', use nominal slew rate for derating value . If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to VREF(dc) region', the slew rate of a tangent line to the actual signal from the dc level to VREF(dc) level is used for derating value.

For a valid transition the input signal has to remain above/below VIH/IL(ac) for some time tVAC. Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached

VIH/IL(ac) at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach VIH/IL(ac).

The derating values may obtained by linear interpolation. These values are typically not subject to production test. They are verified by design and characterization

Table 3-38 — CA Setup and Hold Base-Values

unit [ps]	Data Rate		reference
	1333	1600	
$t_{ISCA(base)}$	100	75	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
$t_{ISCA(base)}$	-	-	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-135mV
$t_{IHCA(base)}$	125	100	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

NOTE 1 ac/dc referenced for 2V/ns CA slew rate and 4V/ns differential CK_t/CK_c slew rate

Table 3-39 — CS_n Setup and Hold Base-Values

unit [ps]	Data Rate		reference
	1333	1600	
$t_{ISCS(base)}$	215	195	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-150mV
$t_{ISCS(base)}$	-	-	$V_{IH/L(ac)} = V_{REF(dc)}$ +/-135mV
$t_{IHCS(base)}$	240	220	$V_{IH/L(dc)} = V_{REF(dc)}$ +/-100mV

HSUL_12 Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment.

Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

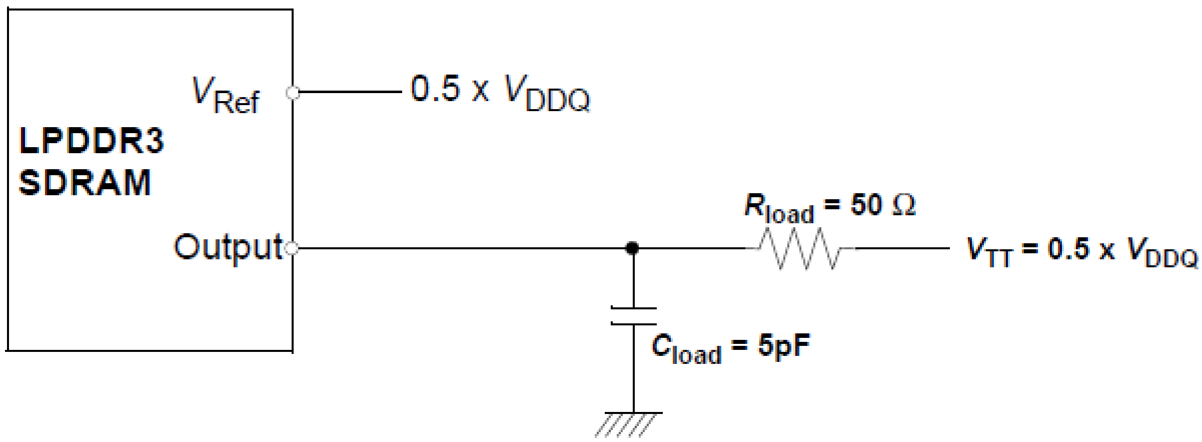

Figure 3-16 HSUL_12 Driver Output Reference Load for Timing and Slew Rate

Note: 1. All output timing parameter values (like tDQSCK, tDQSQ, tQHS, tHZ, tRPRE etc) are reported with respect to this reference load. This reference load is also used to report slew rate.

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Power-up, initialization and Power-Off

DDR3 Mobile RAM Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

Power Ramp and Device Initialization

The following sequence must be used to power up the device. Unless specified otherwise, this procedure is mandatory.

Power Ramp

While applying power (after Ta), CKE must be held LOW (≤ 0.2 × VDDCA) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.

Following the completion of the voltage ramp (Tb), CKE must be maintained LOW. DQ, DM, DQS_t and DQS_c voltage levels must be between VSSQ and VDDQ during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during voltage ramp to avoid latch-up. Voltage ramp power supply requirements are provided in Table 3-41

Table 3-40 — Voltage Ramp Conditions

After...	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDCA}—200mV
	V_{DD1} and V_{DD2} must be greater than V_{DDQ}—200mV
	V_{ref} must always be less than all other supply voltages

NOTE
1 Ta is the point when any power supply first reaches 300mV.
2 Noted conditions apply between Ta and power-off (controlled or uncontrolled).
3 Tb is the point at which all supply and reference voltages are within their defined operating ranges
4 Power ramp duration tINIT0 (Tb – Ta) must not exceed 20ms.
5 The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV.

CKE and Clock

Beginning at Tb, CKE must remain LOW for at least tINIT1, after which CKE can be asserted HIGH. The clock must be stable at least tINIT2 prior to the first CKE LOW-to-HIGH transition (Tc). CKE, CS_n, and CA inputs must observe setup and hold requirements (tIS, tIH) with respect to the first rising clock edge (as well as to subsequent falling and rising edges).
If any MRR commands are issued, the clock period must be within the range defined for tCKb. MRW commands can be issued at normal clock frequencies as long as all AC timings are met. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb)

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before the system is appropriately configured. While keeping CKE HIGH, NOP commands must be issued for at least tINIT3 (Td). The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal shall be statically held at either LOW or HIGH. The ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tZQINIT.

Reset Command

After tINIT3 is satisfied, the MRW RESET command must be issued (Td). An optional PRECHARGE ALL command can be issued prior to the MRW RESET command. Wait at least tINIT4 while keeping CKE asserted and issuing NOP commands. Only NOP commands are allowed during time tINIT4.

Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After tINIT4 is satisfied (Te), only MRR commands and power-down entry/exit commands are supported. After Te, CKE can go LOW in alignment with power-down entry and exit specifications. MRR commands are only valid at this time if the CA bus does not need to be trained. CA Training may only begin after time Tf. User may issue MRR command to poll the DAI bit which will indicate if device auto initialization is complete; once DAI bit indicates completion, SDRAM is in idle state. Device will also be in idle state after tINIT5(max) has expired (whether or not DAI bit has been read by MRR command).As the memory output buffers are not properly configured by Te, some AC parameters must have relaxed timings before the system is appropriately configured.
After the DAI bit (MR0, DAI) is set to zero by the memory device (DAI complete), the device is in the idle state (Tf). DAI status can be determined by issuing the MRR command to MR0. The device sets the DAI bit no later than tINIT5 after the RESET command. The controller must wait at least tINIT5(max) or until the DAI bit is set before proceeding.

ZQ Calibration:

If CA Training is not required, the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10) after time Tf. If CA Training is required, the CA Training may begin at time Tf. See 4.11.3, Mode Register Write – CA Training Mode for the CA Training command. No other CA commands (other than RESET or NOP) may be issued prior to the completion of CA Training. At the completion of CA Training (Tf'), the MRW initialization calibration (ZQ_CAL) command can be issued to the memory (MR10).
This command is used to calibrate output impedance over process, voltage, and temperature. In systems where more than one LPDDR3 device exists on the same bus, the controller must not overlap MRW ZQ_CAL commands. The device is ready for normal operation after tZQINIT..

Normal Operation:

After tZQINIT (Tg), MRW commands must be used to properly configure the memory (for example the output buffer drive strength, latencies, etc.). Specifically, MR1, MR2, and MR3 must be set to configure the memory for the target frequency and memory configuration.
After the initialization sequence is complete, the device is ready for any valid command. After Tg, the clock frequency can be changed using the procedure described in the LPDDR3 specification..

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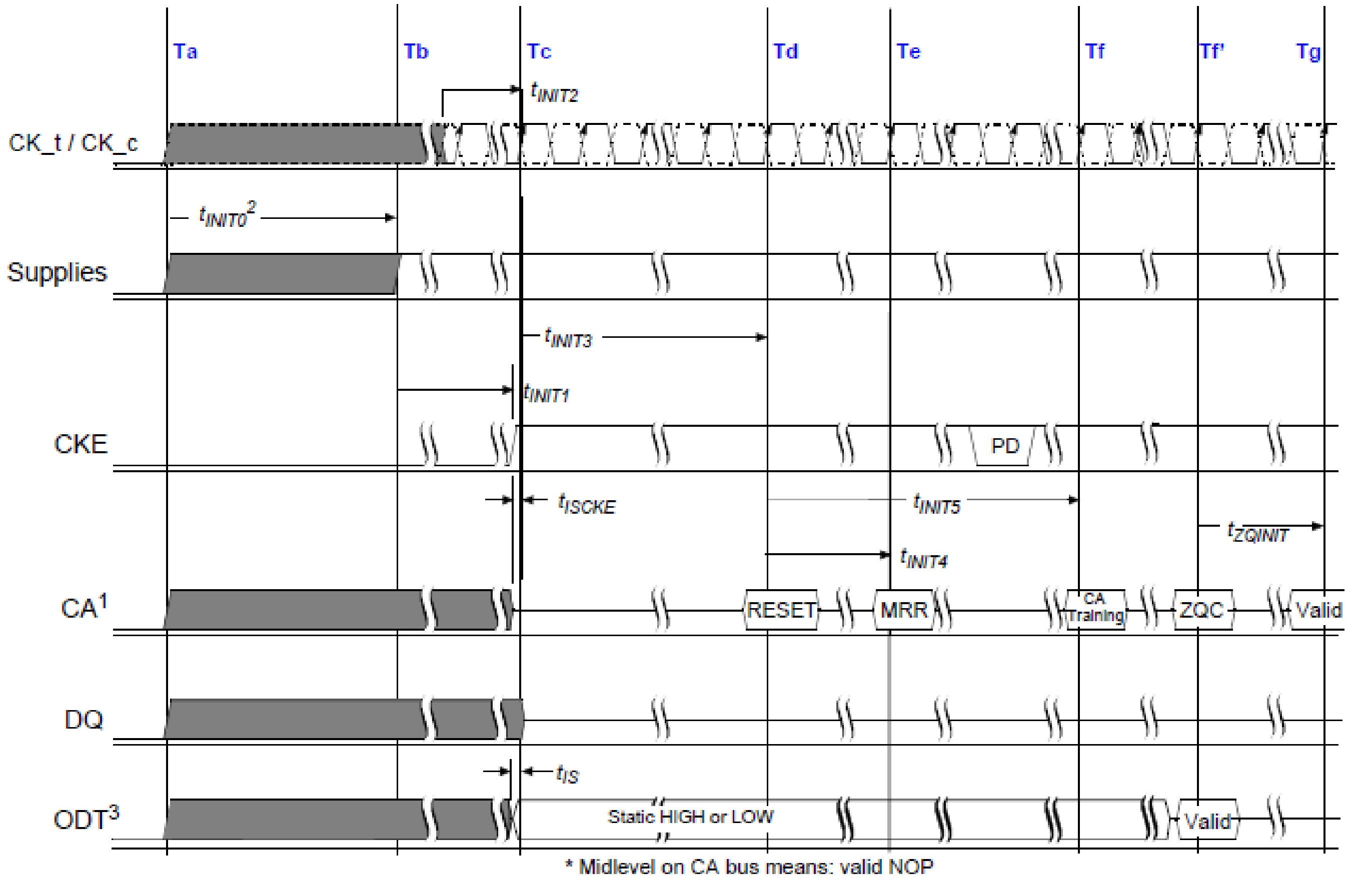

Figure3-17 Voltage Ramp and Initialization Sequence

NOTE:

1. High-Z on the CA bus indicates NOP.
2. For t_{INIT} values, see Table 3-42.
3. After RESET command (time Te), R_{TT} is disabled until ODT function is enabled by MRW to MR11 following Tg.
4. CA Training is optional.

Table 3-41 Timing Parameters for Initialization

Symbol	min.	max.	Unit	Comment
tINIT0	—	20	ms	Maximum Power Ramp Time
tINIT1	100	—	ns	Minimum CKE low time after completion of power ramp
tINIT2	5	—	tCK	Minimum stable clock before first CKE high
tINIT3	200	—	µs	Minimum Idle time after first CKE assertion
tINIT4	1	—	µs	Minimum Idle time after Reset command
tINIT5	—	10	µs	Maximum duration of Device Auto-Initialization
tZQINIT	1	—	µs	ZQ Initial Calibration
tCKb	18	100	ns	Clock cycle time during boot

NOTE 1 If DAI bit is not read via MRR, SDRAM will be in idle state after tINIT5(max) has expired

Initialization After Reset (without Power Ramp):

If the RESET command is issued before or after the power-up initialization sequence, the re-initialization procedure must begin at Td.

Power-Off Sequence

The following procedure is required to power off the device.
While powering off, CKE must be held LOW (≤ 0.2 × VDDCA); all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW.
DQ, DM, DQS_t, and DQS_c voltage levels must be between VSSQ and VDDQ during the power-off sequence to avoid latch-up. CK_t, CK_c, CS_n, and CA input levels must be between VSSCA and VDDCA during the power-off sequence to avoid latch-up.
Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.
The voltage difference between any of VSS, VSSQ, and VSSCA pins must not exceed 100mV

Table 3-42 Power supply conditions

Between...	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}—200mV
Tx and Tz	V_{DD1} must be greater than V_{DDCA}—200mV
Tx and Tz	V_{DD1} must be greater than V_{DDQ}—200mV
Tx and Tz	V_{REF} must always be less than all other supply voltages

Uncontrolled Power-Off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power-supply current capacity must be at zero, except for any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period, the relative voltage between power supplies is uncontrolled. VDD1 and VDD2 must decrease with a slope lower than 0.5 V/μs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device

Table 3-43 — Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	2	s	Maximum Power-Off ramp time

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Command truth table.

Table 3-44 Command Truth Table

SDRAM command	Command Pins			CA pins										
	CKE		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CK EDGE
	CK(n-1)	CK(n)												
MRW	H	H	L	L	L	L	L	MA0	MA1	MA2	MA3	MA4	MA5	↑
			x	MA6	MA7	OP0	OP1	OP2	OP3	OP4	OP5	OP6	OP7	↓
MRR	H	H	L	L	L	L	H	MA0	MA1	MA2	MA3	MA4	MA5	↑
			x	MA6	MA7	X								↓
Refresh (per bank)[11]	H	H	L	L	L	H	L	X						↑
			x	X										↓
Refresh (all bank)	H	H	L	L	L	H	H	X						↑
			x	X										↓
Enter Self Refresh	H	L	L	L	L	H	X							↑
	x		x	X										↓
Activate (bank)	H	H	L	L	H	R8	R9	R10	R11	R12	BA0	BA1	BA2	↑
			x	R0	R1	R2	R3	R4	R5	R6	R7	R13	R14	↓
Write (bank)	H	H	L	H	L	L	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
			x	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Read (bank)	H	H	L	H	L	H	RFU	RFU	C1	C2	BA0	BA1	BA2	↑
			x	AP[3]	C3	C4	C5	C6	C7	C8	C9	C10	C11	↓
Precharge (pre bank, all bank)	H	H	L	H	H	L	H	AB	X	X	BA0	BA1	BA2	↑
			x	X										↓
Enter Deep Power Down	H	L	L	H	H	L	X							↑
	x		x	X										↓
NOP	H	H	L	H	H	H	X							↑
			x	X										↓
Maintain PD, SREF, DPD (NOP)	L	L	L	H	H	H	X							↑
			x	X										↓
NOP	H	H	H	X										↑
			x	X										↓
Maintain PD, SREF, DPD (NOP)	L	L	H	X										↑
			x	X										↓
Enter Power Down	H	L	H	X										↑
	x		x	X										↓
Exit PD, SREF, DPD	L	H	H	X										↑
	x		x	X										↓

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR3 device must be powered down and then restarted through the specified initialization sequence before normal operation can continue.

Notes:
1. All LPDDR3 commands are defined by states of CS_n, CA0, CA1, CA2, CA3, and CKE at the rising edge of the clock
2. Bank addresses BA0, BA1, BA2 (BA) determine which bank is to be operated upon.
3. AP "high" during a READ or WRITE command indicates that an auto-precharge will occur to the bank associated with the READ or WRITE command.
4. X" means "H or L (but a defined logic level)", except when the LPDDR3 SDRAM is in PD, SREF, or DPD, in which case CS_n, CK_t/CK_c, and CA can be floated after the required tCPDED time is satisfied, and until the required exit procedure is initiated as described in the respective entry/exit procedure"
5. Self refresh exit and Deep Power Down exit are asynchronous.
6. VREF must be between 0 and VDDQ during Self Refresh and Deep Power Down operation.
7. Caxr refers to command/address bit "x" on the rising edge of clock.
8. Caxf refers to command/address bit "x" on the falling edge of clock.
9. CS_n and CKE are sampled at the rising edge of clock
10. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
11. AB "high" during Precharge command indicates that all bank Precharge will occur. In this case, Bank Address is do-not-care.

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CKE Truth Table

Table 3-45 — LPDDR3: CKE Table

Device Current State[3]	CKEn-1[1]	CKEn[1]	$\overline{CS}$ [2]	Command n[4]	Operation n[4]	Device Next State	Notes
Active Power Down	L	L	x	x	Maintain Active Power Down	Active Power Down	
	L	H	H	NOP	Exit Active Power Down	Active	6,9
Idle Power Down	L	L	x	x	Maintain Idle Power Down	Idle Power Down	
	L	H	H	NOP	Exit Idle Power Down	Idle	6,9
Resetting Power Down	L	L	x	x	Maintain Resetting Power Down	Resetting Power Down	
	L	H	H	NOP	Exit Resetting Power Down	Idle or Resetting	6,9,12
Deep Power Down	L	L	x	x	Maintain Deep Power Down	Deep Power Down	
	L	H	H	NOP	Exit Deep Power Down	Power On	8
Self Refresh	L	L	x	x	Maintain Self Refresh	Self Refresh	
	L	H	H	NOP	Exit Self Refresh	Idle	7,10
Bank(s) Active	H	L	H	NOP	Enter Active Power Down	Active Power Down	
All Banks Idle	H	L	H	NOP	Enter Idle Power Down	Idle Power Down	13
	H	L	L	Enter Self-Refresh	Enter Self Refresh	Self Refresh	13
	H	L	L	Enter DPD	Enter Deep Power Down	Deep Power Down	13
Resetting	H	L	H	NOP	Enter Resetting Power Down	Resetting Power Down	
Other states	H	H	Refer to the Command Truth Table				

Notes:

1 "CKEn" is the logic state of CKE at clock rising edge n; "CKEn-1" was the state of CKE at the previous clock edge.
2 "CS_n" is the logic state of CS_n at the clock rising edge n;
3 "Current state" is the state of the LPDDR3 device immediately prior to clock edge n.
4 "Command n" is the command registered at clock edge N, and "Operation n" is a result of "Command n".
5 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
6 Power Down exit time (tXP) should elapse before a command other than NOP is issued.
7 Self-Refresh exit time (tXSR) should elapse before a command other than NOP is issued.
8 The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9 The clock must toggle at least twice during the tXP period.
10 The clock must toggle at least twice during the tXSR time.
11 'X' means 'Don't care'.
12 Upon exiting Resetting Power Down, the device will return to the Idle state if tINIT5 has expired.
13 In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VDDQ.

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Mode Register Definition

Table 3-47 shows the mode registers for DDR3 Mobile RAM.
Each register is denoted as "R" if it can be read but not written and "W" if it can be written but not read. Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register

Table 3-46 Mode Register Assignment

MR#	MA [7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00_H	Device Info	R	RL3	WL-B	(RFU)	RZQI		(RFU)		DAI
1	01_H	Device Feature1	W	nWR (for AP)			(RFU)		BL		
2	02_H	Device Feature2	W	WRLev	WL Sel	(RFU)	nWRE	RL & WL			
3	03_H	I/O Config-1	W	(RFU)				DS			
4	04_H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05_H	Basic Config-1	R	Manufacturer ID							
6	06_H	Basic Config-2	R	Revision ID1							
7	07_H	Basic Config-3	R	Revision ID2							
8	08_H	Basic Config-4	R	I/O width		Density				Type	
9	09_H	Test Mode	W	Vendor-Specific Test Mode							
10	$0A_H$	IO Calibration	W	Calibration Code							
11	$0B_H$	ODT	W	(RFU)					PD ctl	DQ ODT	
12-15	$0C_H$-$0F_H$	(Reserved)	—	(RFU)							
16	10_H	PASR_BANK	W	PASR Bank Mask							
17	11_H	PASR_Seg	W	PASR Segment Mask							
18-31	12_H-$1F_H$	(Reserved)	—	(RFU)							
32	20_H	DQ calibration pattern A	R	See Data Calibration Pattern Description							
33-39	21_H-27_H	(Do Not Use)	—	(DNU)							
40	28_H	DQ calibration pattern B	R	See Data Calibration Pattern Description							
41	29_H	CA Training 1	W	See MRW – CA Training Mode							
42	$2A_H$	CA Training 2	W	See MRW – CA Training Mode							
43-47	$2B_H$-$2F_H$	(Do Not Use)	—	(DNU)							
48	30_H	CA Training 3	W	See MRW – CA Training Mode							
49-62	31_H-$3E_H$	(Reserved)	—	(RFU)							
63	$3F_H$	RESET	W	X or 0xFCh							
64-255	40_H-FF_H	(Reserved)	—	(RFU)							

Notes: 1. RFU bits shall be set to '0' during Mode Register writes.
2.. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
3. All Mode Registers that are specified as RFU shall not be written.
4. Writes to read-only registers shall have no impact on the functionality of the device.

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MR#0_Device Information (MA<7:0> = 00H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
RL3	WL (Set B) Support	(RFU)	RZQI		(RFU)		DAI

OP<0>	DAI (Device Auto-Initialization Status) 0B: DAI complete 1B: DAI still in progress
OP<4:3>	RZQI (Built in Self Test for RZQ Information) 01B: ZQ-pin may connect to VDDCA or float 10B: ZQ-pin may short to GND 11B: ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)
OP<6>	WL (Set B) Support 1B: DRAM supports WL (Set B)
OP<7>	RL3 Support 1B: DRAM supports RL = 3, nWR = 3, WL = 1 for frequescies ≤ 166MHz

Notes:

1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to VDDCA to set default calibration, OP[4:3] shall be set to 01. If ZQ is not connected to VDDCA, either OP[4:3]=01 or OP[4:3]=10 might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 per Note 2), the DDR3 Mobile RAM device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e. 240Ω ± 1%).

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MR#1_Device Feature 1 (MA<7:0> = 01H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			(RFU)		BL		

OP<2:0>	BL 011B: BL8 (Default)
OP<7:5>	If nWRE (in MR#2 OP<4>) = 0 001B: nWR = 3 (default) 100B: nWR = 6 110B: nWR = 8 111B: nWR = 9 else (if nWRE (in MR#2 OP<4>) = 1) 000B: nWR = 10 001B: nWR = 11 010B: nWR = 12 100B: nWR = 14 110B: nWR = 16 All others: Reserved

Notes:
1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).
2. The range of nWR is extended using an extra bit (nWRE) in MR#2.

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MR#2_Device Feature 2 (MA<7:0> = 02H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Write Leveling	WL Select	(RFU)	nWRE	RL & WL			

OP<3:0>	RL & WL If OP<6> = 0 (WL Set A, default) 0001B: RL = 3 / WL = 1 (≤ 166MHz) *1 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 6 (≤ 667MHz, default) 1001B: RL = 11 / WL = 6 (≤ 733MHz) 1010B: RL = 12 / WL = 6 (≤ 800MHz) 1100B: RL = 14 / WL = 8 (≤ 933MHz) All others: Reserved If OP<6> = 1 (WL Set B *1) 0001B: RL = 3 / WL = 1 (≤ 166MHz) *1 0100B: RL = 6 / WL = 3 (≤ 400MHz) 0110B: RL = 8 / WL = 4 (≤ 533MHz) 0111B: RL = 9 / WL = 5 (≤ 600MHz) 1000B: RL = 10 / WL = 8 (≤ 667MHz, default) 1001B: RL = 11 / WL = 9 (≤ 733MHz) 1010B: RL = 12 / WL = 9 (≤ 800MHz) 1100B: RL = 14 / WL = 11 (≤ 933MHz) All others: Reserved
OP<4>	nWRE 0B: Enable nWR programming ≤ 9 1B: Enable nWR programming > 9 (default)
OP<6>	WL Select 0B: Select WL Set A (default) 1B: Select WL Set B *2
OP<7>	Write Leveling 0B: Write Leveling Mode disabled (default) 1B: Write Leveling Mode enabled

Notes: 1. See MR#0, OP<7>
2. See MR#0, OP<6>

Table 3-48 DDR3 Mobile RAM Read and Write Latency

Data Rate [Mbps]	333	800	1066	1200	1333	1466	1600
tCK [ns]	6	2.5	1.875	1.67	1.5	1.36	1.25
RL	3	6	8	9	10	11	12
WL (Set A)	1	3	4	5	6	6	6
WL (Set B)	1	3	4	5	8	9	9

MR#3_I/O Configuration 1 (MA<7:0> = 03H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

OP<3:0>	DS 0001B: 34.3Ω typical pull-down/pull-up 0010B: 40Ω typical pull-down/pull-up (default) 0011B: 48Ω typical pull-down/pull-up 0100B: Reserved 0110B: Reserved 1001B: 34.3Ω typical pull-down, 40Ω typical pull-up 1010B: 40Ω typical pull-down, 48Ω typical pull-up 1011B: 34.3Ω typical pull-down, 48Ω typical pull-up All others: Reserved

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MR#4_Device Temperature (MA<7:0> = 04H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				Refresh Rate		

OP<2:0>	Refresh Rate 000B: Low temperature operating limit exceeded 001B: 4 × tREFI, 4 × tREFIpb, 4 × tREFW 010B: 2 × tREFI, 2 × tREFIpb, 2 × tREFW 011B: 1 × tREFI, 1 × tREFIpb, 1 × tREFW(≤ +85℃) 100B: 0.5 × tREFI, 0.5 × tREFIpb, 0.5 × tREFW 101B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, do not de-rate AC timing 110B: 0.25 × tREFI, 0.25 × tREFIpb, 0.25 × tREFW, de-rate AC timing 111B: High temperature operating limit exceeded
OP<7>	TUF(Temperature Update Flag) 0B: OP<2:0> value has not changed since last read of MR4. 1B: OP<2:0> value has changed since last read of MR4.

Notes: 1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up. OP<2:0> bits are undefined after power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to "1" if OP2:OP0 has changed at any time since the last read of MR4.
5. DDR2 Mobile RAM will drive OP<6:5> to '0'.
6. Specified operating temperature range and maximum operating temperature are refer to Section 1 Electrical Conditions on page 6. If maximum temperature is 85°C, functionality for over 85°C is not guaranteed.

MR#5_Basic Configuration 1 (MA<7:0> = 05H): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Manufacturer ID							

OP<7:0>	Manufacturer ID **00000101B (Nanya)**

MR#8_Basic Configuration 4 (MA<7:0> = 08BH): Read-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

OP<1:0>	Type 11B: LPDDR3
OP<5:2>	Density 0110B: 4Gb
OP<7:6>	I/O width 00B: ×32 01B: ×16

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MR#10_Calibration (MA<7:0> = 0AH): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

OP<7:0>	Calibration Code 0xFF: Calibration command after initialization 0xAB: Long calibration 0x56: Short calibration 0xC3: ZQ Reset others: Reserved

Notes: 1. Host processor shall not write MR10 with "Reserved" values.
2. DDR2 Mobile RAM Devices shall ignore calibration command when a "Reserved" value is written into MR10.
3. See AC timing table for the calibration latency.

MR#11_ODT Feature (MA<7:0> = 0BH): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)					PD Control	DQ ODT	

OP<1:0>	DQ ODT 00B : Disabled (default) 01B : RZQ/4 10B : RZQ/2 11B : RZQ/1
OP<2>	PD Control (Power-down Control) 0B: ODT disabled by DRAM during power-down (default) 1B: ODT enabled by DRAM during power-down

MR#16_PASR_Bank Mask (MA<7:0> = 010H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Bank Mask							

OP<7:0>	Bank Mask 0B: refresh enable to the bank (=unmasked, default) 1B: refresh blocked (=masked)

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MR#17_PASR_Segment Mask (MA<7:0> = 11H): Write-only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Segment Mask							

OP<7:0>	Segment 0B: refresh enable to the segment (=unmasked, default) 1B: refresh blocked (=masked)

Segment and OP corresponding table

OP<7:0>	Segment	
	Segment #	Row Address (R14:12)
OP0	Segment 0	000B
OP1	Segment 1	001B
OP2	Segment 2	010B
OP3	Segment 3	011B
OP4	Segment 4	100B
OP5	Segment 5	101B
OP6	Segment 6	110B
OP7	Segment 7	111B

Note: 1. Each bank can be masked independently by setting each OP value.

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Section 4

Revision History

Revision History

Rev.	History	Date
1.0	Initial Release	03 / 2022
1.1	Added Kingston contact info	06 / 2022

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