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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HM628100I Series

Wide Temperature Range Version
8 M SRAM (1024-kword × 8-bit)



ADE-203-1302B (Z)
Rev. 1.0
Sep. 25, 2002

Description

The Hitachi HM628100I Series is 8-Mbit static RAM organized 1,048,576-word × 8-bit. HM628100I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is packaged in standard 44-pin TSOP II for high density surface mounting.

Features

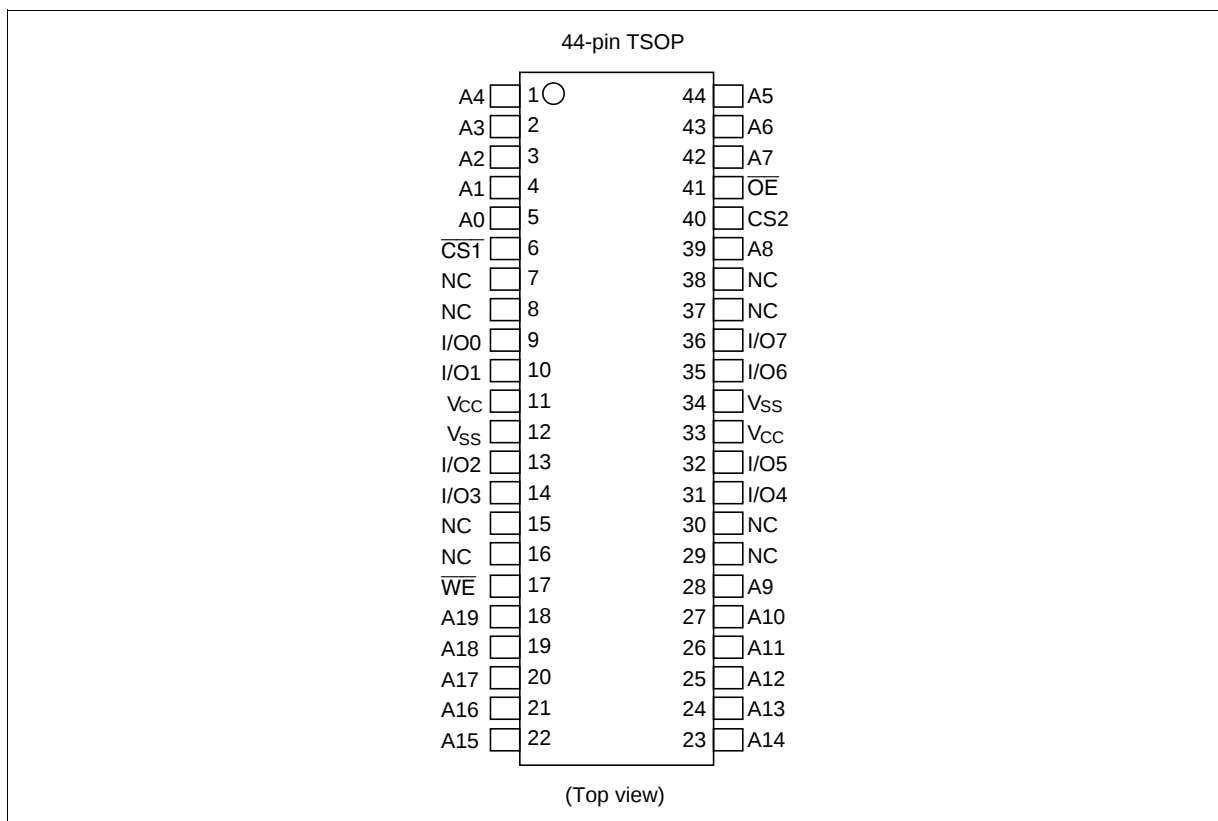
- Single 5.0 V supply: 5.0 V ± 10 %
- Fast access time: 55 ns (max)
- Power dissipation:
 - Active: 10 mW/MHz (typ)
 - Standby: 7.5 μW (typ)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup
- Temperature range: −40 to +85°C

HM628100I Series

Ordering Information

Type No.	Access time	Package
HM628100LTTI-5SL	55 ns	400-mil 44pin plastic TSOP II (normal-bend type) (TTP-44DE)

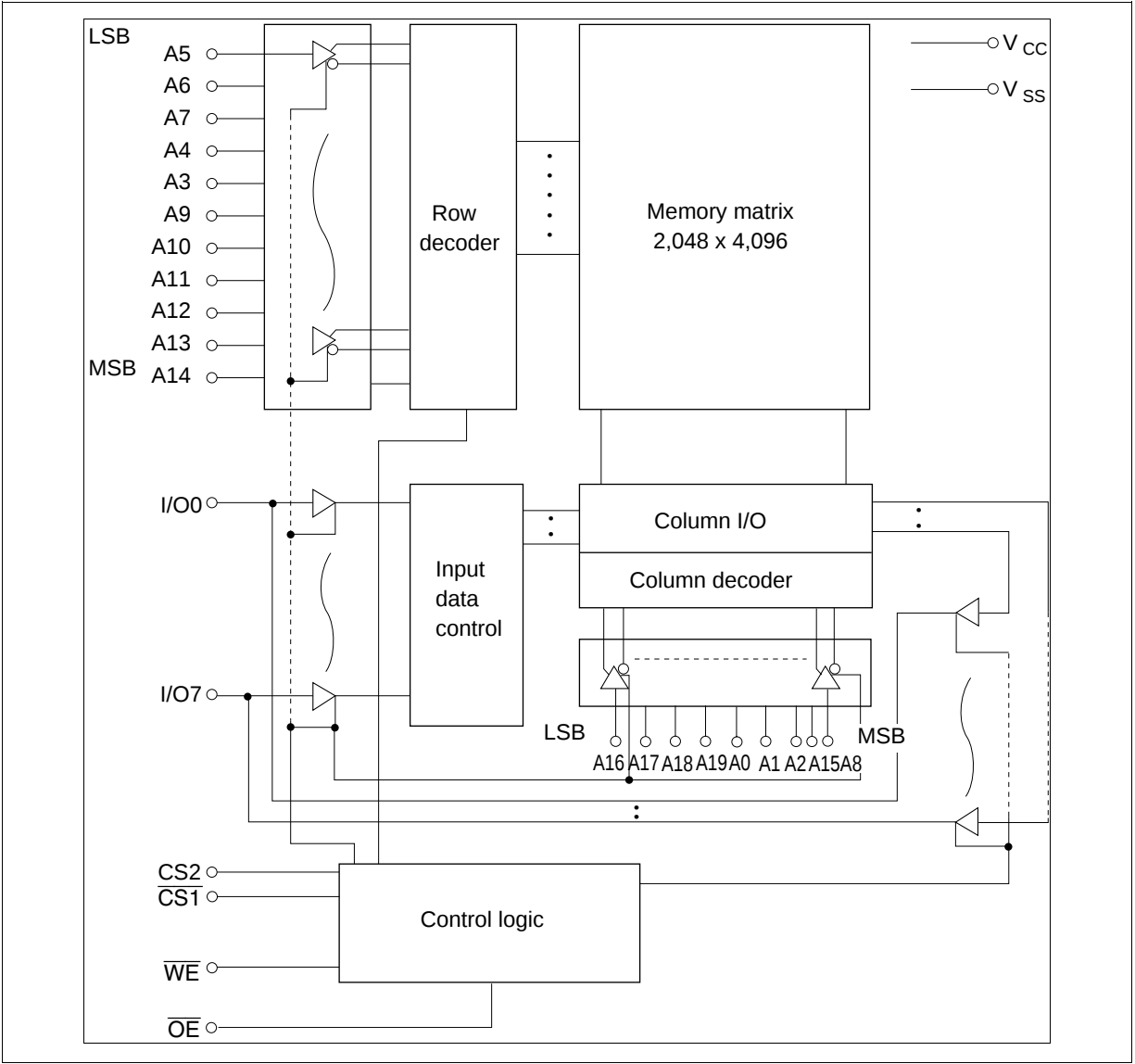
Pin Arrangement



Pin Description (TSOP)

Pin name	Function
A0 to A19	Address input
I/O0 to I/O7	Data input/output
$\overline{\text{CS1}}$	Chip select 1
CS2	Chip select 2
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power supply
V _{SS}	Ground
NC	No connection

Block Diagram (TSOP)



Operation Table

$\overline{\text{CS1}}$	CS2	$\overline{\text{WE}}$	$\overline{\text{OE}}$	I/O0 to I/O7	Operation
H	x	x	x	High-Z	Standby
x	L	x	x	High-Z	Standby
L	H	H	L	Dout	Read
L	H	L	x	Din	Write
L	H	H	H	High-Z	Output disable

Note: H: V_{IH} , L: V_{IL} , x: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to + 7.0	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.3$ * ²	V
Power dissipation	P_T	1.0	W
Storage temperature range	Tstg	-55 to +125	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Notes: 1. V_T min: -3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is +7.0 V.

DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V	
Input low voltage	V_{IL}	-0.3	—	0.8	V	1
Ambient temperature range	Ta	-40	—	85	°C	

Note: 1. V_{IL} min: -3.0 V for pulse half-width ≤ 30 ns.

DC Characteristics

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, or $V_{I/O} = V_{SS} \text{ to } V_{CC}$
Operating current	I_{CC}	—	—	20	mA	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL} , $I_{I/O} = 0 \text{ mA}$
Average operating current	I_{CC1}	—	14	25	mA	Min. cycle, duty = 100%, $I_{I/O} = 0 \text{ mA}$, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, Others = V_{IH}/V_{IL}
	I_{CC2}	—	2	4	mA	Cycle time = 1 μs , duty = 100%, $I_{I/O} = 0 \text{ mA}$, $\overline{CS1} \leq 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$ $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $V_{IL} \leq 0.2 \text{ V}$
Standby current	I_{SB}	—	0.1	0.3	mA	$CS2 = V_{IL}$
Standby current	I_{SB1}	—	0.8	10	μA	$0 \text{ V} \leq V_{in}$ (1) $0 \text{ V} \leq CS2 \leq 0.2 \text{ V}$ or (2) $\overline{CS1} \geq V_{CC} - 0.2 \text{ V}$, $CS2 \geq V_{CC} - 0.2 \text{ V}$
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1 \text{ mA}$
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1 \text{ mA}$

Note: 1. Typical values are at $V_{CC} = 5.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

Capacitance ($T_a = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0 \text{ V}$	1
Input/output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0 \text{ V}$	1

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -40$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{ V} \pm 10\%$, unless otherwise noted.)**Test Conditions**

- Input pulse levels: $V_{IL} = 0.4\text{ V}$, $V_{IH} = 2.2\text{ V}$
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (50 pF) (Including scope and jig)

Read Cycle

		HM628100I			
		-5			
Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	ns	
Address access time	t _{AA}	—	55	ns	
Chip select access time	t _{ACS1}	—	55	ns	
	t _{ACS2}	—	55	ns	
Output enable to output valid	t _{OE}	—	35	ns	
Output hold from address change	t _{OH}	10	—	ns	
Chip select to output in low-Z	t _{CLZ1}	10	—	ns	2, 3
	t _{CLZ2}	10	—	ns	2, 3
Output enable to output in low-Z	t _{OLZ}	5	—	ns	2, 3
Chip deselect to output in high-Z	t _{CHZ1}	0	20	ns	1, 2, 3
	t _{CHZ2}	0	20	ns	1, 2, 3
Output disable to output in high-Z	t _{OHZ}	0	20	ns	1, 2, 3

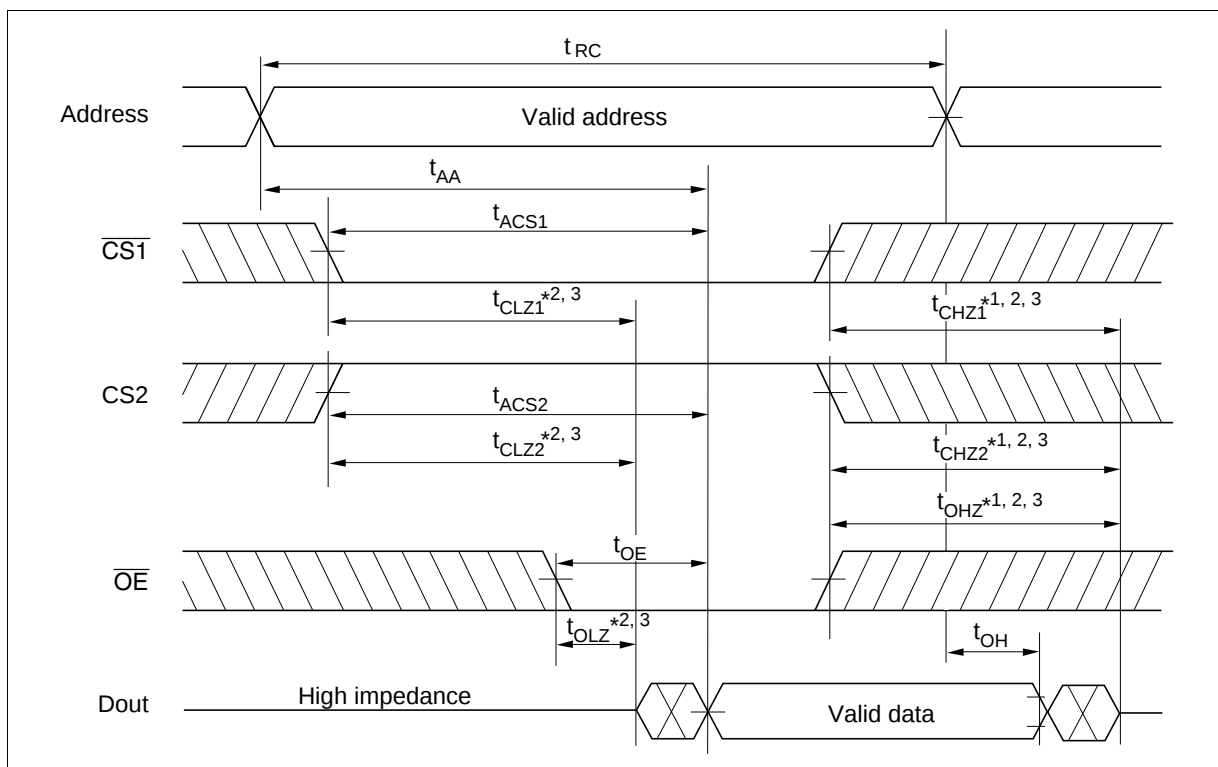
Write Cycle

		HM628100I			
		-5			
Parameter	Symbol	Min	Max	Unit	Notes
Write cycle time	t _{WC}	55	—	ns	
Address valid to end of write	t _{AW}	50	—	ns	
Chip selection to end of write	t _{CW}	50	—	ns	5
Write pulse width	t _{WP}	40	—	ns	4
Address setup time	t _{AS}	0	—	ns	6
Write recovery time	t _{WR}	0	—	ns	7
Data to write time overlap	t _{DW}	25	—	ns	
Data hold from write time	t _{DH}	0	—	ns	
Output active from end of write	t _{OW}	5	—	ns	2
Output disable to output in high-Z	t _{OHZ}	0	20	ns	1, 2
Write to output in high-Z	t _{WHZ}	0	20	ns	1, 2

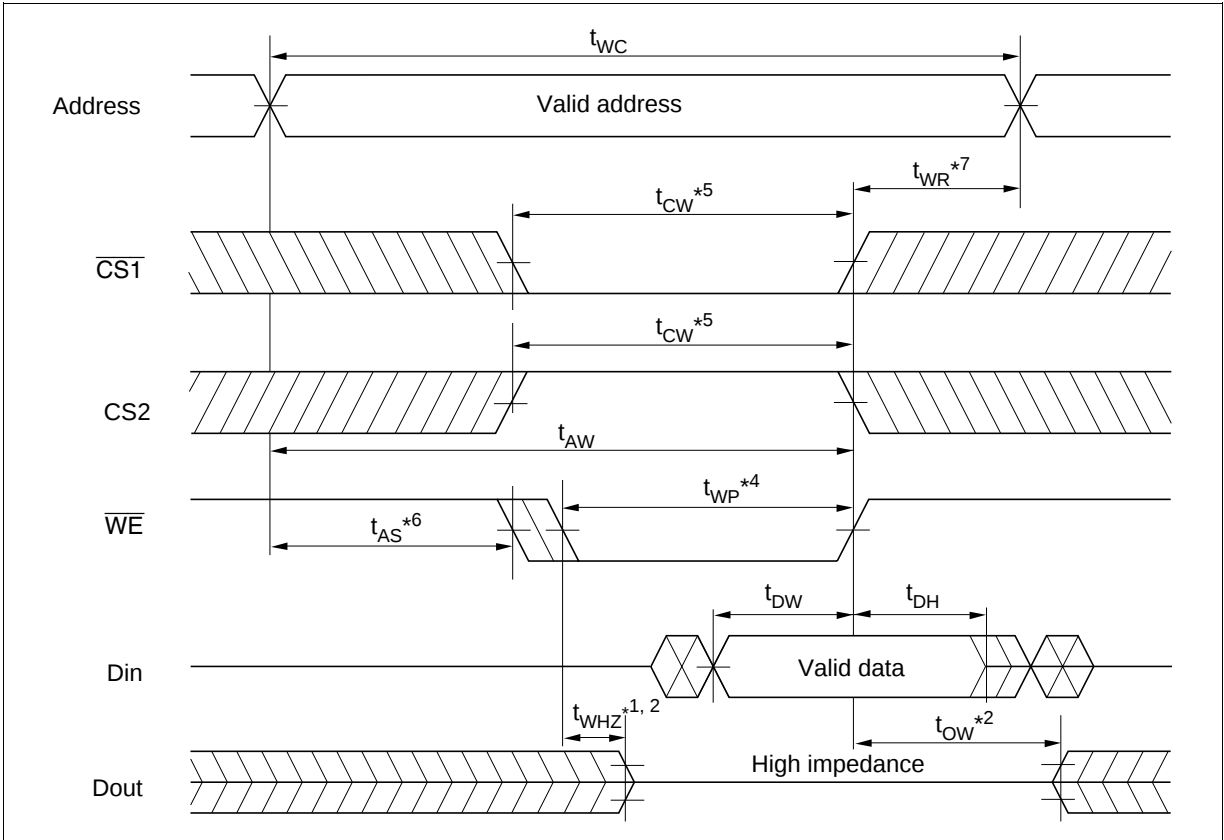
- Notes: 1. t_{CHZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
4. A write occurs during the overlap of a low $\overline{CS1}$, a high CS2, a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high, $\overline{WE}$ going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low, $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
5. t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
6. t_{AS} is measured from the address valid to the beginning of write.
7. t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of write cycle.

Timing Waveform

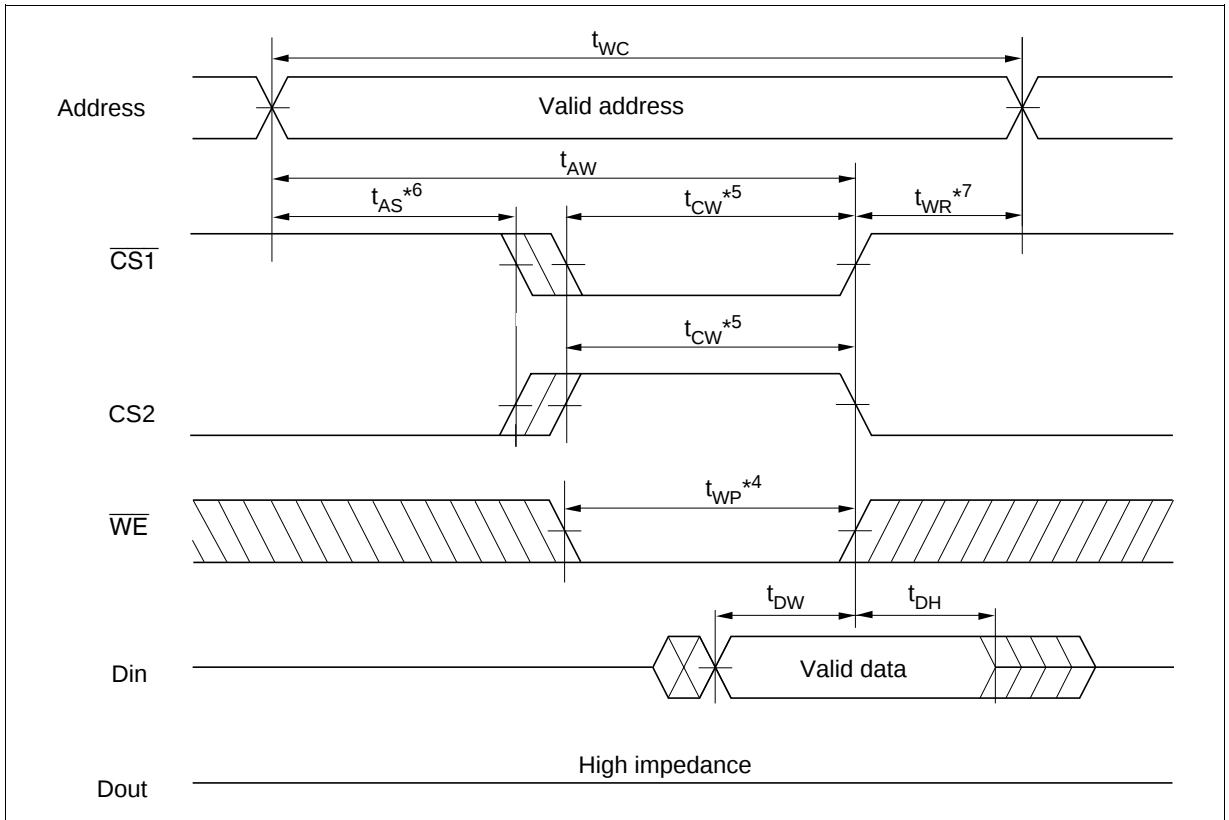
Read Cycle



Write Cycle (1) ($\overline{\text{WE}}$ Clock)



Write Cycle (2) ($\overline{\text{CS}}$ Clock, $\overline{\text{OE}} = V_{\text{IH}}$)



Low V_{CC} Data Retention Characteristics ($T_a = -40$ to $+85^{\circ}\text{C}$)

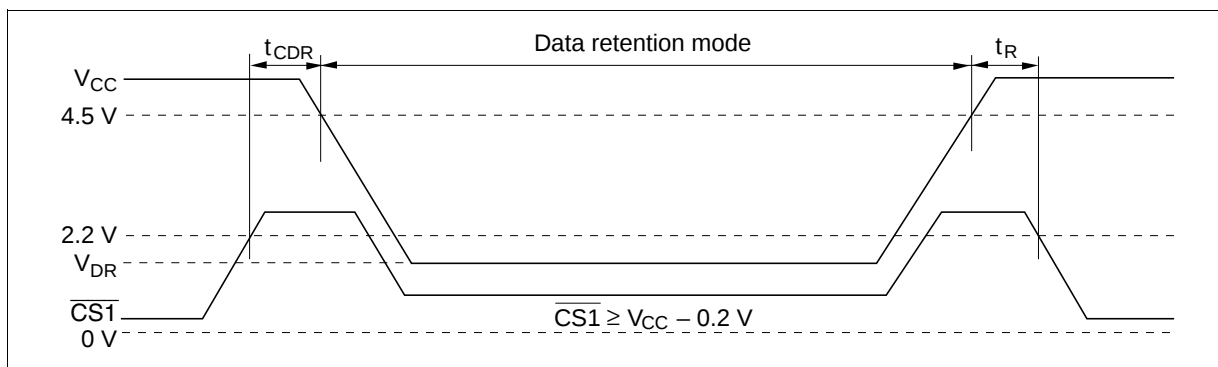
Parameter	Symbol	Min	Typ* ²	Max	Unit	Test conditions* ¹
V_{CC} for data retention	V_{DR}	2.0	—	—	V	$V_{in} \geq 0\text{ V}$ (1) $0\text{ V} \leq \overline{\text{CS2}} \leq 0.2\text{ V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{ V}$, $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{ V}$
Data retention current	I_{CCDR}	—	0.8	10	μA	$V_{CC} = 3.0\text{ V}$, $V_{in} \geq 0\text{ V}$ (1) $0\text{ V} \leq \overline{\text{CS2}} \leq 0.2\text{ V}$ or (2) $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{ V}$, $\overline{\text{CS1}} \geq V_{CC} - 0.2\text{ V}$
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC} * ³	—	—	ns	

Notes: 1. $\overline{\text{CS2}}$ controls address buffer, $\overline{\text{WE}}$ buffer, $\overline{\text{CS1}}$ buffer, $\overline{\text{OE}}$ buffer and Din buffer. If $\overline{\text{CS2}}$ controls data retention mode, V_{in} levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, $\overline{\text{CS1}}$, I/O) can be in the high impedance state. If $\overline{\text{CS1}}$ controls data retention mode, $\overline{\text{CS2}}$ must be $\overline{\text{CS2}} \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq \overline{\text{CS2}} \leq 0.2\text{ V}$. The other input levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, I/O) can be in the high impedance state.

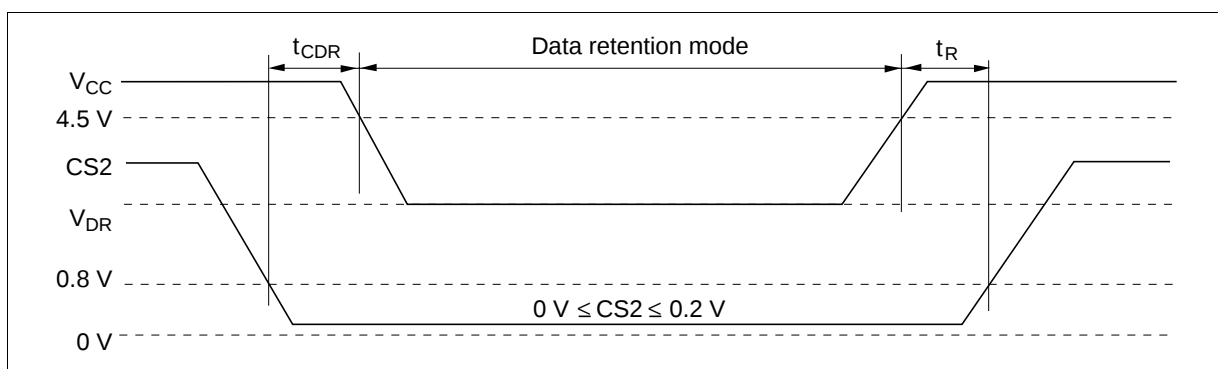
2. Typical values are at $V_{CC} = 3.0\text{ V}$, $T_a = +25^{\circ}\text{C}$ and not guaranteed.

3. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (1) ($\overline{CS1}$ Controlled)



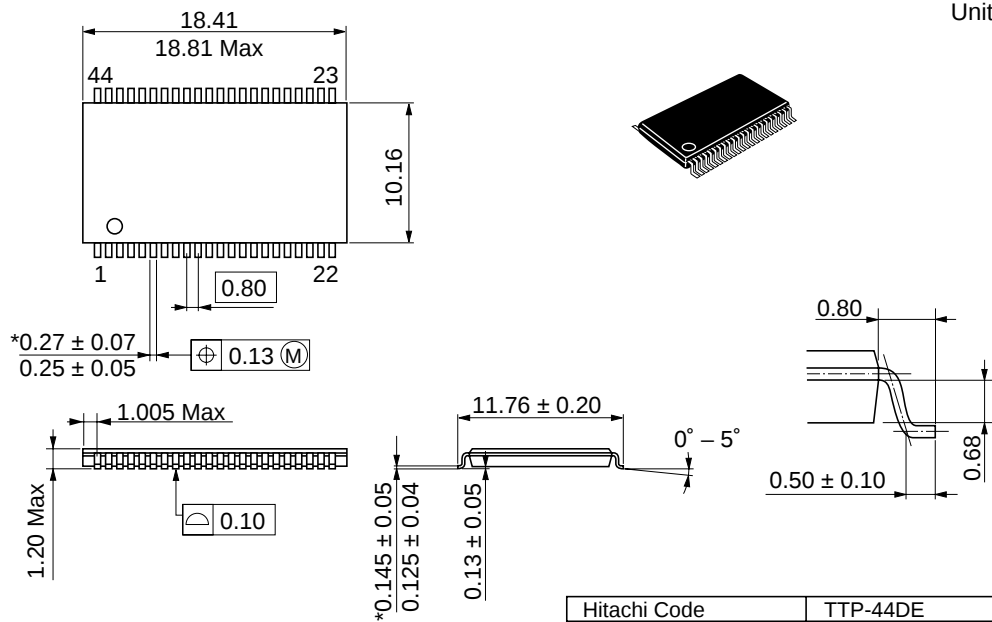
Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Package Dimensions

HM628100LTTI Series (TTP-44DE)

As of January, 2002
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-44DE
JEDEC	—
JEITA	—
Mass (reference value)	0.43 g

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