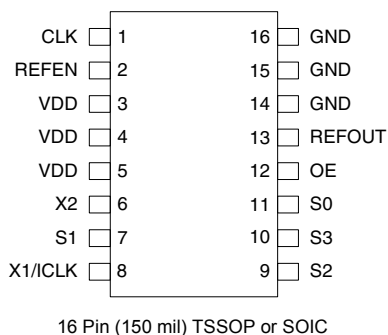


Pin Assignment



Multiplier Select Table

S3	S2	S1	S0	CLK (see note 2 on following page)
0	0	0	0	TEST
0	0	0	1	TEST
0	0	1	0	Input x1
0	0	1	1	Input x3
0	1	0	0	Input x4
0	1	0	1	Input x5
0	1	1	0	Input x6
0	1	1	1	Input x8
1	0	0	0	TEST
1	0	0	1	Crystal osc. pass through (no PLL)
1	0	1	0	Input x2
1	0	1	1	TEST
1	1	0	0	Input x8
1	1	0	1	Input x10
1	1	1	0	Input x12
1	1	1	1	Input x16

0 = connect directly to ground

1 = connect directly to VDD

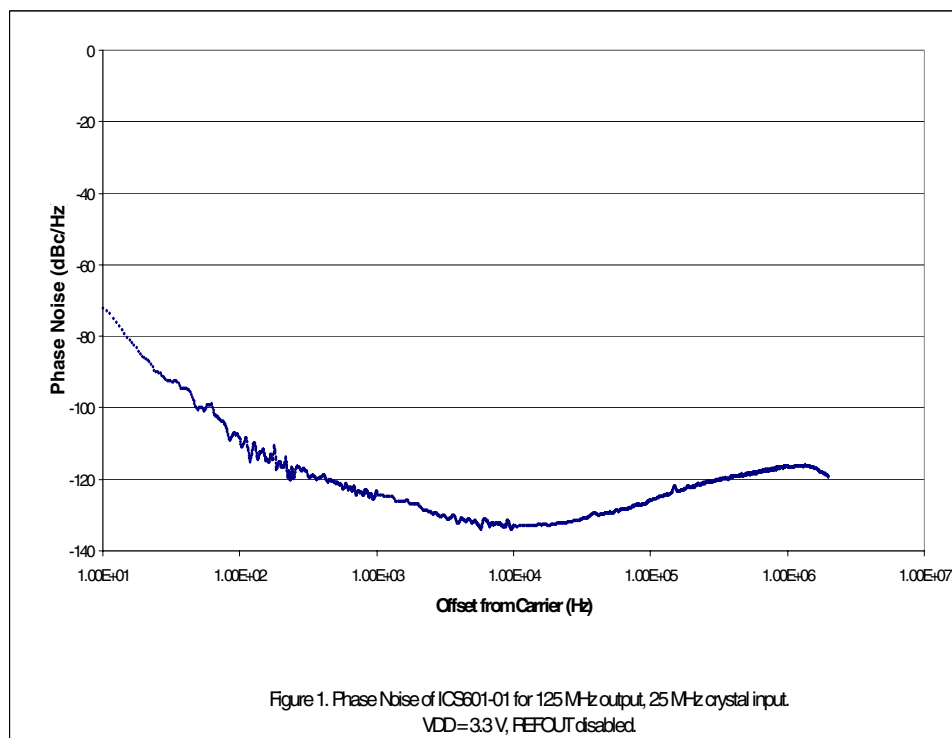
Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	CLK	Output	Clock output from VCO. Output frequency equals the input frequency times multiplier.
2	REFEN	Input	Reference clock enable. Turns off the buffered crystal oscillator clock (stops low) when low.
3	VDD	Power	Connect to +3.3V or +5V. Must match other VDDs.
4	VDD	Power	Connect to +3.3V or +5V. Must match other VDDs.
5	VDD	Power	Connect to +3.3V or +5V. Must match other VDDs.
6	X2	XO	Crystal connection. Connect to a 10 - 27 MHz fundamental parallel mode crystal. Leave disconnected for an external clock input.
7	S1	Input	Multiplier select pin 1. Determines CLK output per table above. Internal pull-up.
8	X1/ICLK	XI	Crystal connection. Connect to a 10 - 27 MHz fundamental parallel mode crystal or clock.
9	S2	Input	Multiplier select pin 2. Determines CLK output per table above. Internal pull-up.
10	S3	Input	Multiplier select pin 3. Determines CLK output per table above. Internal pull-up.
11	S0	Input	Multiplier select pin 0. Determines CLK output per table above. Internal pull-up.
12	OE	Input	Output Enable. Tri-states both output clocks when low. Internal pull-up.
13	REFOUT	Output	Buffered crystal oscillator clock output. Controlled by REFIN.
14 - 16	GND	Power	Connect to ground.

Achieving Low Phase Noise

Figure 1 shows a typical phase noise measurement in a 125 MHz system. There are a few simple steps that can be taken to achieve these levels of phase noise from the ICS601-01. Variations in VDD will increase the phase noise, so it is important to have a stable, low noise supply voltage at the device. Use decoupling capacitors of 0.1 μ F in parallel with 0.01 μ F. It is important to have these capacitors as close as possible to the ICS601-01 supply pins.

Disabling the REFOUT clock is also important for achieving low phase noise; lab tests have shown that this can reduce the phase noise by as much as 10 dBc/Hz.



External Component/Crystal Selection

The ICS601-01 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 μ F and 0.1 μ F should be connected between VDD and GND, as close to the part as possible. A series termination resistor of 33 Ω may be used for each clock output. The crystal must be connected as close to the chip as possible. The crystal should be fundamental mode, parallel resonant. Do not use third overtone. For exact tuning when using a crystal, capacitors should be connected from pins X1 to ground and X2 to ground. In general, the value of these capacitors is given by the following equation, where CL is the crystal load capacitance: Crystal caps (pF) = (CL - 5) x 2. So for a crystal with 16 pF load capacitance, two 22 pF caps can be used. For any given board layout, ICS can measure the board capacitance and recommend the exact capacitance value to use.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS601-01. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Commercial version	0 to +70 °C
Ambient Operating Temperature, Industrial version	-40 to +85 °C
Storage Temperature	-65 to +150 °C
Junction Temperature	125 °C
Soldering Temperature	260 °C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=3.3 V \pm 10%, Ambient temperature -40 to +85°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V _{IH}	X1/ICLK pin only Note 1	VDD/2+1			V
Input Low Voltage	V _{IL}	X1/ICLK pin only Note 1			VDD/2-1	V
Input High Voltage	V _{IH}		2			V
Input Low Voltage	V _{IL}				0.8	V
Output High Voltage	V _{OH}	CMOS level I _{OH} = -4mA	VDD-0.4			V
		I _{OH} = -12mA	2.4			
Output Low Voltage	V _{OL}	I _{OL} = 12mA			0.4	V
Operating Supply Current	IDD	No load, 125 MHz		22	30	mA
Short Circuit Current		Each output	\pm 40	\pm 60		mA
Input Capacitance	C _{IN}	OE, select pins		5		pF

Note 1: Switching occurs nominally at VDD/2

AC Electrical Characteristics

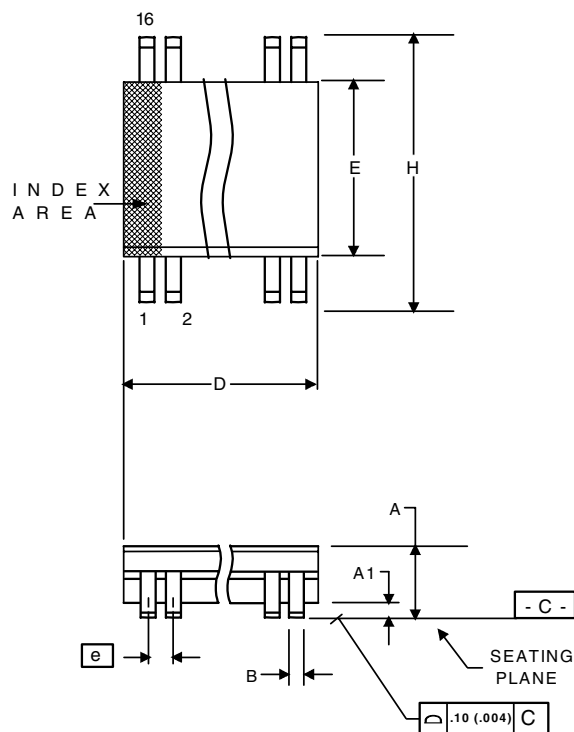
VDD = 3.3V ±10%, Ambient Temperature -40 to +85° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	Fin		10		27	MHz
Output Frequency		at 3.3V or 5V			156	MHz
Output Rise Time	t _{OR}	0.8 to 2.0V no load			1.5	ns
Output Fall Time	t _{OF}	0.8 to 2.0V, no load			1.5	ns
Output Clock Duty Cycle		at VDD/2	45	50	55	%
Maximum Absolute jitter, short term, 125 MHz		No load		±50	±75	ps
Maximum jitter, one sigma, 125 MHz (x5)		No load		12	20	ps
Phase Noise, relative to carrier, 125 MHz (x5)		100 Hz offset	-90	-94		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		1 kHz	-116	-120		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		10 kHz offset	-118	-122		dBc/Hz
Phase Noise, relative to carrier, 125 MHz (x5)		100 kHz offset	-115	-119		dBc/Hz

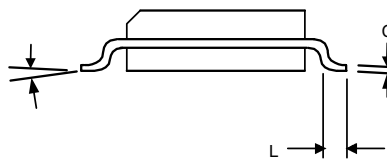
Note 2: Input frequency limited by maximum output frequency and multiplication factor (I.e. For 16x, maximum input frequency is 13.75 MHz).

Package Outline and Package Dimensions (16 pin SOIC, 150 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95

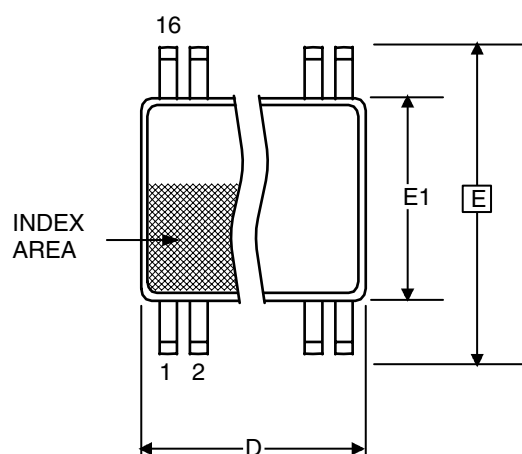


Symbol	SOIC	
	Min	Max
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	9.80	10.00
E	3.80	4.00
e	1.27 BASIC	
H	5.80	6.20
L	0.40	1.27
α	0°	8°

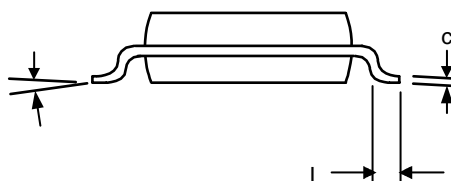
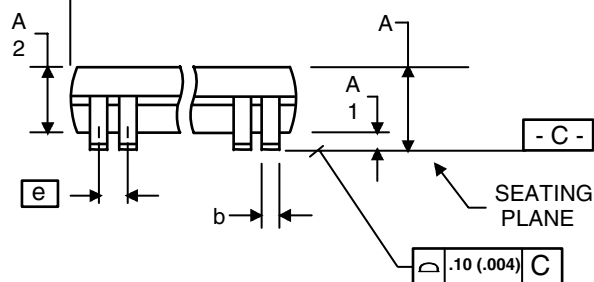


Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°



Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
601M-01LF	ICS601M-01LF	Tubes	16-pin narrow SOIC	0 to 70° C
601M-01LFT	ICS601M-01LF	Tape and Reel	16-pin narrow SOIC	0 to 70° C
601M-01ILF	ICS601M01ILF	Tubes	16-pin narrow SOIC	-40 to 85° C
601M-01ILFT	ICS601M01ILF	Tape and Reel	16-pin narrow SOIC	-40 to 85° C
601G-01LF	601G01LF	Tubes	16-pin TSSOP	0 to 70° C
601G-01LFT	601G01LF	Tape and Reel	16-pin TSSOP	0 to 70° C
601G-01ILF	601G01IL	Tubes	16-pin TSSOP	-40 to 85° C
601G-01ILFT	601G01IL	Tape and Reel	16-pin TSSOP	-40 to 85° C

"L" designates Pb (lead) free package; "I" designates industrial grade.

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