XT55Q1GF

Quad IO Serial NOR Flash

Datasheet

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Serial NOR Flash Memory

1.8V Multi I/O with 4KB, 32KB & 64KB Sector/Block Erase

- **1G-bit Serial Flash**
  - 128M-byte
  - 256 bytes per programmable page
- **Support SFDP table**
- **Standard, Dual, Quad SPI, DTR**
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#, RESET#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#, RESET#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - QPI: SCLK, CS#, IO0, IO1, IO2, IO3
  - SPI/QPI DTR (Double Transfer Rate) Read
- **Flexible Architecture**
  - Sector of 4K-byte
  - Block of 32/64K-byte
- **Advanced security Features**
  - 3 x1024 Bytes Security Registers With OTP Lock
- **Support 128 bits Unique ID**
- **Software/Hardware Write Protection**
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top or Bottom Block Protection
- **Data integrity Check**
  - On-chip ECC (1-bit Correction every 8-byte)
  - CRC detects accidental changes to raw data
- **Package Options**
  - See 1.1 Available Ordering OPN
  - All Pb-free packages are compliant RoHS, Halogen-Free and REACH.
- **Erase/Program Suspend/Resume**
- **Allows XIP (eXecute In Place) operation**
  - High speed Read reduce overall XIP instruction fetch time
- **Continuous Read With 16/32/64-byte Wrap**
- **Temperature Range & Moisture Sensitivity Level**
  - Industrial Level Temperature. (-40 ℃ to +85 ℃), MSL3
  - Industrial Plus Level Temperature. (-40 ℃ to +105 ℃), MSL3
- **Power Consumption**
  - 8uA typ. Deep Power-Down current
- **Single Power Supply Voltage**
  - 1.7~2.0V
- **Endurance and Data Retention**
  - Minimum 100,000 Program/Erase Cycle
  - 20-year Data Retention typical
- **High Speed Clock Frequency**
  - 104MHz for fast read with 30 pF load
  - Dual I/O Data transfer up to 266Mbit/s
  - Quad I/O Data transfer up to 416Mbit/s
  - QPI Mode Data transfer up to 416Mbit/s
  - DTR Quad I/O Data transfer up to 640Mbit/s
- **Program/Erase Speed**
  - Page Program time: 0.4ms typical
  - Sector Erase time: 45ms typical
  - Block Erase time: 0.15s/0.3s typical
  - Chip Erase time: 240s typical

CONTENTS

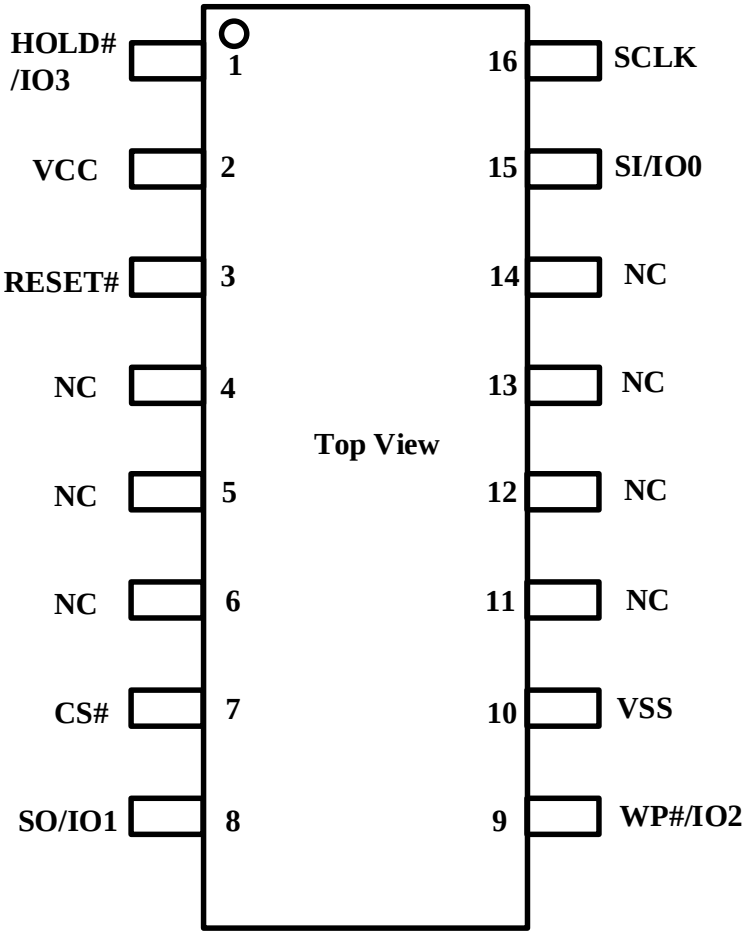
1. GENERAL DESCRIPTION

The XT55Q1GF (1G-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD# / RESET#).

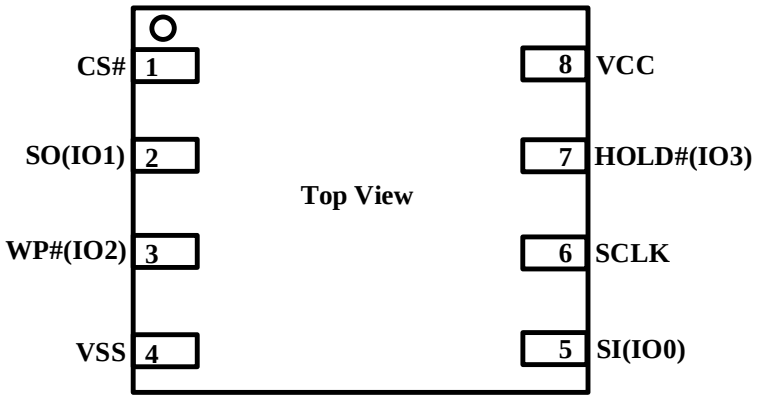
1.1. Available Ordering Part Numbers (OPN)

OPN	Package Type	Package Carrier
XT55Q1GFSFIGA	SOP16 300mil	Tray
XT55Q1GFSFHGA	SOP16 300mil	Tray
XT55Q1GFBGIGA	BGA 24	Tray
XT55Q1GFBGHGA	BGA 24	Tray
XT55Q1GFWSIGA	WSON8 8x6mm	Tray
XT55Q1GFWSHGA	WSON8 8x6mm	Tray

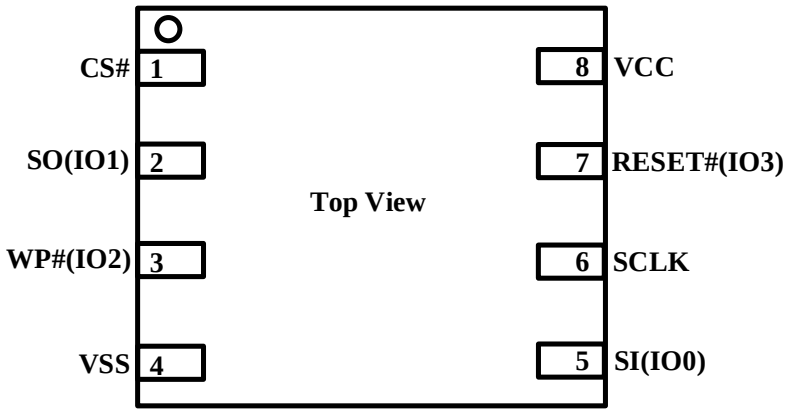
1.2. Connection Diagram



16-pin SOP

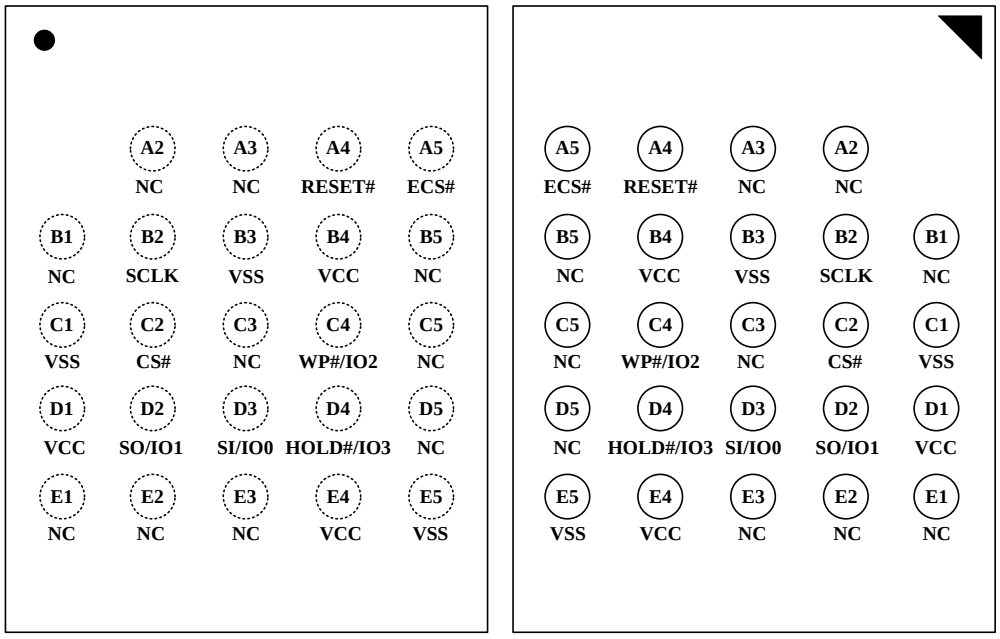


8-pin WSON



8-pin WSON (Default)

Top View **Bottom View**



BGA 24 ball (5x5)

1.3. Pin Description

SOP16 300mil

Pin No.	Pin Name	I/O	Description
1	HOLD#/IO3	I/O	Hold Input / Data Input Output3
2	VCC		Power Supply
3	RESET#	I	Reset Input
4	NC		No Connection
5	NC		No Connection
6	NC		No Connection
7	CS#	I	Chip Select Input
8	SO/IO1	I/O	Data Output/Data Input Output1
9	WP#/IO2	I/O	Write Protect Input/Data Input Output2
10	VSS		Ground
11	NC		No Connection
12	NC		No Connection
13	NC		No Connection
14	NC		No Connection
15	SI/IO0	I/O	Data Input/Data Input Output0
16	SCLK	I	Serial Clock Input

WSON8 8x6mm

Pin No.	Pin Name	I/O	Description
1	CS#	I	Chip Select Input
2	SO (IO1)	I/O	Data Output (Data Input Output 1)
3	WP# (IO2)	I/O	Write Protect Input (Data Input Output 2)
4	VSS		Ground
5	SI (IO0)	I/O	Data Input (Data Input Output 0)
6	SCLK	I	Serial Clock Input
7	HOLD#(IO3) or RESET#(IO3)	I/O	Hold Input (Data Input Output 3, Please contact with XTX) or Reset Input (Data Input Output 3, Default)
8	VCC		Power Supply

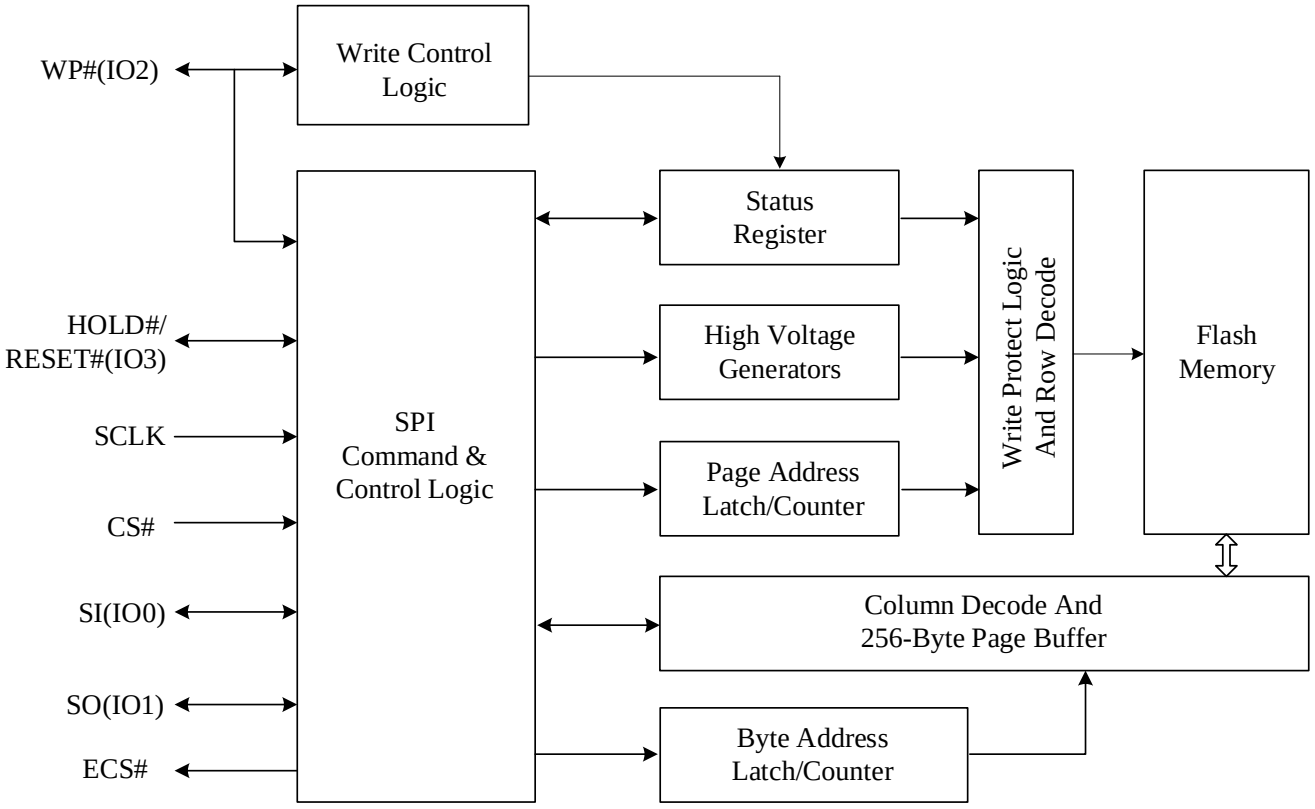
BGA24

Pin No.	Pin Name	I/O	Description
A2	NC		No Connection
A3	NC		No Connection
A4	RESET#	I	Reset Input
A5	ECS#	O	ECC Correction Signal (Open Drain)
B1	NC		No Connection
B2	SCLK	I	Serial Clock Input
B3	VSS		Ground
B4	VCC		Power Supply
B5	NC		No Connection
C1	VSS		Ground
C2	CS#	I	Chip Select Input
C3	NC		No Connection
C4	WP#/IO2	I/O	Write Protect Input/Data Input Output2
C5	NC		No Connection
D1	VCC		Power Supply
D2	SO/IO1	I/O	Data Output/Data Input Output1
D3	SI/IO0	I/O	Data Input/Data Input Output0
D4	HOLD#/IO3	I/O	Hold Input / Data Input Output3
D5	NC		No Connection
E1	NC		No Connection
E2	NC		No Connection
E3	NC		No Connection
E4	VCC		Power Supply
E5	VSS		Ground

Notes:

1. IO0 and IO1 are used for Standard and Dual SPI instructions.
2. IO0 – IO3 are used for Quad SPI instructions, WP# & HOLD# (or Reset#) functions are only available for Standard/Dual SPI.
3. Hardware RESET# pin is available on SOP16 Package, If the hardware reset function is not used, this pin can be left floating or connected to VCC in the system.

1.4. Block Diagram



2. MEMORY ORGANIZATION

Uniform Block Sector Architecture

Block(64K-Byte)	Block(32K-Byte)	Sector(4K-Byte)	Address Range	
2047	4095	32767	07FFF000H	07FFFFFFH
		……	……	……
		32760	07FF8000H	07FF8FFFH
	4094	32759	07FF7000H	07FF7FFFH
		……	……	……
		32752	07FF0000H	07FF0FFFH
2046	4093	32751	07FEF000H	07FEFFFFH
		……	……	……
		32744	07FE8000H	07FE8FFFH
	4092	32743	07FE7000H	07FE7FFFH
		……	……	……
		32736	07FE0000H	07FE0FFFH
……	……	……	……	……
		……	……	……
		……	……	……
1	3	31	0001F000H	0001FFFFH
		……	……	……
		24	00018000H	00018FFFH
	2	23	00017000H	00017FFFH
		……	……	……
		16	00010000H	00010FFFH
0	1	15	0000F000H	0000FFFFH
		……	……	……
		8	00008000H	00008FFFH
	0	7	00007000H	00007FFFH
		……	……	……
		0	00000000H	00000FFFH

3. DEVICE OPERATION

3.1. SPI Mode

Standard SPI

The device features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The device supports Dual SPI operation when using the "Dual Output Fast Read" and "Dual I/O Fast Read" (3BH/3CH and BBH/BCH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The device supports Quad SPI operation when using the "Quad Output Fast Read" (6BH/6CH), "Quad I/O Fast Read" (EBH/ECH), "DTR Fast Read Quad I/O" (EDH/EEH) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

3.2. QPI Mode

The device supports Quad Peripheral Interface (QPI) operations only when the device is switched from Standard/Dual/Quad SPI mode to QPI mode using the "Enable the QPI (38H)" command. The QPI mode utilizes all four IO pins to input the command code. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given times. "Enable the QPI (38H)" and "Disable the QPI (FFH)" commands are used to switch between these two modes. Upon power-up and after software reset using "Enable Chip Reset (66H)" and "Reset (99H)" command, the default state of the device is Standard/Dual/Quad SPI mode. The QPI mode requires the non-volatile Quad Enable bit (QE) in Status Register to be set.

3.3. DTR Read

To effectively improve the read operation throughput without increasing the serial clock frequency, the device introduces multiple DTR (Double Transfer Rate) Read instructions that support Standard/Dual/Quad SPI and QPI modes. The byte-long instruction code is still latched into the device on the rising edge of the serial clock similar to all other SPI/QPI instructions. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of SCLK.

3.4. ECC Function

The ECC Correction Signal (ECS#) pin is provided to the system hardware designers to determine the ECC status during any Read operation. The ECS# pin will be pulled low during any 8-Byte Read data output period in which an ECC event has occurred. ECS# pin can be used to represent SEC (Single Error Correction) event. ECC Correction Signal Output pin is an Open-Drain connection.

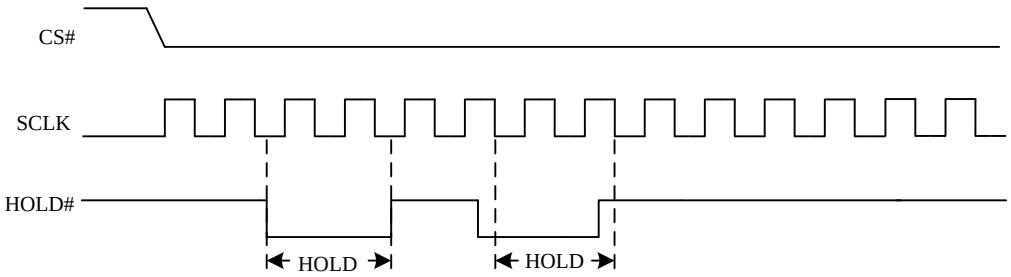
3.5. Hold Function

The HOLD# signal goes low to stop any serial communications with the device, but doesn't stop the operation of writing status register, programming, or erasing in progress.

The operation of HOLD needs CS# keeping low, and starts on the falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK is being low). The HOLD condition ends on the rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK is being low).

The SO is high impedance, and both SI and SCLK don't care during the HOLD operation, if CS# drives high during the HOLD operation, it will reset the internal logic of the device. To re-start the communication with the device, the HOLD# must be at high and then the CS# must be at low.

Hold Condition

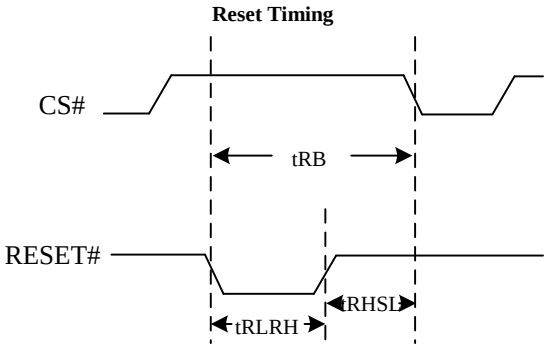


3.6. RESET Function

The RESET# pin allows the device to be reset by the control. The RESET# pin goes low for a period of tRLRH or longer will reset the device. After the reset cycle, the device is at the following states:

- Standby mode.
- All the volatile bits will return to the default status as power on.

Reset Timing



Symbol	Parameter	Min.	Typ.	Max.	Unit
tRLRH	Reset Pulse Width	1			μs
tRHSL	Reset High Time Before CS# Low	40			μs
tRB	Reset Recovery Time (Standby)			50	μs
	Reset Recovery Time (Read)			50	μs
	Reset Recovery Time (Erase)			25	ms
	Reset Recovery Time (Program)			50	μs

3.7. The Reset Signaling Protocol (JEDEC 252)

The protocol consists of two phases: reset request, and completion (a device internal reset).

Reset Request

1. CS# is driven active low to select the device Note1
2. Clock (SCLK) remains stable in either a high or low state Note 2
3. SI / IO0 is driven low by the bus master, simultaneously with CS# going active low Note 3
4. CS# is driven inactive Note 4

Repeat the steps 1-4 each time alternating the state of SI Note 5

Note:

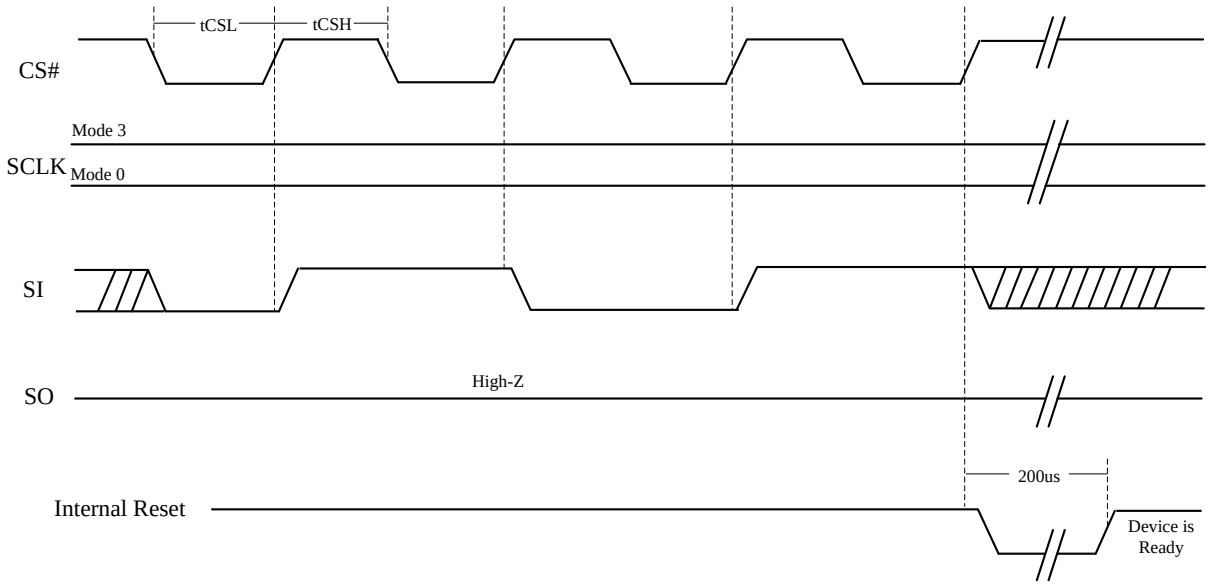
1. This powers up the device.
2. This prevents any confusion with a command, as no command bits are transferred (clocked).
3. No SPI bus slave drives SI during CS# low before a transition of SCLK, i.e., slave streaming output active is not allowed until after the first edge of SCLK.
4. The slave captures the state of SI on the rising edge of CS#.
5. SI is low on the first CS#, high on the second, low on the third, high on the fourth (This provides a 5h pattern, to differentiate it from random noise).

Reset Completion

After the fourth CS# pulse, the slave triggers its internal reset.

Timing Diagram and Timing Parameters

Reset Signaling Protocol



Symbol	Parameter	Min.	Typ.	Max.	Unit
tCSL	CS# Low Time	500			ns
tCSH	CS# High Time	500			ns
	Setup Time	5			ns
	Hold Time	5			ns

4. DATA PROTECTION

The device provides the following data protection methods:

- Write Enable (WREN) command: The WREN command sets the Write Enable Latch (WEL) bit. The WEL bit will return to reset by the following situation:
  - •Power-Up / Software Reset (66H+99H)
  - •Write Disable (WRDI)
  - •Write Status Register (WRSR) / Write Extended Address Register (WEAR) / Write Configuration Register (WCR)
  - •Page Program (PP) / Quad Page Program / Extended Quad Input Fast Program
  - •Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
  - •Erase Security Register / Program Security Register
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits, WPS bit define the section of the memory array that can be read but cannot be changed.
- Hardware Protection Mode: WP# goes low to WP# goes low to protect the BP0~BP4 bits, WPS, SRP0 and SRP1 bit.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command (ABH) and software reset (66H+99H).

Table 1. XT55Q1GF Protected area size (WPS=0)

Status bit					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	0	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	2047th	07FF0000h-07FFFFFFh	64KB	Upper 1/2048
0	0	0	1	0	2046th~2047th	07FE0000h-07FFFFFFh	128KB	Upper 1/1024
0	0	0	1	1	2044th~2047th	07FC0000h-07FFFFFFh	256KB	Upper 1/512
0	0	1	0	0	2040th~2047th	07F80000h-07FFFFFFh	512KB	Upper 1/256
0	0	1	0	1	2032nd~2047th	07F00000h-07FFFFFFh	1MB	Upper 1/128
0	0	1	1	0	2016th~2047th	07E00000h-07FFFFFFh	2MB	Upper 1/64
0	0	1	1	1	1984th~2047th	07C00000h-07FFFFFFh	4MB	Upper 1/32
0	1	0	0	0	1920th~2047th	07800000h-07FFFFFFh	8MB	Upper 1/16
0	1	0	0	1	1792nd~2047th	07000000h-07FFFFFFh	16MB	Upper 1/8
0	1	0	1	0	1536th~2047th	06000000h-07FFFFFFh	32MB	Upper 1/4
0	1	0	1	1	1024th~2047th	04000000h-07FFFFFFh	64MB	Upper 1/2
1	0	0	0	1	0th	00000000h-0000FFFFh	64KB	Lower 1/2048
1	0	0	1	0	0th~1st	00000000h-0001FFFFh	128KB	Lower 1/1024
1	0	0	1	1	0th~3rd	00000000h-0003FFFFh	256KB	Lower 1/512
1	0	1	0	0	0th~7th	00000000h-0007FFFFh	512KB	Lower 1/256
1	0	1	0	1	0th~15th	00000000h-000FFFFFh	1MB	Lower 1/128
1	0	1	1	0	0th~31st	00000000h-001FFFFFh	2MB	Lower 1/64
1	0	1	1	1	0th~63rd	00000000h-003FFFFFh	4MB	Lower 1/32
1	1	0	0	0	0th~127th	00000000h-007FFFFFh	8MB	Lower 1/16
1	1	0	0	1	0th~255th	00000000h-00FFFFFFh	16MB	Lower 1/8
1	1	0	1	0	0th~511th	00000000h-01FFFFFFh	32MB	Lower 1/4
1	1	0	1	1	0th~1023rd	00000000h-03FFFFFFh	64MB	Lower 1/2
X	1	1	X	X	ALL	00000000h-07FFFFFFh	128MB	ALL

Table 2. XT55Q1GF Individual Block Protection (WPS=1)

Table 3. lock	Sector	Address range		Individual Block Lock Operation
2047	32767	07FFF000H	07FFFFFFH	**The Top/Bottom block is protected by sector.** **Other 2046 Blocks are protected by block.** **Block Lock:** 36H+Address **Block Unlock:** 39H+Address **Read Block Lock:** 3DH+Address **Global Block Lock:** 7EH **Global Block Unlock:** 98H
	……	……	……	
	32752	07FF0000H	07FF0FFFH	
……				
……				
2				
1				
0	15	0000F000H	0000FFFFH	
	……	……	……	
	0	00000000H	00000FFFH	

5. STATUS REGISTER

Status Register-1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	**BP4**	**BP3**	**BP2**	**BP1**	**BP0**	**WEL**	**WIP**
Status Register Protection bit	Block Protect bit	Block Protect bit	Block Protect bit	Block Protect bit	Block Protect bit	Write Enable Latch	Erase/Write In Progress
Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Non-volatile	Volatile Read Only	Volatile Read Only
0	0	0	0	0	0	0 = Disable 1= Enable	0 = No busy 1 = Busy

Status Register-2

S15	S14	S13	S12	S11	S10	S9	S8
SUS1	**WPS**	**LB3**	**LB2**	**LB1**	**SUS2**	**QE**	**ADS**
Erase Suspend	Write protection selection	Security Register Lock bit	Security Register Lock bit	Security Register Lock bit	Program Suspend	Quad Enable	Current Address Mode
Volatile Read Only	Non-volatile	Non-volatile (OTP)	Non-volatile (OTP)	Non-volatile (OTP)	Volatile Read Only	Non-volatile	Volatile Read Only
0 = Non-suspend 1 = Suspend	0	0	0	0	0 = Non-suspend 1 = Suspend	0	0 = 3-Byte Add 1 = 4-Byte Add

Status Register-3

S23	S22	S21	S20	S19	S18	S17	S16
LC1	**DRV1**	**DRV0**	**ADP**	**EE**	**PE**	**LC0**	**SRP1**
Latency Code	Output Driver Strength	Output Driver Strength	Power Up Address Mode	Erase Error bit	Program Error bit	Latency Code	Status Register Protection bit
Non-volatile Writable	Non-volatile	Non-volatile	Non-volatile	Volatile Read Only	Volatile Read Only	Non-volatile Writable	Non-volatile
0	1	0	0	0 = Successful 1 = Erase Error	0 = Successful 1 = Program Error	0	0

Extended Address Register

EA7	EA6	EA5	EA4	EA3	EA2	EA1	EA0
SEC	**Reserved**	**Reserved**	**DLP**	**Reserved**	**A26**	**A25**	**A24**
Single Error Bit	Reserved	Reserved	Data Learning Pattern enable Bit	Reserved	Address Bit	Address Bit	Address Bit
Volatile Read Only	Reserved	Reserved	Volatile Writable	Reserved	Volatile Writable	Volatile Writable	Volatile Writable
0 = No ECC events 1 = ECC events	0	0	0	0	0	0	0

Configuration Register

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
CRC1	**CRC0**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**ECC**
Cyclic Redundancy Check bit	Cyclic Redundancy Check bit	Reserved	Reserved	Reserved	Reserved	Reserved	ECC Enabled
Non-volatile	Non-volatile	Reserved	Reserved	Reserved	Reserved	Reserved	Read Only
1	1	0	0	0	0	0	Fixed to 1

Note: For the initial delivery state, all Status Register bits except S22/CR0/CR6/CR7 bits are 0, S22/CR0/CR6/CR7 bits are 1.

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1) becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set.

SRP0, SRP1 bits.

The Status Register Protect (SRP) bits are non-volatile Read/Write bits in the status register. The SRP bits control the method of write protection: software protection, hardware protection.

Status Register Protect (SRP) bits

SRP1	SRP0	WP#	Status Register	Description
0	0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1. (Default)
0	1	0	Hardware Protected	WP#=0, the Status Register locked and cannot be written to.
0	1	1	Hardware Unprotected	WP#=1, the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle. Note 1
1	1	X	One-Time Program Note 2	Status Register is protected and cannot be written to.

Status Register Protect (SRP) bits (QE=1 fixed)

SRP1	SRP0	Status Register	Description
0	0	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1. (Default)
1	0	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next Power-Down, Power-Up cycle. Note 1
1	1	One-Time Program Note 2	Status Register is protected and cannot be written to.

NOTE:

1. When SRP1, SRP0= (1, 0), a Power-Down, Power-Up cycle will change SRP1, SRP0 to (0, 0) state.
2. This feature is available on special order. Please contact XTX for details.

ADS bit.

The Address Status (ADS) bit is a read only bit that indicates the current address mode the device is operating in. The device is in 3-Byte address mode when ADS=0 (default), and in 4-Byte address mode when ADS=1.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# (or RESET#) pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# (or RESET#) pins are tied directly to the power supply or ground).

SUS1, SUS2 bits.

The SUS1 and SUS2 bits are read only bit in the status register (S15 and S10) that are set to 1 after executing an Program/Erase Suspend (75H) command (The Erase Suspend will set the SUS1 to 1, and the Program Suspend will set the SUS2 to 1). The SUS1 and SUS2 bits are cleared to 0 by Program/Erase Resume (7AH) command, software reset (66H+99H) command as well as a power-down, power-up cycle.

LB1, LB2, LB3 bits.

The LB1-LB3 bits are non-volatile One Time Program (OTP) bits in Status Register (S11-S13) that provide the write protect control and status to the Security Registers. The default state of LB1-LB3 bits are 0, the security registers are unlocked. The LB1-LB3 bits can be set to 1 individually using the Write Register instruction. The LB1-LB3 bits are One Time Programmable, once being set to 1, the corresponding Security Register will become read-only permanently.

WPS bit.

The WPS Bit is used to select which Write Protect scheme should be used. When WPS=0, the device will use the combination of T/B, BP (3:0) bits to protect a specific area of the memory array. When WPS=1, the device will utilize the Individual Block Locks to protect any individual sector or blocks. The default value for all Individual Block Lock bits is 1 upon device power on or after reset.

Note: When WPS=1, Global Block Unlock (98H) command is needed before executing chip erase operation.

LC0, LC1 bits.

The Latency Code (LC) selects the mode and number of dummy cycles between the end of address and the start of read data output for BBH/BCH_SPI, EBH/ECH_SPI, 0DH_QPI, BDH_SPI, EDH/EEH_SPI and EDH/EEH_QPI.

Some read commands send mode bits following the address to indicate that the next command will be of the same type with an implied, rather than an explicit instruction. The next command thus does not provide an instruction Byte, only a new address and mode bits. This reduces the time needed to send each command when the same command type is repeated in a sequence of commands.

Dummy cycles provide additional latency that is needed to complete the initial read access of the flash array before data can be returned to the host system. Some read commands require additional latency cycles as the SCLK frequency is increased.

Latency Code and DTR Mode Frequency Table

LC1(1)	LC0(1)	Dummy clock cycles
0	0	8 (Default)
0	1	6
1	0	12
1	1	16(2)(3)

Note:

1. This value is Non-Volatile, so it will not change after power-on and reset, unless the user modifies it by writing the status register instruction.
2. The number of dummy clocks for BBH/BCH/EBH/ECH/EEH at SPI mode and EEH at QPI mode will be set by LC bit in status register, the number of dummy clocks can be configured as either 8/6/12/16 (default = 8).
3. The number of dummy clocks for BDH/EDH at SPI mode and 0DH/EDH at QPI mode will be set by LC bit in status register, the number of dummy clocks can be configured as either 8/6/12 (default = 8).

PE bit.

The Program Error (PE) bit is a read only bit that indicates a program failure. It will also be set when the user attempts to program a protected array sector or access the locked OTP space. If the program operation times out, the write enable latch bit is reset and the program error bit is set to 1. Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

Note: The PE bit can only be accessed when WIP=0. The PE bit can also be reset at the next program operation.

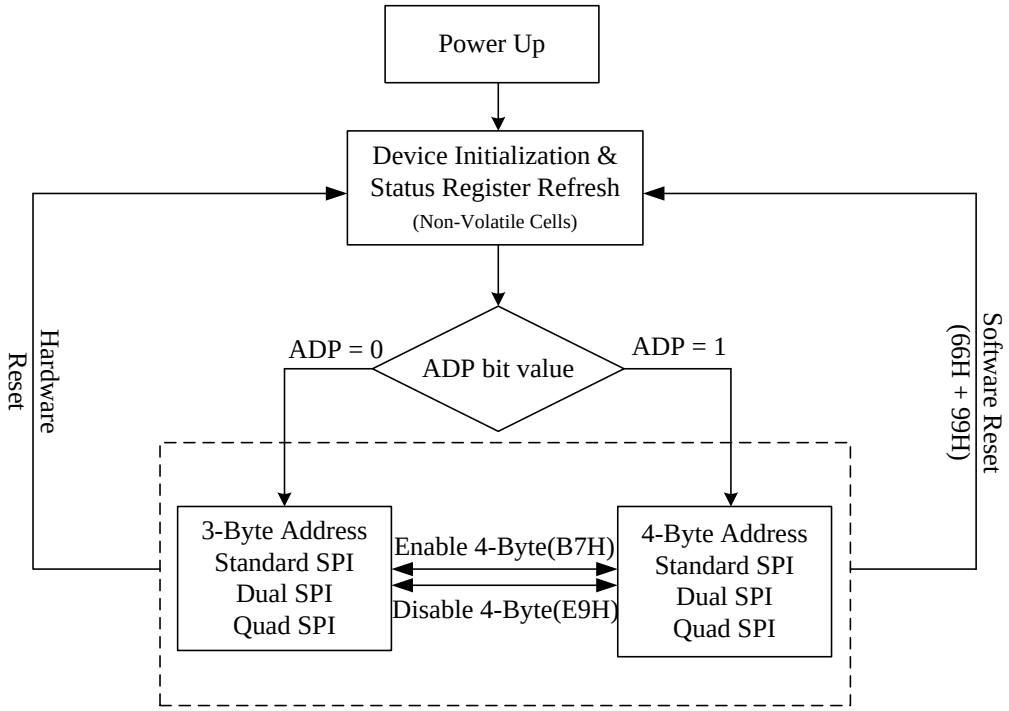
EE bit.

The Erase Error (EE) bit is a read only bit that indicates an erase failure. It will also be set when the user attempts to erase a protected array sector or access the locked OTP space. If the erase operation times out, the write enable latch bit is reset and the Erase error bit is set to 1. Error bits can be reset by CLEAR FLAG STATUS REGISTER command (30H).

Note: The EE bit can only be accessed when WIP=0. The EE bit can also be reset at the next erase operation.

ADP bit.

The Address Power-up (ADP) bit is a non-volatile writable bit that determines the initial address mode when the device is powered on or reset. This bit is only used during the power on or device reset initialization period. When ADP=0(factory default), the device will power up into 3-Byte address mode, the Extended Address Register must be used to access memory regions beyond 128Mb. When ADP=1, the device will power up into 4-Byte address mode directly.



DRV1, DRV0 bits.

The Output Driver Strength (DRV1 & DRV0) bits are used to determine the output driver strength for the Read operations.

DRV1	DRV0	Driver Strength
0	0	25%
0	1	50%
1	0	75% (Default)
1	1	100%

Address bits.

The Extended Address Bits A26, A25, A24 are used only when the device is operating in the 3-Byte Address Mode (ADS=0), which are volatile writable by Write Extended Address Register command (C5H). The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0).

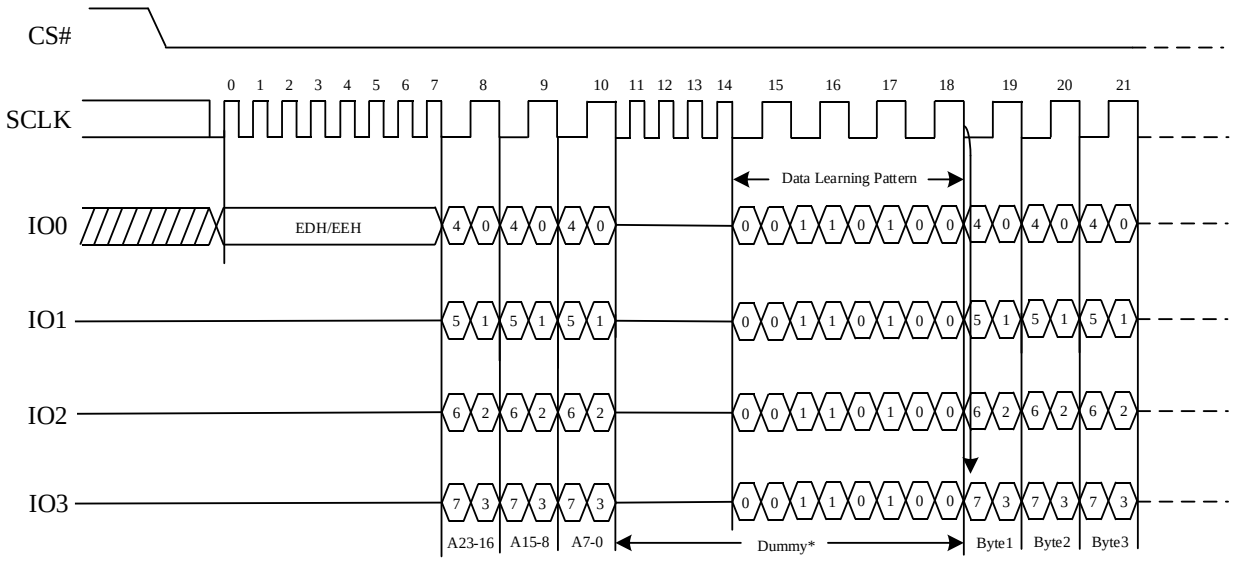
If the device powers up with ADP bit set to 1, or an "Enter 4-Byte Address Mode (B7H)" instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bits setting will be ignored. However, any instruction with 4-Byte address input will replace the Extended Address Bits with new settings.

A26, A25, A24	Address Range
000	0000 0000H – 00FF FFFFH
001	0100 0000H – 01FF FFFFH
010	0200 0000H – 02FF FFFFH
011	0300 0000H – 03FF FFFFH
100	0400 0000H – 04FF FFFFH
101	0500 0000H – 05FF FFFFH
110	0600 0000H – 06FF FFFFH
111	0700 0000H – 07FF FFFFH

DLP bit.

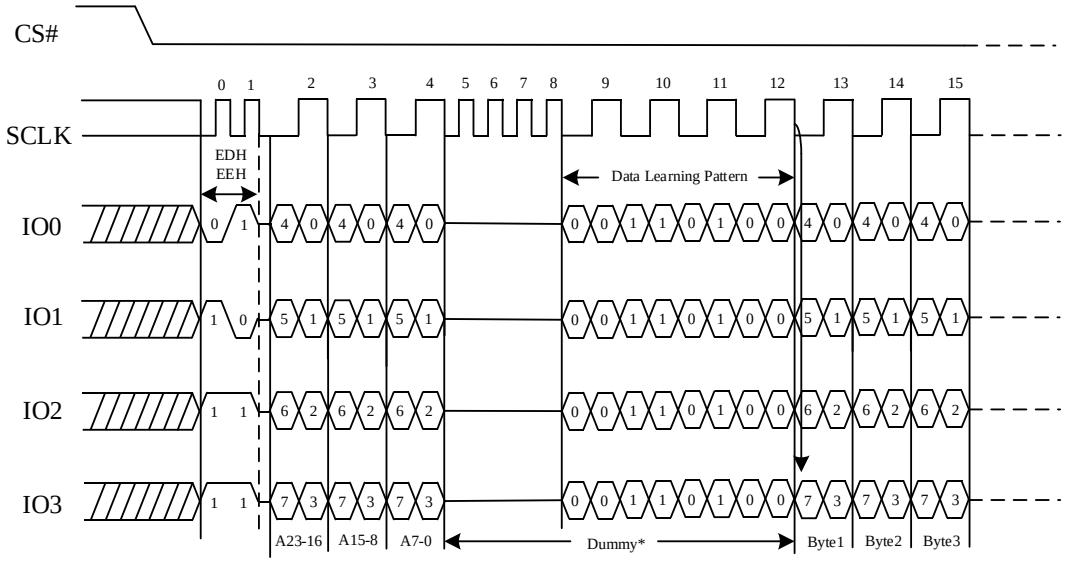
The DLP bit is Data Learning Pattern Enable bit. For DTR Fast Read Quad I/O command (EDH/EEH), a pre-defined "Data Learning Pattern" can be used by the flash memory controller to determine the flash data output timing on 4 I/O pins. When DLP=1, during the last 4 dummy clocks just prior to the data output, the flash will output "00110100" Data Learning Pattern sequence on each of the 4 I/O pins. During this period, controller can fine tune the data latching timing for each I/O pins to achieve optimum system performance. DLP=0 will disable the Data Learning Pattern output.

DLP Sequence Diagram



* The number of dummy clocks can be set by LC bit

DLP Sequence Diagram (QPI)



* The number of dummy clocks can be set by LC bit

SEC bit.

SEC (Single Error Correction) Status Bit are used to show the ECC results for the last Read operation. SEC bit will be cleared to 0 once the device accepts a new Read command

SEC	Definitions
0	No ECC Events in all aligned 8-Byte granularities
1	SEC events in single or multiple 8-Byte granularities, and the data is ok to use. (Unless it contains more than one odd bit errors in8-Byte granularity)

ECC bit.

ECC (Error Correction Codes) Status Bit is used to configuration the ECC function for prevent the data storage errors. ECC Status Bit is set to 1 by default in the factory, which is fixed and cannot be reset to 0, therefore the ECC function is always on.

CRC0, CRC1 bits.

CRC0 and CRC1 (Cyclic Redundancy Check bit) Status bits are used to configure the CRC chunk size for prevent the data transmission errors.

Function	CRC1	CRC0	Definitions
CRC configuration	1	1	CRC Disabled (Default)
	1	0	16-Byte CRC
	0	1	32-Byte CRC
	0	0	64-Byte CRC

6. DATA INTEGRITY CHECK

The data storage and transmission errors will cause unexpected Flash device variation that makes a harmful impact on overall system functions. To prevent these errors, the device provides advanced Data Integrity Check function. For the data storage and data transmission in the flash device, Data Integrity Check can check errors and correct them, allowing self-checking and preventing errors in advance.

The Data Integrity Check function includes two methods:

- ECC (Error Correction Codes): to prevent the data storage errors.
- CRC (Cyclic Redundancy Check): to prevent the data transmission errors.

The register data and software signals can also be used to associate the Data Integrity Check function to fully record the results of checking, and can also immediately feedback.

6.1. ECC (Error Correction Codes)

Error Correction Codes (ECC) is a commonly used technique in non-volatile memory to reduce the device Bit Error Rate (BER) during the device operation life and improve device reliability. To achieve error detection and correction, redundancy data must be added to store the ECC calculation results for a given length of data. In XT55Q1GF every aligned 8-Byte data stored in the memory array will be checked by the internal ECC engine using SEC (Single Error Correction) Hsiao Codes algorithm. With 8-Byte ECC data granularity, ECC calculation latency time can be minimized and higher level of data integrity can be preserved.

The default value of all memory data is FFH (Erased) when the device is shipped from the factory. A “Page Program (02H/12H)” or “Quad Page Program (32H/34H)” or “Extended Quad Page Program (C2H/3EH)” command can be used to program the user data into the memory array. ECC calculation will be performed during the internal programming operation and the results are stored in the redundancy or spare area of the memory array. It is necessary to program every page in aligned 8-Byte granularity so that ECC engine can store the correct ECC information. It is also required that every aligned 8-Byte data granularity can only be programmed once to avoid additional ECC calculation in the same granularity resulting incorrect ECC results. A technique previously known as “Incremental Byte/Bit Programming to the same Byte location” cannot be used for the device when ECC is enabled. During data read operations, the internal ECC engine will check the ECC results stored in the spare area and apply necessary error correction or error detection to the main array data being read out. It is necessary to check the ECC Status Bits (SEC) in the Status Register after every Read operation to see if the data read out contains one bit error or not. A Read operation can start from any Byte address and continue through the entire memory array, so it is not necessary to align the 8-Byte granularity boundary address to start a Read command.

Additional hardware monitoring of the ECC status can also be used to observe the ECC status in real time during any data output. When configured, the ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC event.

The SEC bit can be reset through anyone of the following situations:

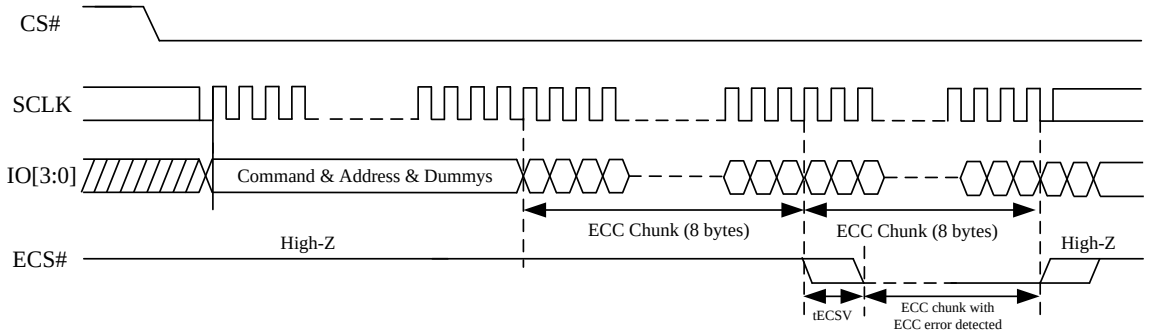
- Sending a new Read Command
- Issuing Software Reset Command
- Hardware Reset
- Power-up cycle

6.2. ECS# (Error corrected Signal) Pin

The ECS# pin is a real time hardware signal to feedback the ECC correction status. The ECS# pin is designed as an open drain structure and a pull-up resistor is required. In normal situation, the ECS# is kept on High-Z state. Once error correction begins, the ECS# pin will pull low during the whole ECC chunk unit after a duration of tECSV delay timing.

The ECS# (ECC Correction Signal) pin will be pulled low during any aligned 8-Byte data output if it contains SEC (Single Error Correction) event.

Figure 1. ECS# Timing



6.3. Parity Check (CRC)

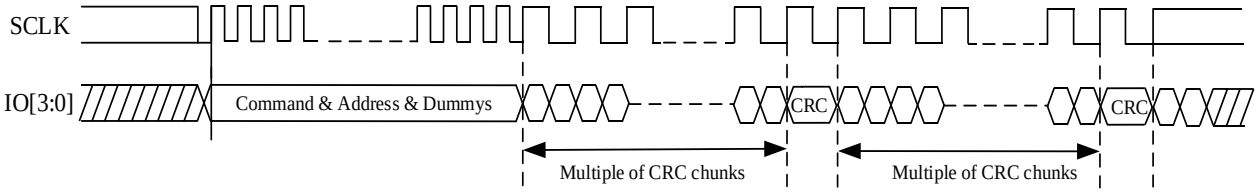
The parity check function can only be operated in DTR Fast Read Quad I/O mode. The Extended REGISTER (bit5-bit4) can set the parity check function.

For read operation after the Parity check function is enabled, the data CRC bit should be output by each CRC chunk unit. Otherwise, read CRC code might be error.

The CRC Chunk size can be configured as 16-Byte, 32-Byte, or 64-Byte by the ECC Register setting. However, when the device enters the “Read with Wrap” mode, while the CRC function is also enabled, and the CRC Chunk size will be set to be identical with the Wrap Length (16-Byte, 32-Byte, or 64-Byte) by internal circuitry. Only when the device is not in the “Read with Wrap” mode, the original CRC Chunk size setting will be restored.

The data CRC Bytes are calculated by exclusive-OR on each I/O bus in the CRC chunk.

Figure 2. CRC Timing



7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See the table below, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must be driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table 4. Commands

Command Name	Command Code	SPI	QPI	Address Byte					Dummy Clock	Data Byte
				Total ADD Byte	Byte1	Byte2	Byte3	Byte4		
Register Access										
Read Status Register_1	05H	√	√	0					0	1 to ∞
Read Status Register_2	35H	√	√	0					0	1 to ∞
Read Status Register_3	15H	√	√	0					0	1 to ∞
Write Status Register_1	01H	√	√	0					0	1 or 2
Write Status Register_2	31H	√	√	0					0	1
Write Status Register_3	11H	√	√	0					0	1
Read Extended Address Register	C8H	√	√	0					0	1 to ∞
Write Extended Address Register	C5H	√	√	0					0	1
Read Configuration Register	B5H	√	√	0					0	1 to ∞
Write Configuration Register	B1H	√	√	0					0	1
Read Manufacturer/Device ID	90H	√	√	3	ADD1	ADD2	ADD3		0	1 to ∞
Read Serial Flash Discoverable Parameters	5AH	√	√	3	ADD1	ADD2	ADD3		8 Note1	1 to ∞
Read Unique ID	4BH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8 Note1	1 to 128bit

Read Identification	9EH/9FH	√	√	0					0	1 to ∞
Array access										
Read Data	03H	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to ∞
Fast Read	0BH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8 Note1	1 to ∞
Dual Output Fast Read	3BH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
Dual I/O Fast Read	BBH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	8/6/12/16Note2/3	1 to ∞
Quad Output Fast Read	6BH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	8	1 to ∞
Quad I/O Fast Read	EBH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8/6/12/16Note1/2/3	1 to ∞
4-Byte Read	13H	√		4	ADD1	ADD2	ADD3	ADD4	0	1 to ∞
4-Byte Fast Read	0CH	√	√	4	ADD1	ADD2	ADD3	ADD4	8 Note1	1 to ∞
4-Byte Dual Output Fast Read	3CH	√		4	ADD1	ADD2	ADD3	ADD4	8	1 to ∞
4-Byte Dual I/O Fast Read	BCH	√		4	ADD1	ADD2	ADD3	ADD4	8/6/12/16Note2/3	1 to ∞
4-Byte Quad Output Fast Read	6CH	√		4	ADD1	ADD2	ADD3	ADD4	8	1 to ∞
4-Byte Quad I/O Fast Read	ECH	√	√	4	ADD1	ADD2	ADD3	ADD4	8/6/12/16Note1/2/3	1 to ∞
4-Byte DTR Quad I/O Fast Read	EEH	√	√	4	ADD1	ADD2	ADD3	ADD4	8/6/12Note5	1 to ∞
DTR Fast Read	0DH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8/6/12 Note5	1 to ∞
DTR Fast Read Dual I/O	BDH	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	8/6/12Note2/5	1 to ∞
DTR Fast Read Quad I/O	EDH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8/6/12Note5	1 to ∞
Page Program	02H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Quad Page Program	32H	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Extended Quad Input Fast Program	C2H	√		3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
4-Byte Page Program	12H	√	√	4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
4-Byte Quad Input Fast Program	34H	√		4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
4-Byte Quad Input Extended Fast Program	3EH	√		4	ADD1	ADD2	ADD3	ADD4	0	1 to 256
4KB Sector Erase	20H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
32KB Block Erase	52H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
64KB Block Erase	D8H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0

Chip Erase	C7/60H	√	√	0					0	0
4-Byte 4KB Sector Erase	21H	√	√	4	ADD1	ADD2	ADD3	ADD4	0	0
4-Byte 32KB Block Erase	5CH	√	√	4	ADD1	ADD2	ADD3	ADD4	0	0
4-Byte 64KB Block Erase	DCH	√	√	4	ADD1	ADD2	ADD3	ADD4	0	0
Device Operations										
Enable Reset	66H	√	√	0					0	0
Reset	99H	√	√	0					0	0
Write Enable	06H	√	√	0					0	0
Write Enable for Volatile Status Register	50H	√	√	0					0	0
Write Disable	04H	√	√	0					0	0
Program Erase Suspend	75H	√	√	0					0	0
Program Erase Resume	7AH	√	√	0					0	0
Enable QPI	38H	√		0					0	0
Disable QPI	FFH		√	0					0	0
Set Burst with Wrap	77H	√		4	Dummy	Dummy	Dummy	W7-W0	0	0
Set Read Parameters	C0H		√	1	P7-P0				0	0
Enter 4-Byte Address Mode	B7H	√	√	0					0	0
Exit 4-Byte Address Mode	E9H	√	√	0					0	0
Clear Flag Status Register Command	30H	√	√	0					0	0
Deep Power-Down	B9H	√	√	0					0	0
Release From Deep Power-Down	ABH	√	√	0					0	0
Release From Deep Power-Down/Read Device ID	ABH	√	√	3	Dummy	Dummy	Dummy	ID7-ID0	0 Note4	1 to ∞
One-Time Programmable (OTP) Operations										
Read Security Register	48H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8 Note1	1 to ∞
Program Security Register	42H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	1 to 256
Erase Security Register	44H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Advanced Sector Protection Operations										

Global Block Lock	7EH	√	√	0					0	0
Global Block Unlock	98H	√	√	0					0	0
Individual Block Lock	36H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Individual Block Unlock	39H	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	0	0
Read Block Lock	3DH	√	√	3(4)	ADD1	ADD2	ADD3	(ADD4)	8 Note4	1

Note:

1. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command. Depending on the Read Parameter bits P[5:4] setting, the number of dummy clocks can be configured as either 8/6/12/16 (default = 8).
2. M7-0 is counted for dummy clocks.
3. The number of dummy clocks for BBH/BCH/EBH/ECH at SPI mode will be set by LC bit in status register, the number of dummy clocks can be configured as either 8/6/12/16 (default = 8).
4. In QPI mode, the number of dummy clocks of ABH_QPI is 6, and 3DH_QPI is 8.
5. The number of dummy clocks for BDH/EDH/EEH at SPI mode and 0DH/EDH/EEH at QPI mode will be set by LC bit in status register, the number of dummy clocks can be configured as either 8/6/12 (default = 8).

7.1. Clock Frequencies

Number of Dummy Clocks	Dual I/O Fast Read At SPI (BBH/BCH)	Quad I/O Fast Read At SPI (EBH/ECH)	Fast Read At QPI (0BH/0CH)	Quad I/O Fast Read At QPI (EBH/ECH)
8(Default)	104 MHz @ 85 ℃ 96MHz @ 105 ℃	96 MHz	96 MHz	96 MHz
6	84 MHz	72 MHz @ 85 ℃ 64 MHz @ 105 ℃	72 MHz @ 85 ℃ 64 MHz @ 105 ℃	72 MHz @ 85 ℃ 64 MHz @ 105 ℃
12	133 MHz	104 MHz	104 MHz	104 MHz
16	133 MHz	104 MHz	104 MHz	104 MHz

Number of Dummy Clocks	DTR Fast Read At QPI (0DH)	DTR Fast Read Dual I/O At SPI (BDH)	DTR Quad I/O Fast Read At SPI (EDH/EEH)	DTR Quad I/O Fast Read At QPI (EDH/EEH)
8(Default)	60 MHz	60 MHz	60 MHz	60 MHz
6	50 MHz	50 MHz	50 MHz	50 MHz
12	80 MHz	80 MHz	80 MHz	80 MHz

Note:

1. Values are guaranteed by characterization and not 100% tested in production.

7.2. Table of Device ID Definitions

Operation Code	MID7-MID0	ID15-ID8	ID7-ID0
9FH	0B	60	1B
90H	0B		1A
ABH			1A

7.3. Register Access

7.3.1. Read Status Register (05H or 35H or 15H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register can be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code "05H", the SO will output Status Register bits S7~S0. For the command code "35H", the SO will output Status Register bits S15~S8. For the command code "15H", the SO will output Status Register bits S23~S16.

Figure 3. Read Status Register Sequence Diagram

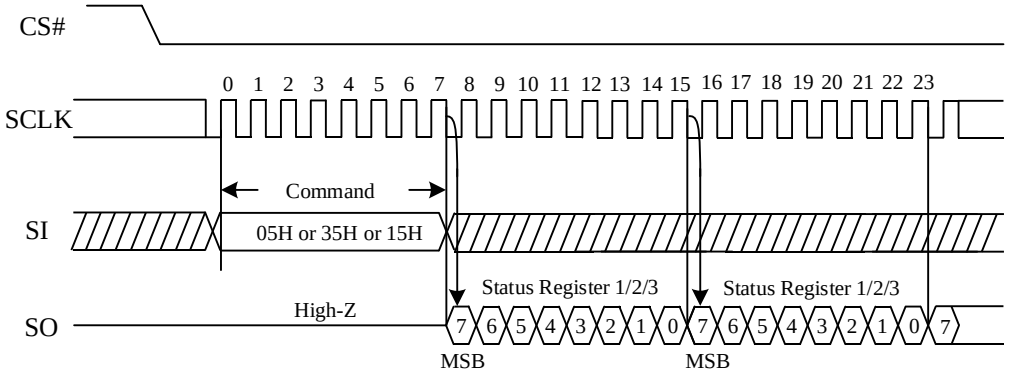
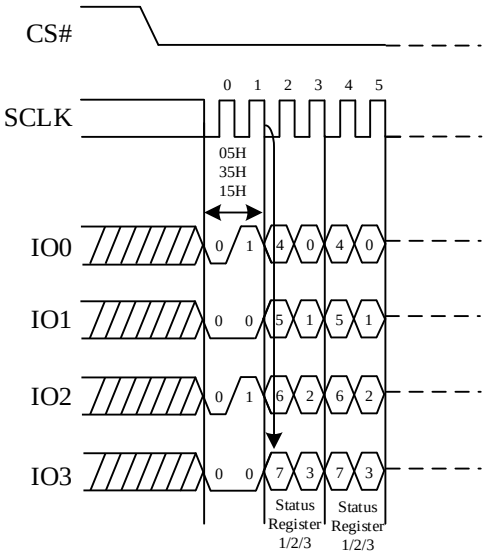


Figure 4. Read Status Register Sequence Diagram (QPI)



7.3.2. Write Status Register (01H or 31H or 11H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on the volatile bits of the Status Register. CS# must be driven high after the eighth or sixteenth bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is tW) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in the section of DATA PROTECTION The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered. For command code “01H”, the SI will input Status Register bits S7~S0, S15~S8. For the command code “31H”, the SI will input Status Register bits S15~S8. For the command code “11H”, the SI will input Status Register bits S23~S16.

Figure 5. Write Status Register Sequence Diagram

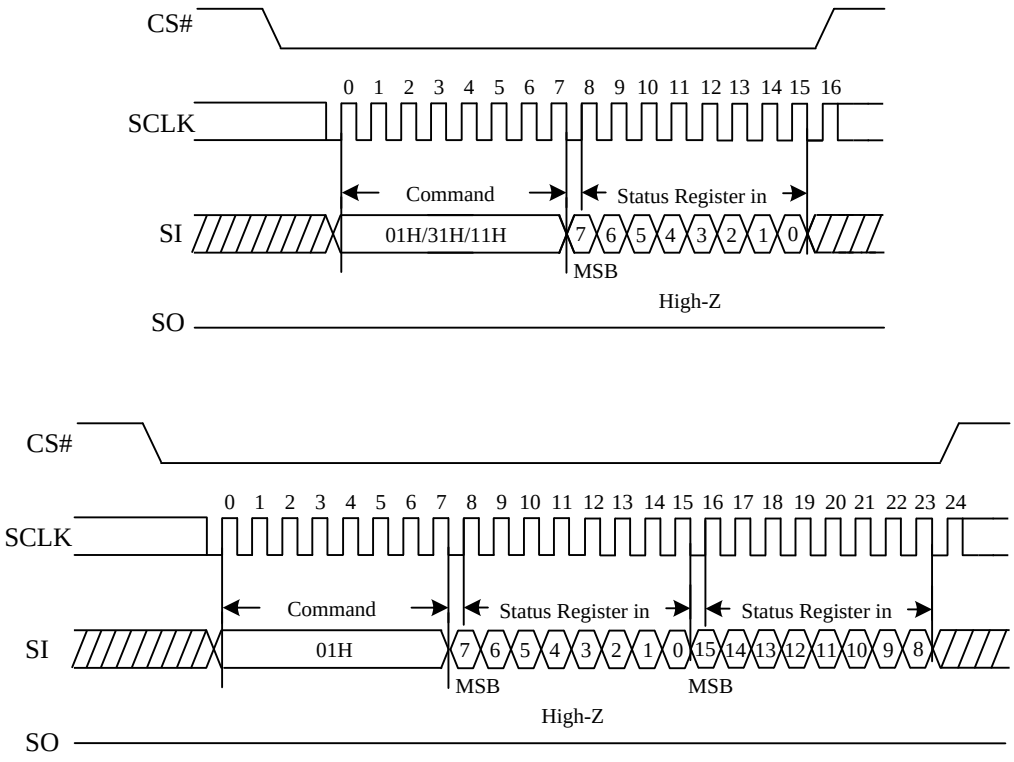
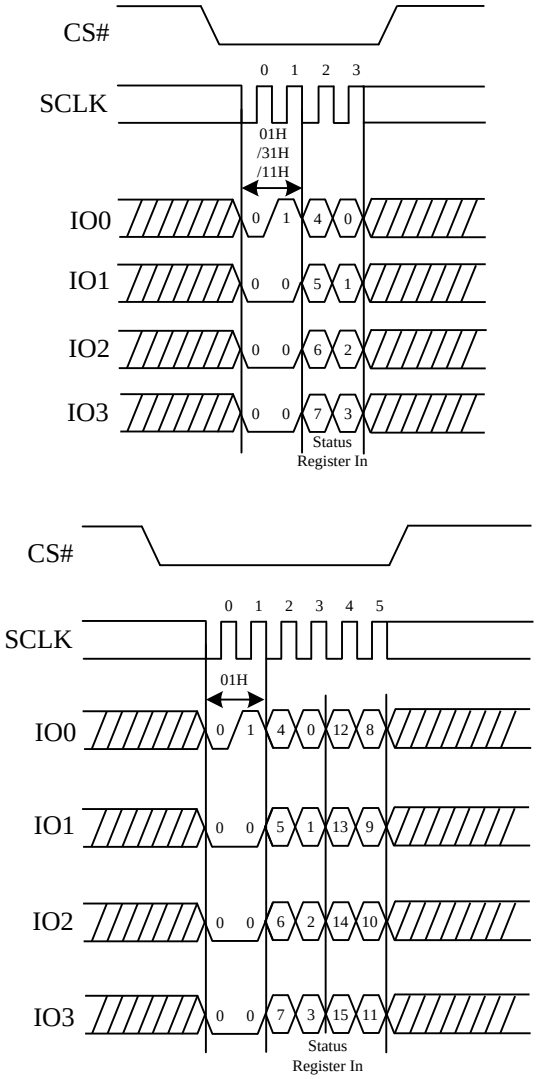


Figure 6. Write Status Register Sequence Diagram (QPI)



7.3.3. Read Extended Address Register (C8H)

The Read Extended Address Register instruction is entered by driving CS# low and shifting the instruction code "C8H" into the SI pin on the rising edge of SCLK. The Extended Address Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first.

When the device is in the 4-Byte Address Mode, the value of Address bits in Extended Address Register <EA2-EA0> is ignored.

Figure 7. Read Extended Address Register Diagram

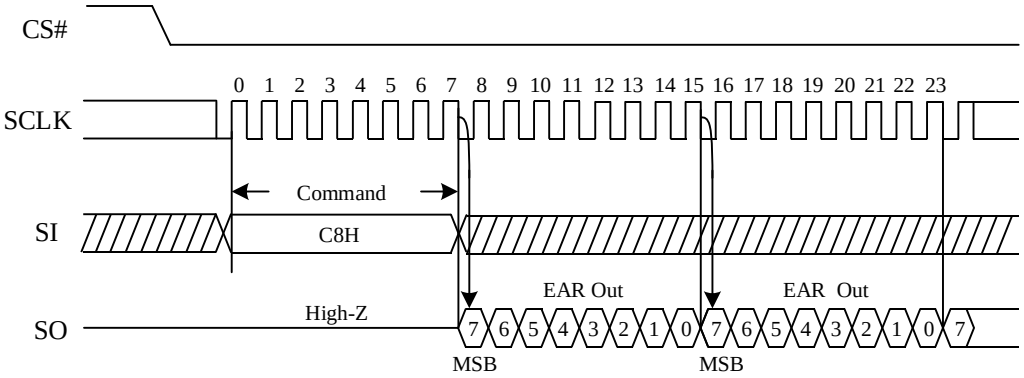
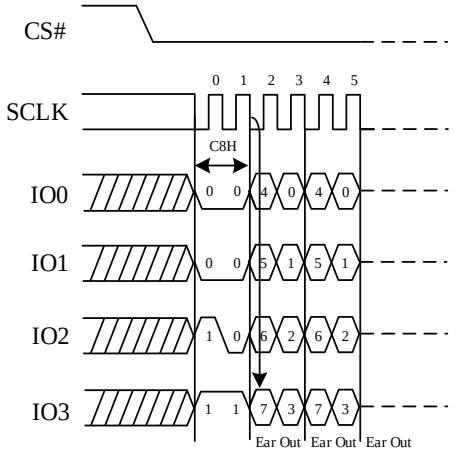


Figure 8. Read Extended Address Register Diagram (QPI)



7.3.4. Write Extended Address Register (C5H)

The Extended Address Register is a volatile register that stores the 4th byte address (A31-A24) when the device is operating in the 3-Byte Address Mode (ADS=0) with register bits <EA2-EA0>. To write the Extended Address Register, a Write Enable (06H) instruction must previously have been executed for the device to accept the Write Extended Address Register instruction (WEAR). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code "C5H", and then writing the Extended Address Register data byte.

Upon power up or the execution of a Software/Hardware Reset, the Extended Address Register bit values will be cleared to 0.

The Extended Address bits <EA2-EA0> is only effective when the device is in the 3-Byte Address Mode. If the device powers up with ADP bit set to 1, or an "Enter 4-Byte Address Mode (B7H)" instruction is issued, the device will require 4-Byte address input for all address related instructions, and the Extended Address Bits setting will be ignored. It is recommended to check and update the Extended Address Register if necessary when the device is switched from 4-Byte to 3-Byte Address Mode.

Figure 9. Write Extended Address Register Diagram

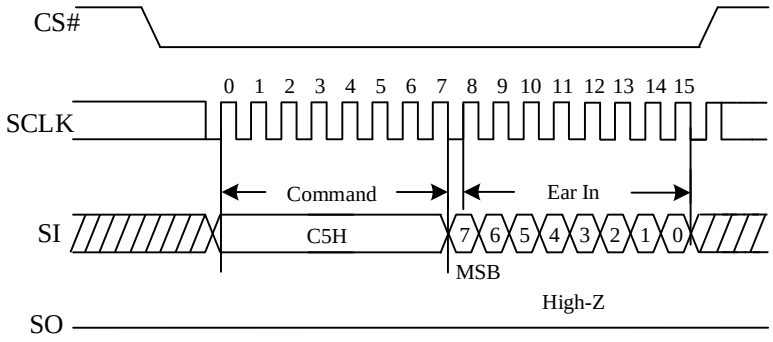
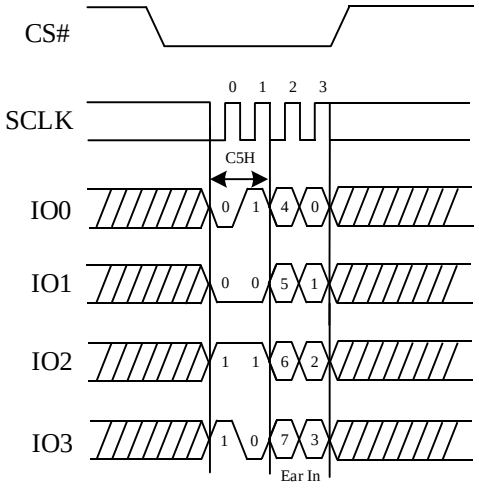


Figure 10. Write Extended Address Register Diagram (QPI)



7.3.5. Read Configuration Register (B5H)

The Read Configuration Register instruction is entered by driving CS# low and shifting the instruction code "B5H" into the SI pin on the rising edge of SCLK. The Configuration Register bits are then shifted out on the SO pin at the falling edge of SCLK with most significant bit (MSB) first. Read Configuration Register command, while an Erase, Program or Write Register cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 11. Read Configuration Register Diagram

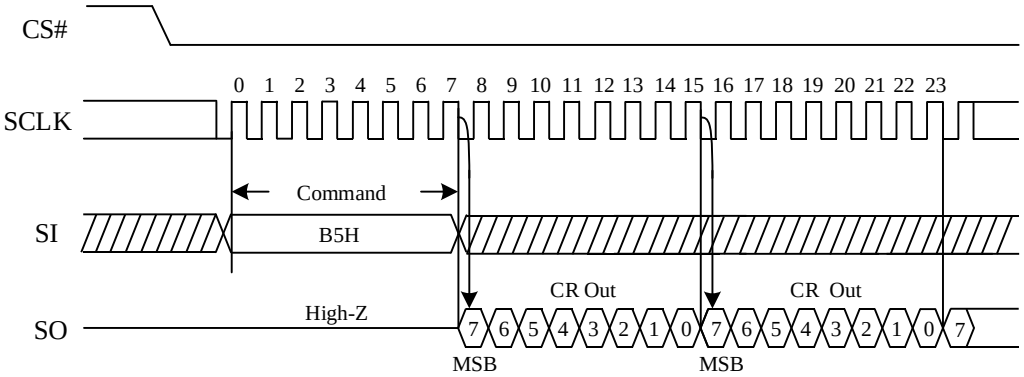
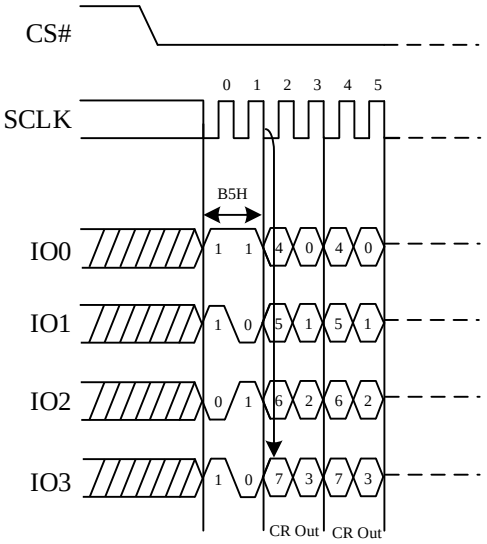


Figure 12. Read Configuration Register Diagram (QPI)



7.3.6. Write Configuration Register (B1H)

The Write Configuration Register (WCR) command allows new values to be written to the Configuration Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL). Once write enabled, the instruction is entered by driving CS# low, sending the instruction code "B1H", and then writing the Configuration Register data byte.

CS# must be driven high after the data Byte has been latched in. If not, the Write Configuration Register (WCR) command is not executed. As soon as CS# is driven high, the self-timed Write Configuration Register cycle (whose duration is tW for B1H) is initiated. The Write In Progress (WIP) bit is 1 during the self-timed Write Configuration Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

Figure 13. Write Configuration Register Diagram

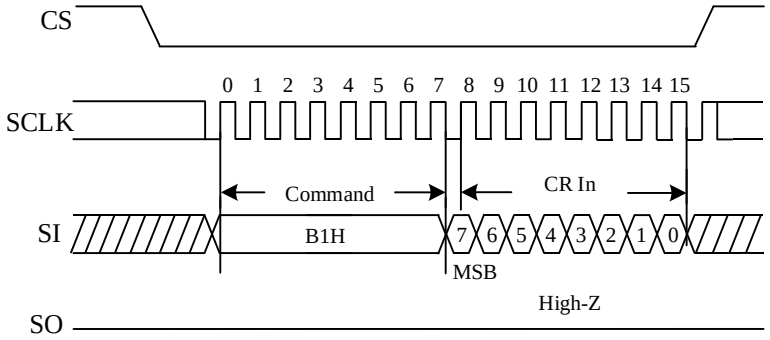
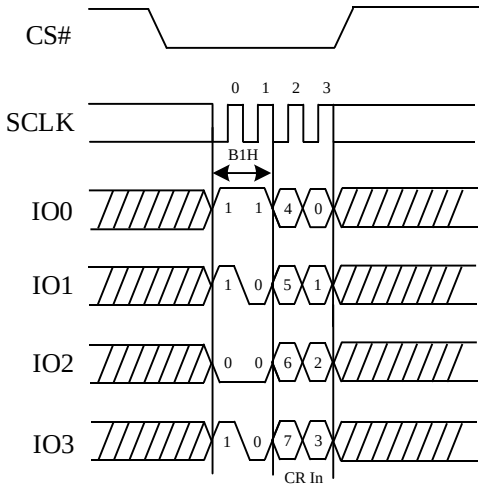


Figure 14. Write Configuration Register Diagram (QPI)



7.3.7. Read Manufacture ID/Device ID (90H)

The command is initiated by driving the CS# pin low and shifting the command code "90H" followed by a 24-bit address (A23-A0) of 000000H. After which, the Manufacturer ID and the Device ID are shifted out on the falling edge of SCLK with most significant bit (MSB) first is shown in the figure below. If the 24-bit address is initially set to 000001H, the Device ID will be read first.

Figure 15. Read Manufacture ID/ Device ID Sequence Diagram

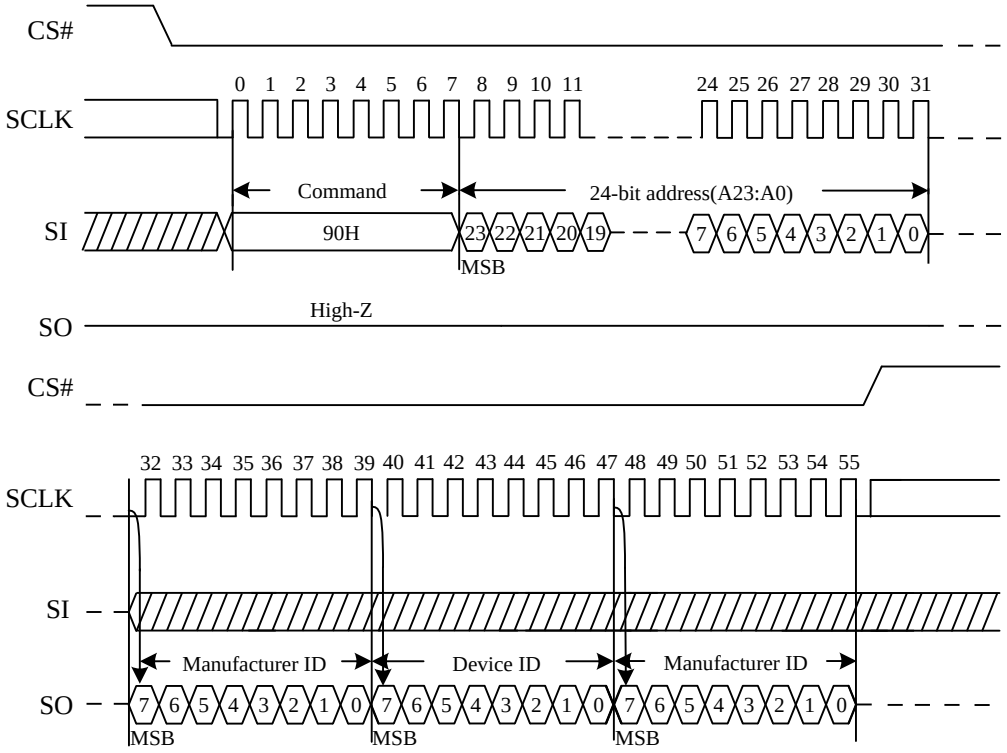
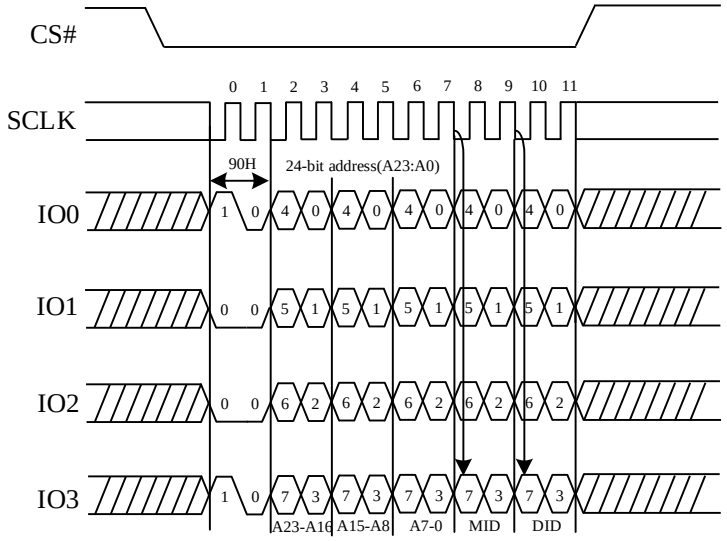


Figure 16. Read Manufacture ID/ Device ID Sequence Diagram (QPI)

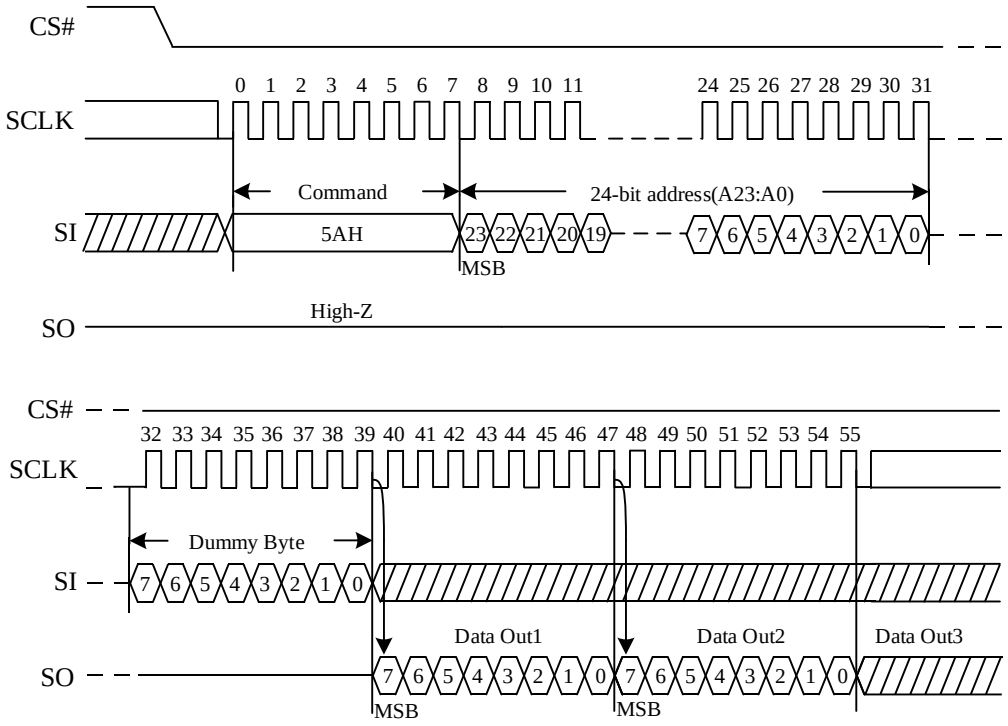


7.3.8. Read SFDP (5AH)

The Serial Flash Discoverable Parameter (SFDP) standard provides a consistent method of describing the functional and feature capabilities of serial flash devices in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features from multiple vendors. The concept is similar to the one found in the Introduction of JEDEC Standard, JESD68 on CFI. SFDP is a standard of JEDEC Standard No.216.

Note: For SFDP Table, please contact XTX.

Figure 17. Read Serial Flash Discoverable Parameter command Sequence Diagram



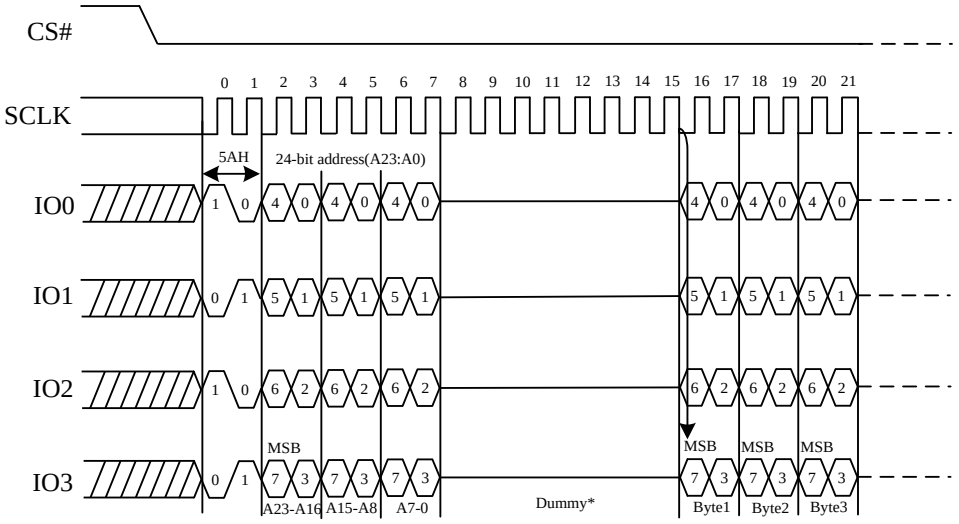
Note:

1. A23-A8 = 0, A7-A0 is the starting byte address for 256-byte SFDP Register.

Read Serial Flash Discoverable Parameter (5AH) in QPI mode

The Read Serial Flash Discoverable Parameter command is also supported in QPI mode. See the following figure. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter bits P[5:4] setting, the number of dummy clocks can be configured as either 8/6/12/16.

Figure 18. Read Serial Flash Discoverable Parameter command Sequence Diagram (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy clocks

Note:

1. A23-A8 = 0, A7-A0 is the starting byte address for 256-byte SFDP Register.

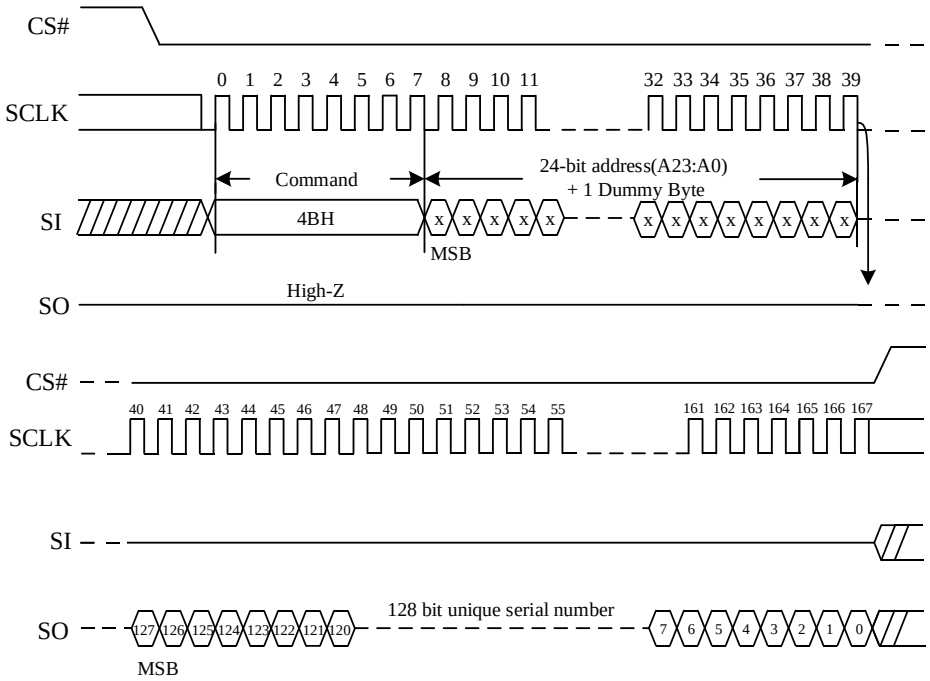
7.3.9. Read Unique ID (4BH)

The Read Unique ID command accesses a factory-set read-only 128bit number that is unique to each device. The Unique ID can be used in conjunction with user software methods to help prevent copying or cloning of a system.

The Read Unique ID command sequence: CS# goes low → Sending Read Unique ID command → 24-bit address (A23:A0) (Don't care) + 1 dummy Byte → 128bit Unique ID Out → CS# goes high.

The command sequence is shown below.

Figure 19. Read Unique ID (RUID) Sequence

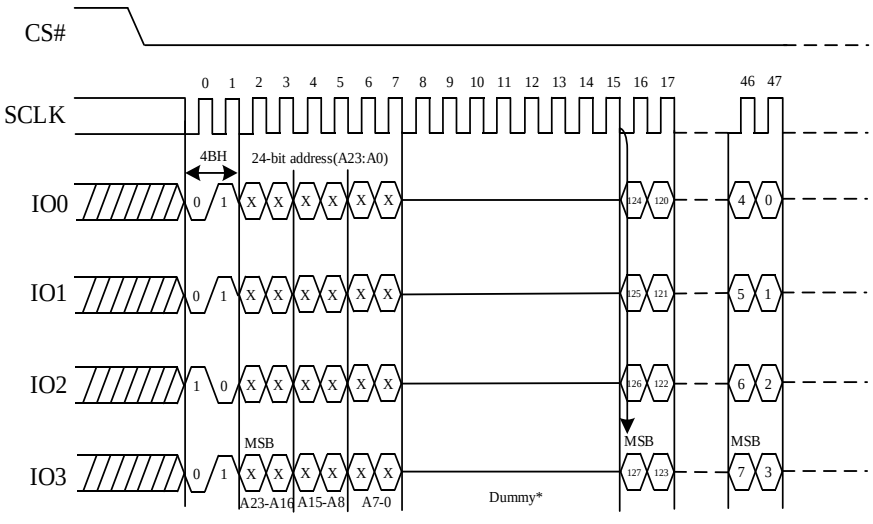


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Read Unique ID (4BH) in QPI mode

The Read Unique ID command is also supported in QPI mode. See the figure below, In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter bits P[5:4] setting, the number of dummy clocks can be configured as either 8/6/12/16.

Figure 20. Read Unique ID (RUID) Sequence (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy clocks

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.3.10. Read Identification (9EH/9FH)

The Read Identification (RDID) command allows the 8-bit manufacturer identification to be read, followed by two bytes of device identification. The device identification indicates the memory type in the first byte, and the memory capacity of the device in the second byte. Any Read Identification (RDID) command while an Erase or Program cycle is in progress will not be decoded, and has no effect on the cycle that is in progress. The Read Identification (RDID) command should not be issued while the device is in Deep Power-Down Mode.

The device is first selected by driving CS# to low. Then, the 8-bit command code for the command is shifted in. This is followed by the 24-bit manufacture identification and device identification, stored in the memory, being shifted out on Serial Data Output, each bit being shifted out during the falling edge of Serial Clock. The command sequence is shown in the figure below. The Read Identification (RDID) command is terminated by driving CS# to high at any time during data output. When CS# is driven high, the device is put in the Standby Mode. Once in the Standby Mode, the device waits to be selected, so that it can receive, decode and execute commands.

Figure 21. Read Identification ID Sequence Diagram

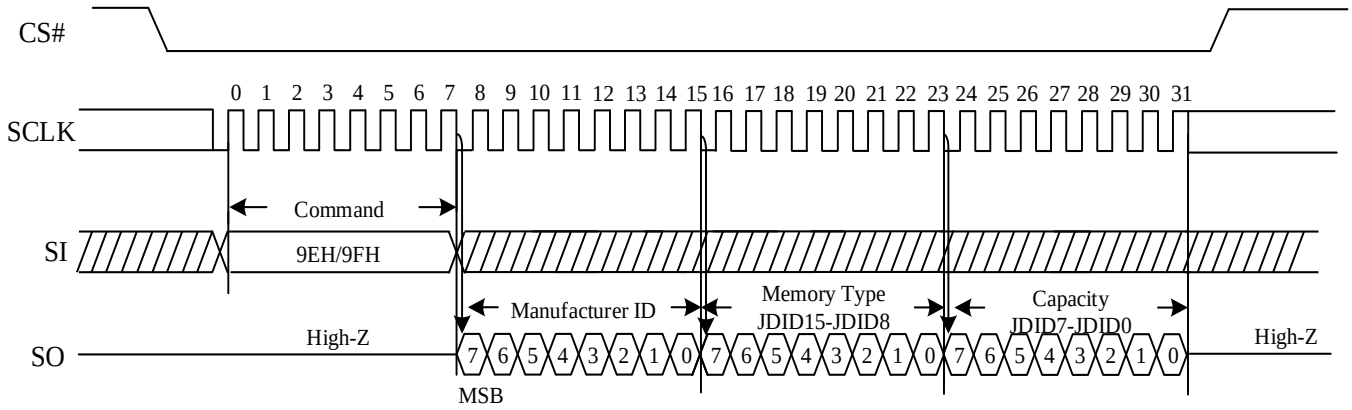
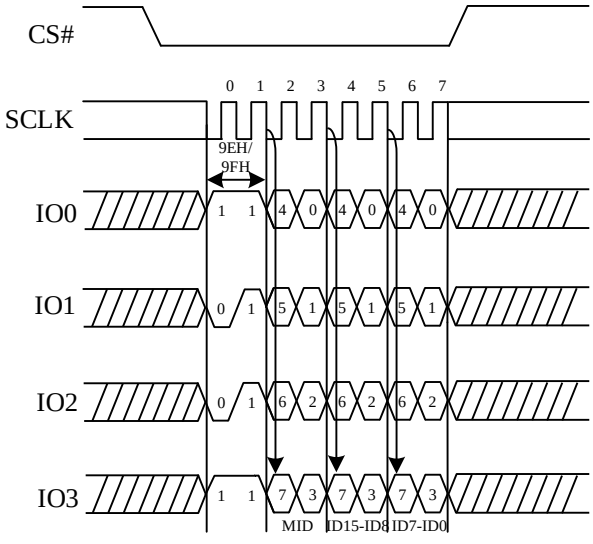


Figure 22. Read Identification ID Sequence Diagram (QPI)



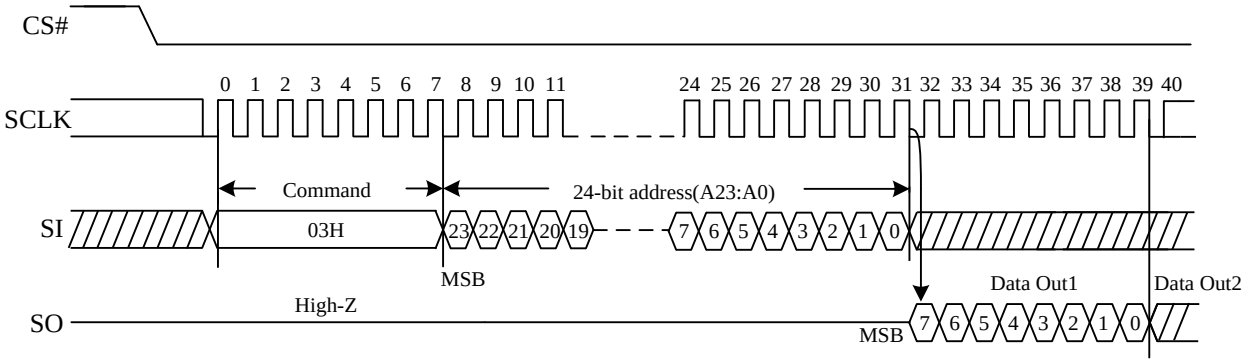
7.4. Array Access

7.4.1. Normal Read (03H/13H)

The Read Data Bytes (READ, 03H) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fR, during the falling edge of SCLK. The first byte address can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

The “13H” instruction is similar to “03H” instruction except the address length becomes 32-bit.

Figure 23. Read Data Bytes Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

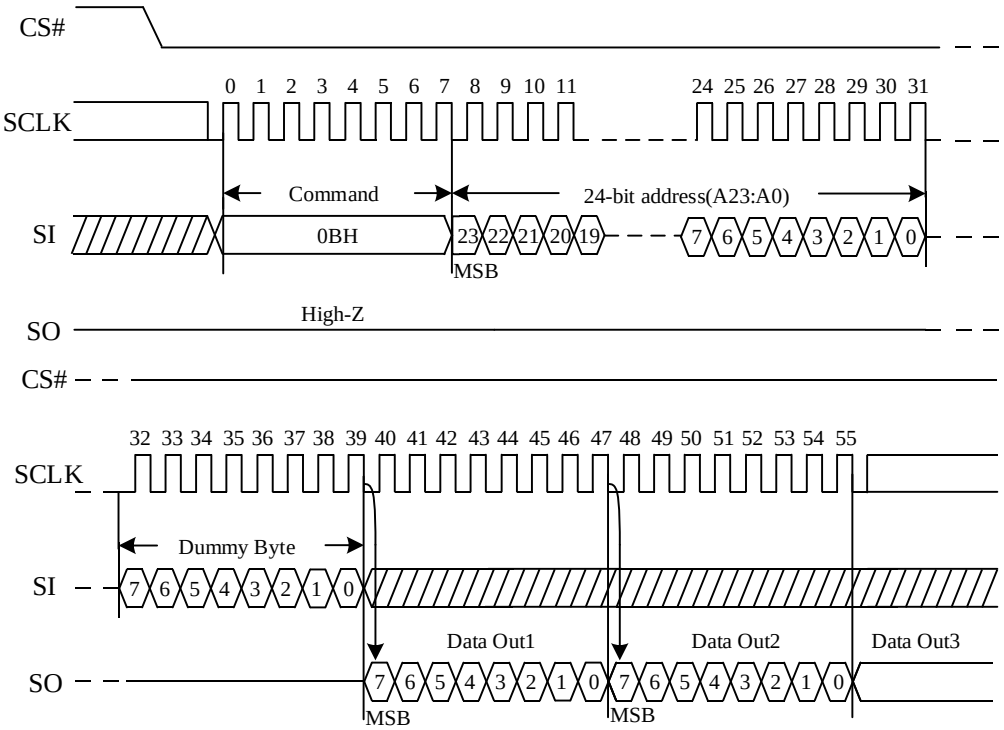
7.4.2. Fast Read (0BH/0CH)

The Read Data Bytes at Higher Speed (Fast Read, 0BH) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte address can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

The number of Dummy clocks for “Fast Read (0BH)” is 8.

The “0CH” instruction is similar to “0BH” instruction except the address length becomes 32-bit.

Figure 24. Read Data By test Higher Speed Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

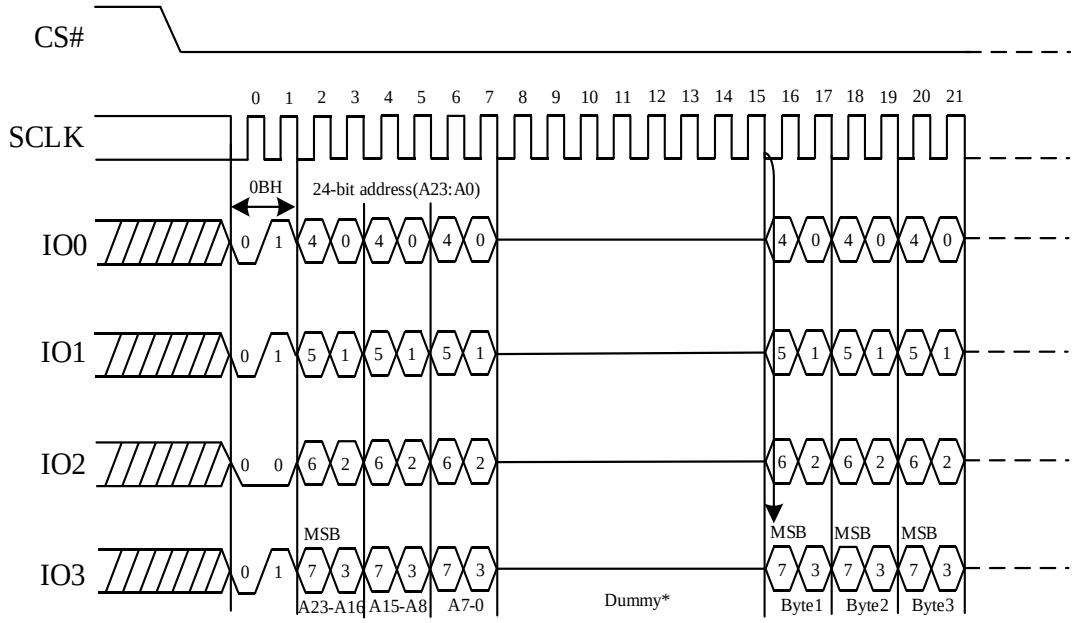
Fast Read (0BH/0CH) in QPI mode

The Fast Read (0BH) command is also supported in QPI mode. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency.

Depending on the Read Parameter bits P5-P4 setting, the number of dummy clocks can be configured as either 8/6/12/16.

The "Wrap Around" feature is not available in QPI mode for Fast Read instruction.

Figure 25. Read Data Bytes at Higher Speed Sequence Diagram (QPI)



*Set Read Parameters Command (C0H) can set the number of dummy clocks

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

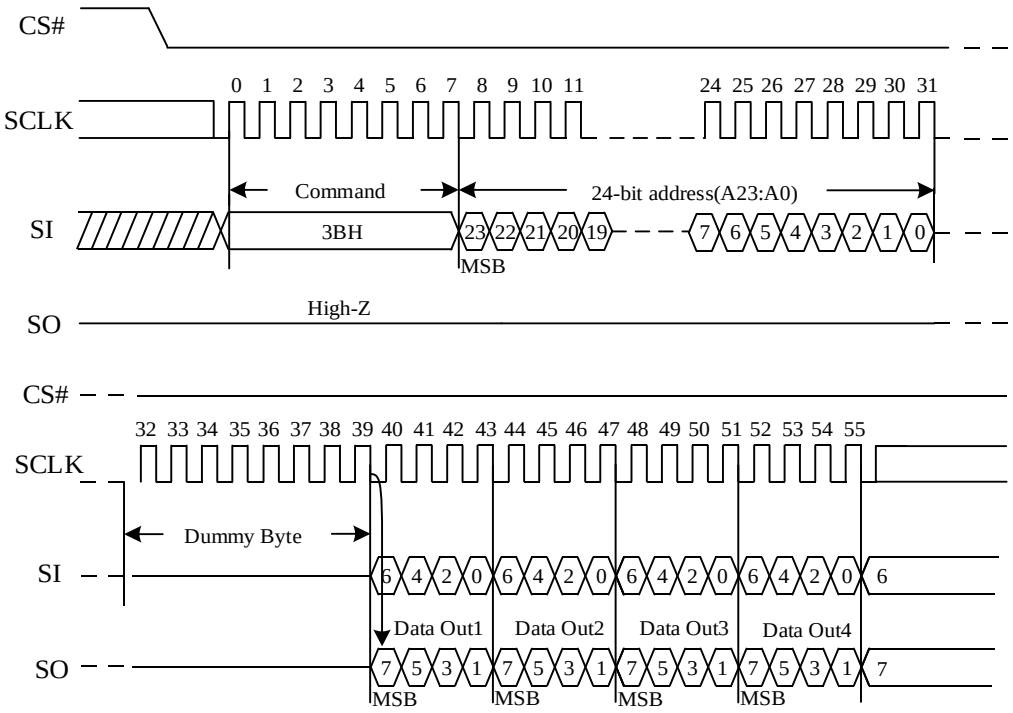
7.4.3. Dual Output Fast Read (3BH/3CH)

The Dual Output Fast Read (3BH) command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the following figure. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

The number of Dummy clocks for “Dual Output Fast Read (3BH)” is 8.

The “3CH” instruction is similar to “3BH” instruction except the address length becomes 32-bit.

Figure 26. Dual Output Fast Read Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

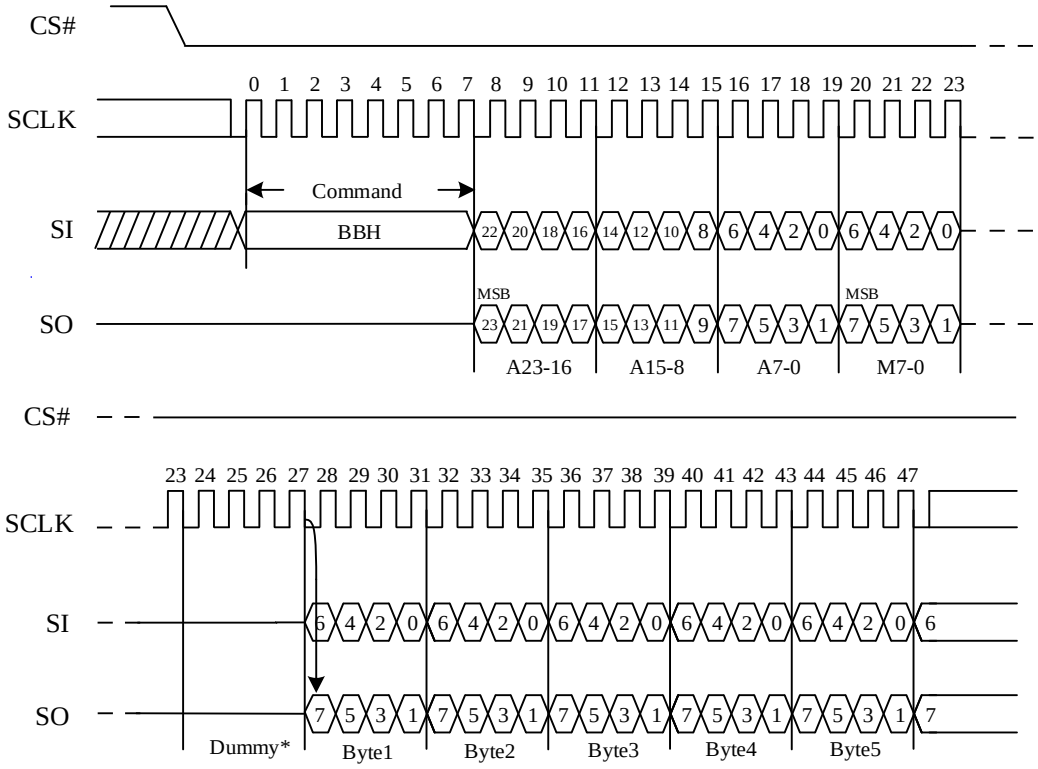
7.4.4. Dual I/O Fast Read (BBH/BCH)

The Dual I/O Fast Read (BBH) command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in the following figure. The first byte address can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out.

The number of dummy clocks for "Dual I/O Fast Read" (BBH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8(Include M7-0). When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6(Include M7-0). When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12(Include M7-0). When the LC (LC1, LC0) bits are set to (1,1), the dummy clock cycles is 16(Include M7-0).

The "BCH" instruction is similar to "BBH" instruction except the address length becomes 32-bit.

Figure 27. Dual I/O Fast Read Sequence Diagram (M5-4≠(1,0))



* The number of dummy clocks can be set by LC bit

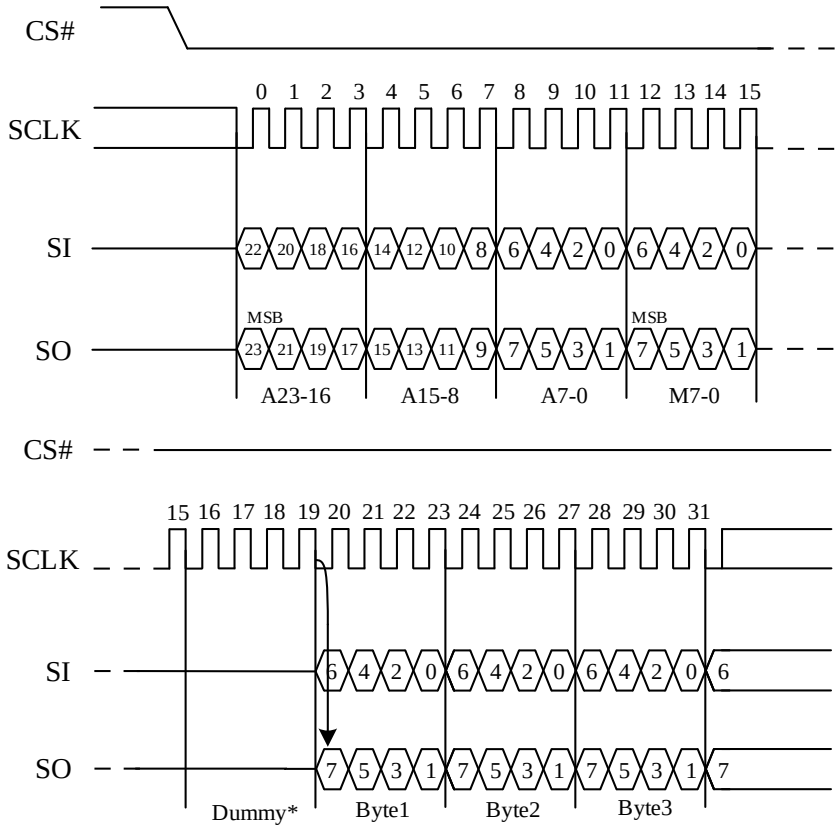
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Dual I/O Fast Read with "Continuous Read Mode"

The Dual I/O Fast Read (BBH) command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in the figure below. If the "Continuous Read Mode" bits (M5-4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

The number of dummy clocks for "Dual I/O Fast Read" (BBH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8(Include M7-0). When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6(Include M7-0). When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12(Include M7-0). When the LC (LC1, LC0) bits are set to (1,1), the dummy clock cycles is 16(Include M7-0).

Figure 28. Dual I/O Fast Read Sequence Diagram (M5-4=(1,0))



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

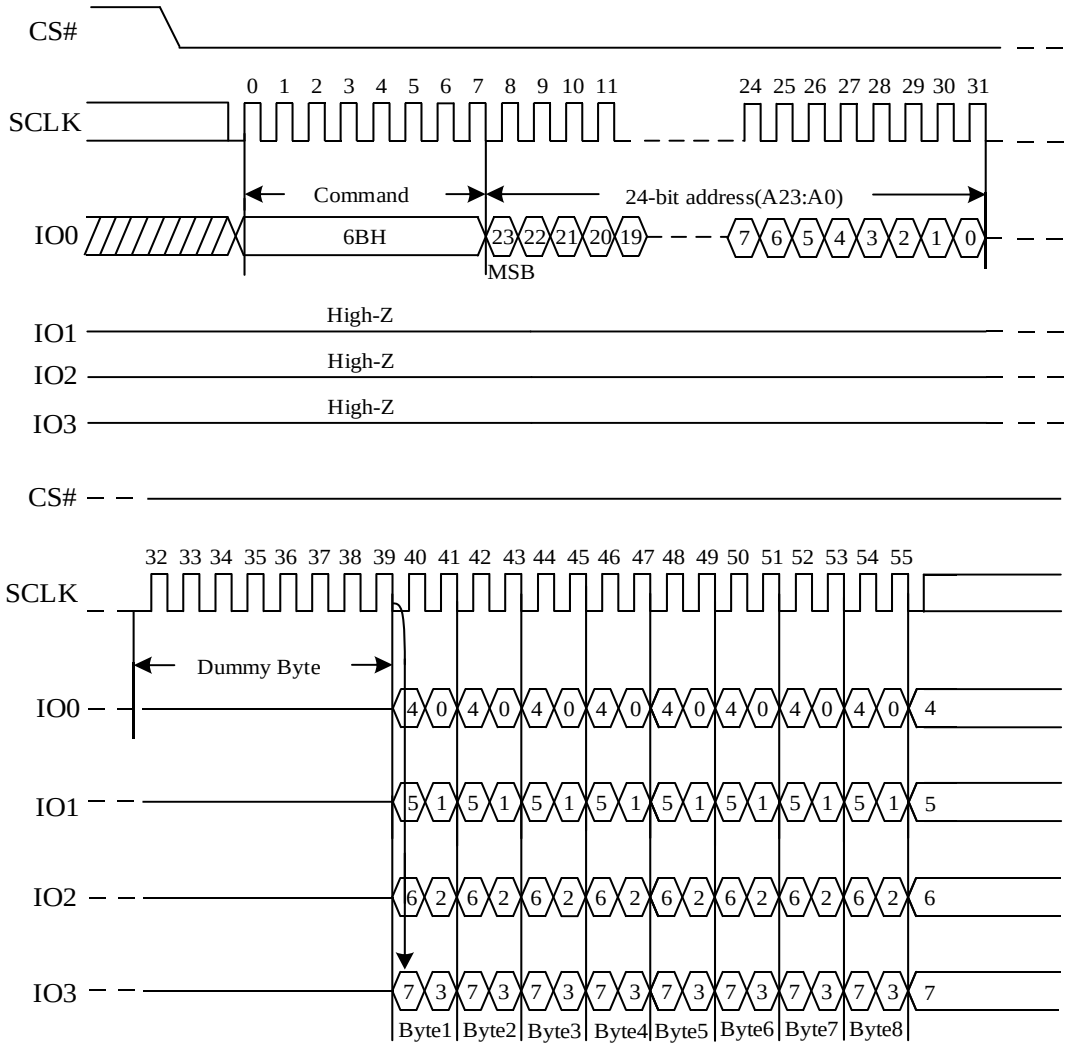
7.4.5. Quad Output Fast Read (6BH/6CH)

The Quad Output Fast Read (6BH) command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in the figure below. The first byte address can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

The number of Dummy clocks for "Quad Output Fast Read (6BH)" is 8.

The "6CH" instruction is similar to "6BH" instruction except the address length becomes 32-bit.

Figure 29. Quad Output Fast Read Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

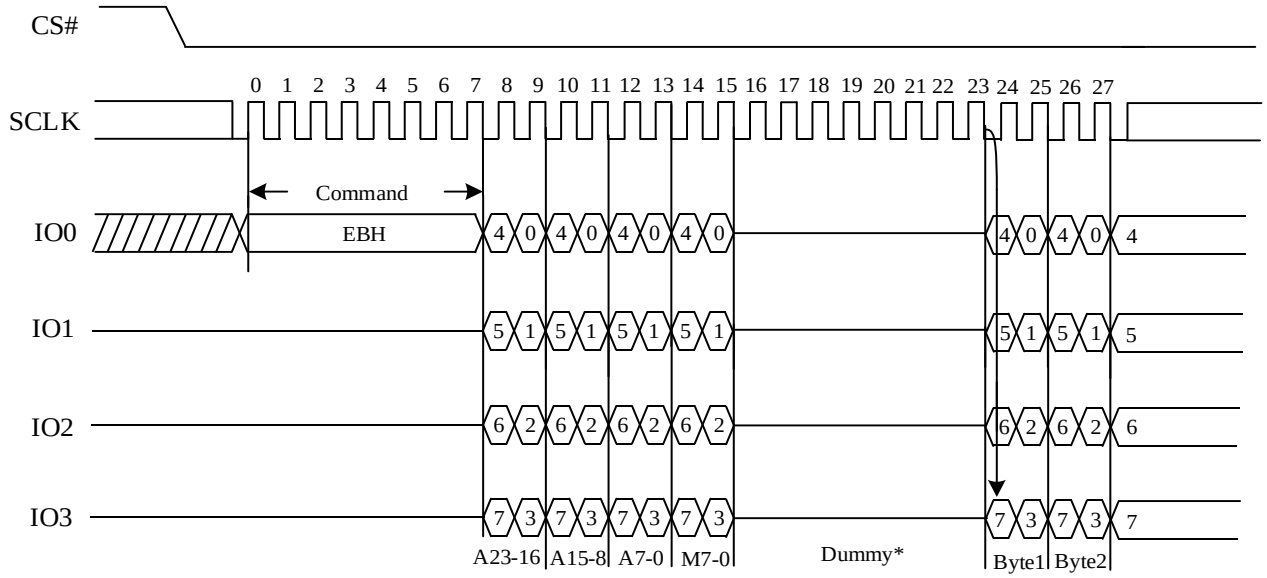
7.4.6. Quad I/O Fast Read (EBH/ECH)

The Quad I/O Fast Read (EBH) command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a "Continuous Read Mode" byte and 4 dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in the figure below. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command.

The number of dummy clocks for "Quad I/O Fast Read" (EBH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8(Include M7-0). When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6(Include M7-0). When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12(Include M7-0). When the LC (LC1, LC0) bits are set to (1,1), the dummy clock cycles is 16(Include M7-0).

The "ECH" instruction is similar to "EBH" instruction except the address length becomes 32-bit.

Figure 30. Quad I/O Fast Read Sequence Diagram (M5-4≠(1,0))



* The number of dummy clocks can be set by LC bit

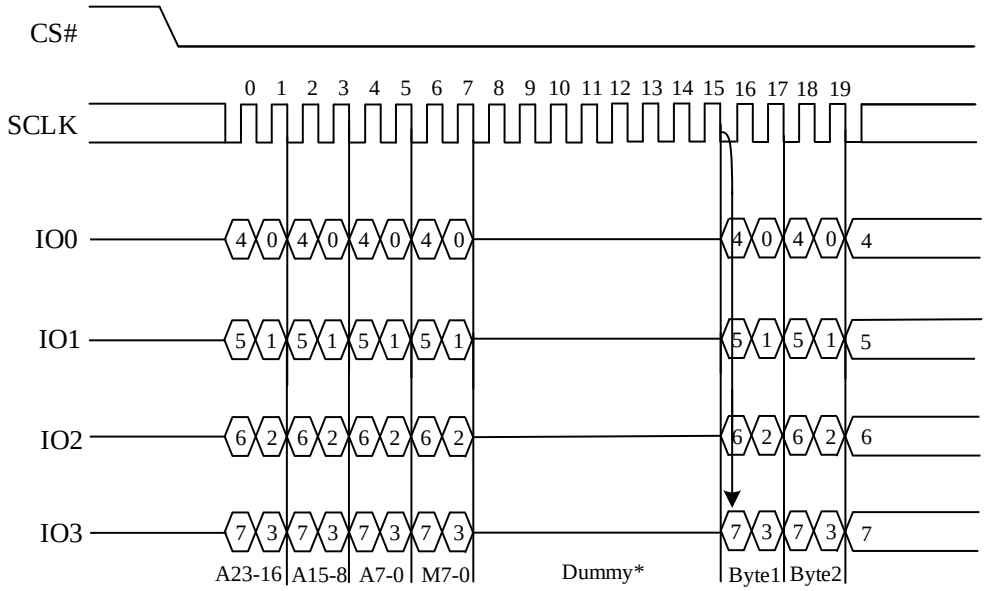
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Quad I/O Fast Read with "Continuous Read Mode"

The Quad I/O Fast Read command (EBH) can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in the figure below. If the "Continuous Read Mode" (M5-4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M5-4) before issuing normal command.

The number of dummy clocks for "Quad I/O Fast Read" (EBH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8(Include M7-0). When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6(Include M7-0). When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12(Include M7-0). When the LC (LC1, LC0) bits are set to (1,1), the dummy clock cycles is 16(Include M7-0).

Figure 31. Quad I/O Fast Read Sequence Diagram (M5-4=(1,0))



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Quad I/O Fast Read with "16/32/64-Byte Wrap Around" in Standard SPI mode

The Quad I/O Fast Read command (EBH) can be used to access a specific portion within a page by issuing "Set Burst With Wrap" (77H) Command" prior to EBH. The Set Burst With Wrap" (77H) Command can either enable or disable the "Wrap Around" feature for the following EBH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command, once it reaches the ending boundary of the 16/32/64-byte section, the output will wrap around the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (16/32/64-byte) of data without issuing multiple read commands.

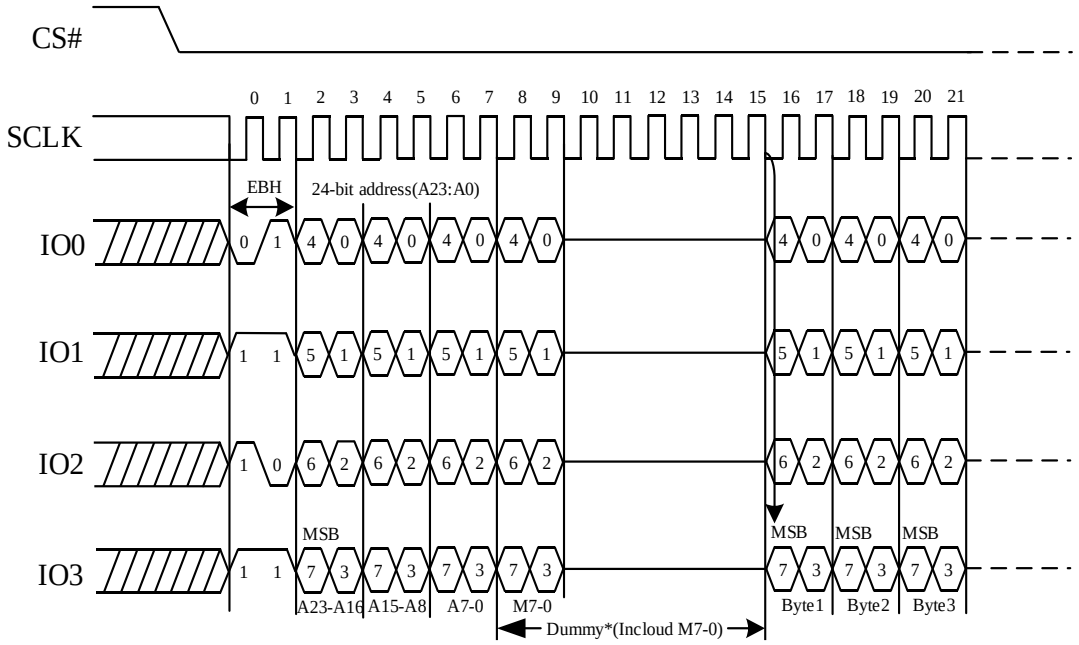
Quad I/O Fast Read (EBH) in QPI mode

The Quad I/O Fast Read command (EBH) is also supported in QPI mode. See the figure below. In QPI mode, the “Wrap Length” and the number of dummy clocks is configured by the “Set Read Parameters (C0H)” command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency.

Depending on the Read Parameter bits P[5:4] setting, the number of dummy clocks can be configured as either 8/6/12/16.

In QPI mode, the “Continuous Read Mode” bits M7-M0 are also considered as dummy clocks. “Continuous Read Mode” feature is also available in QPI mode for Quad I/O Fast Read command.

Figure 32. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0) QPI)



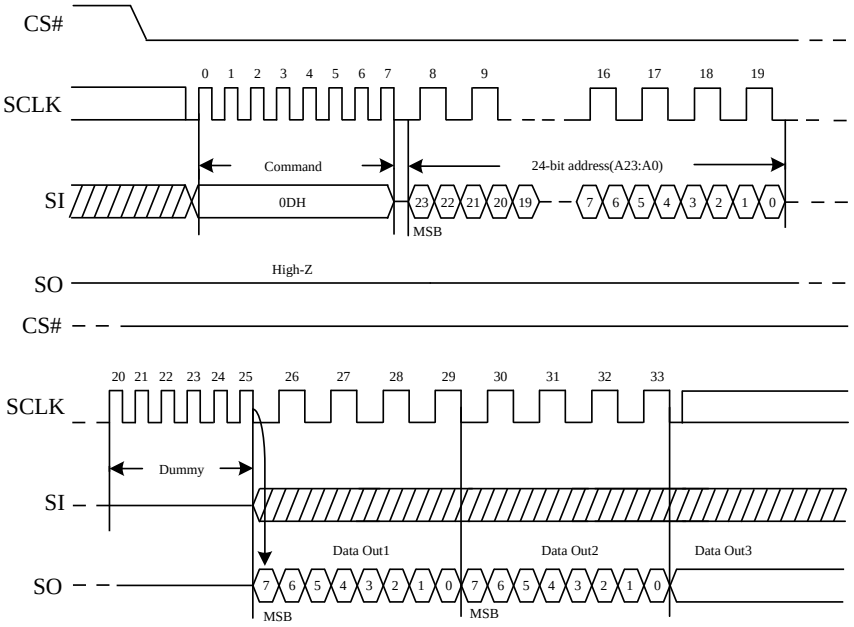
*Set Read Parameters Command (C0H) can set the number of Dummy clocks

7.4.7. DTR Fast Read (0DH)

The DTR Fast Read command (0DH) is similar to the Fast Read instruction except that the 24-bit address input and the data output require DTR (Double Transfer Rate) operation. This is accomplished by adding six dummy clocks after a 3-byte address (A23-A0) or a 4-byte address (A31-A0) as shown in the figure below. The dummy clocks allow the devices internal circuits additional time for setting up the initial address. During the dummy clocks the data value on the SO pin is a "don't care".

The number of Dummy clocks for "DTR Fast Read" (0DH) is 6.

Figure 33. DTR Fast Read Instruction

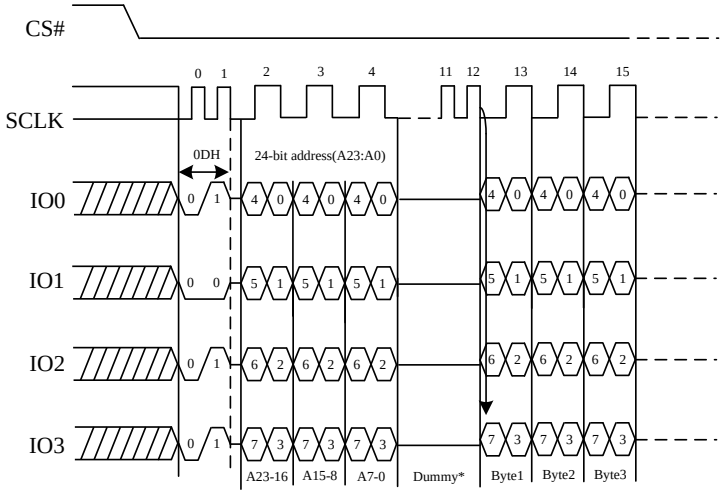


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

DTR Fast Read (0DH) in QPI Mode

The DTR Fast Read instruction is also supported in QPI mode. The number of dummy clocks for "DTR Fast Read" (0DH) under QPI mode and "DTR Fast Read Quad IO" (EDH/EEH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8. When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6. When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12.

Figure 34. DTR Fast Read Instruction (QPI)



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.8. DTR Fast Read Dual I/O(BDH)

The DTR Fast Read Dual I/O (BDH) instruction allows for improved random access while maintaining two IO pins, IO0 and IO1. It is similar to the Dual I/O Fast Read (BBH) instruction but with the capability to input a 3-byte address (A23-A0) or a 4-byte address (A31-A0) four bits per clock. This reduced instruction overhead may allow for code execu-tion (XIP) directly from the Dual SPI in some applications.

The number of dummy clocks for "DTR Fast Read Dual IO" (BDH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8(Include M7-0). When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6(Include M7-0). When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12(Include M7-0) (Include M7-0).

DTR Fast Read Dual I/O with "Continuous Read Mode"

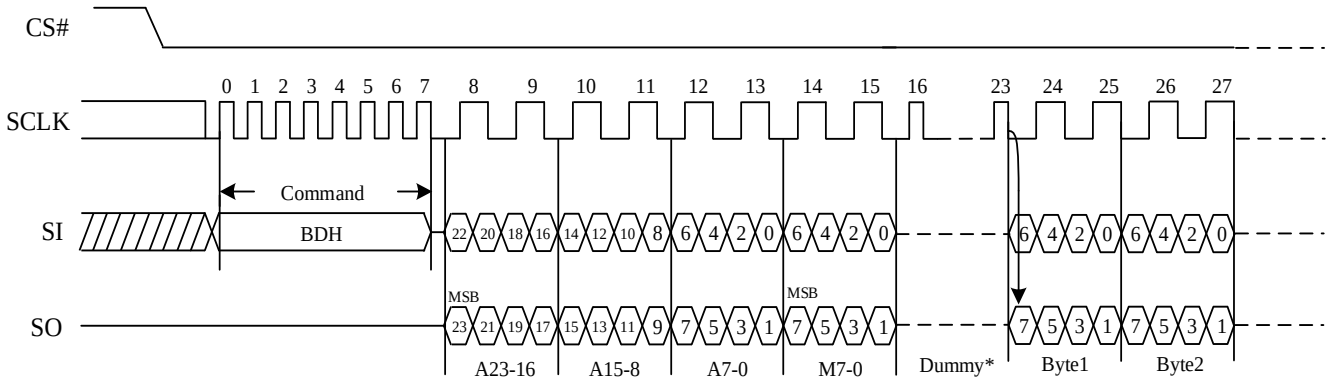
The DTR Fast Read Dual I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after a 3-byte address (A23-A0) or a 4-byte address (A31-A0), as shown in "BDH" command description. The upper nibble of the (M7-4) controls the length of the next DTR Fast Read Dual I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are "don't care" ("x"). However, the IO pins should be high-impedance for 4 dummy clocks prior to the falling edge of the first data out clock.

The number of Dummy clocks for "DTR Fast Read Dual I/O" (BDH) under continuous read mode is 6 (Include M7-0).

If the "Continuous Read Mode" bits (M5-4) = (1, 0), then the next DTR Fast Read Dual I/O instruction (after CS# is raised and then lowered) does not require the BDH instruction code, as shown in the figure below. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFFFH/FFFFFH on IO0 for the next instruc-tion (16/20 clocks), to ensure M4 = 1 and return the device to normal operation.

The number of dummy clocks for "DTR Fast Read Dual IO" (BDH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8(Include M7-0). When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6(Include M7-0). When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12(Include M7-0) (Include M7-0).

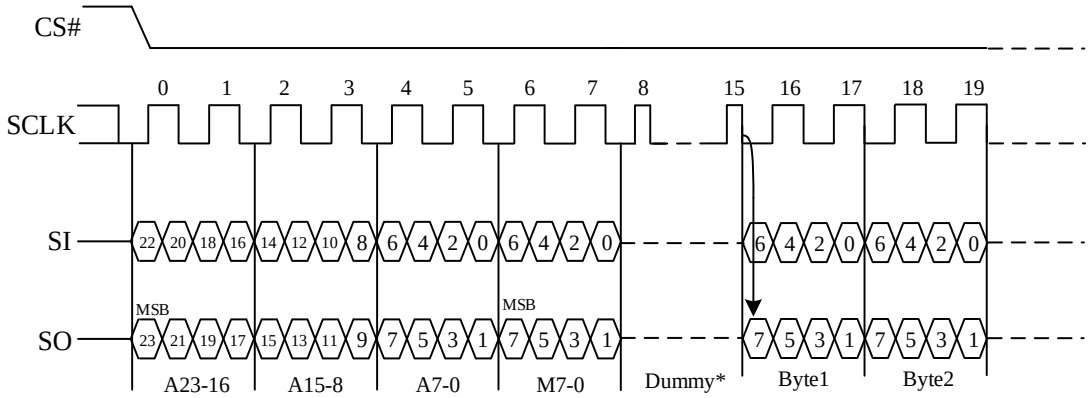
Figure 35. DTR Fast Read Dual I/O(Initial instruction or previous M5-4≠10, SPI Mode only)



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 36. DTR Fast Read Dual I/O (Previous instruction set M5-4=10, SPI Mode only)



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.9. DTR Fast Read Quad I/O (EDH/EEH)

The DTR Fast Read Quad I/O (EDH) instruction is similar to the Quad I/O Fast Read (EBH) instruction except that address and data bits are input and output twice for each clock through four pins IO0, IO1, IO2 and IO3 and several Dummy clocks are required in SPI mode prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code execution (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register must be set to enable the DTR Fast Read Quad I/O Instruction.

The number of dummy clocks for "DTR Fast Read Quad IO" (EDH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8. When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6. When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12.

The "EEH" instruction is similar to "EDH" instruction except the address length becomes 32-bit.

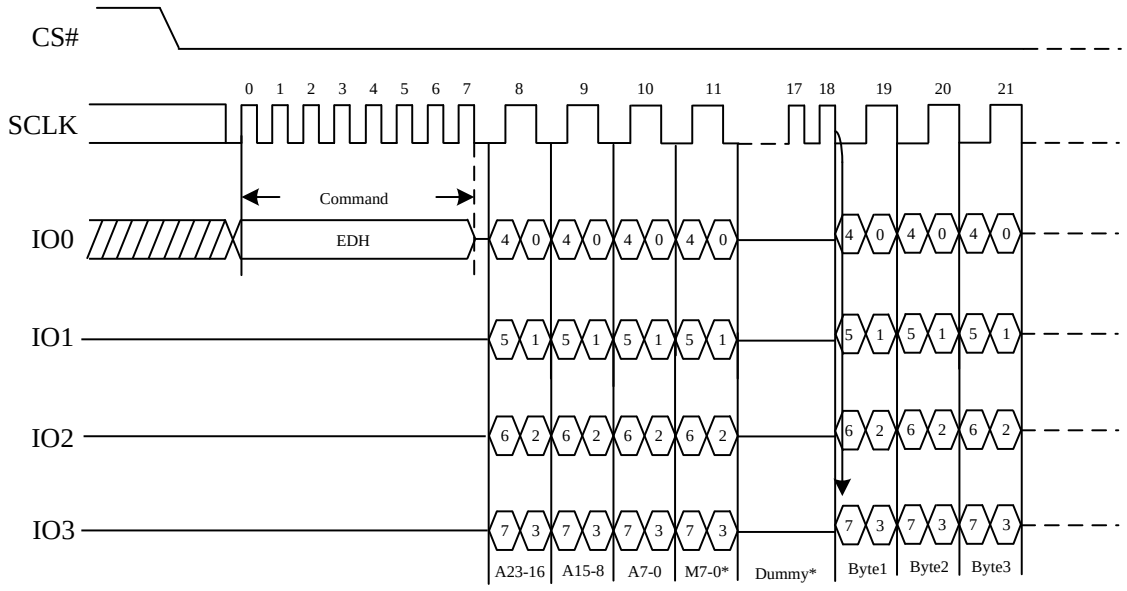
DTR Fast Read Quad I/O with "Continuous Read Mode"

The DTR Fast Read Quad I/O instruction can further reduce instruction overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address bits (A23-0), as shown in "EDH" command description. The upper nibble of the (M7-4) controls the length of the next DTR Fast Read Quad I/O instruction through the inclusion or exclusion of the first byte instruction code. The lower nibble bits of the (M3-0) are "don't care ("x")". However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

The number of dummy clocks for "DTR Fast Read Quad IO" (EDH) can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8. When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6. When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12.

If the "Continuous Read Mode" bits (M5-4) = (1,0), then the next DTR Fast Read Quad I/O instruction (after CS# is raised and then lowered) does not require the EDH instruction code. This reduces the instruction sequence by eight clocks and allows the Read address to be immediately entered after CS# is asserted low. If the "Continuous Read Mode" bits M5-4 do not equal to (1,0), the next instruction (after CS# is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. It is recommended to input FFH/3FFH on IO0 for the next instruction (8/10 clocks), to ensure M4 = 1 and return the device to normal operation.

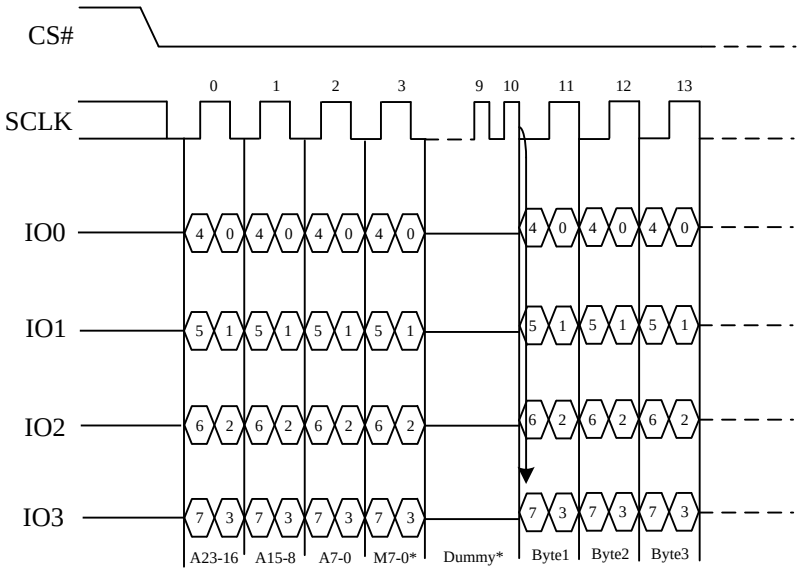
Figure 37. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, SPI Mode)



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 38. DTR Fast Read Quad I/O (Previous instruction set M5-4=10, SPI Mode)



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

DTR Fast Read Quad I/O with "16/32/64-Byte Wrap Around" in Standard SPI mode

The DTR Fast Read Quad I/O instruction can also be used to access a specific portion within a page by issuing a "Set Burst With Wrap" (77H) Command prior to EDH. The "Set Burst With Wrap" (77H) Command can either enable or disable the "Wrap Around" feature for the following EDH commands. When "Wrap Around" is enabled, the data being accessed can be limited to either an 16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the instruction, once it reaches the ending boundary of the 16/32/64-byte section, the output will wrap around to the beginning boundary automatically until CS# is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (16/32/64-byte) of data without issuing multiple read commands.

DTR Fast Read Quad I/O (EDH) in QPI Mode

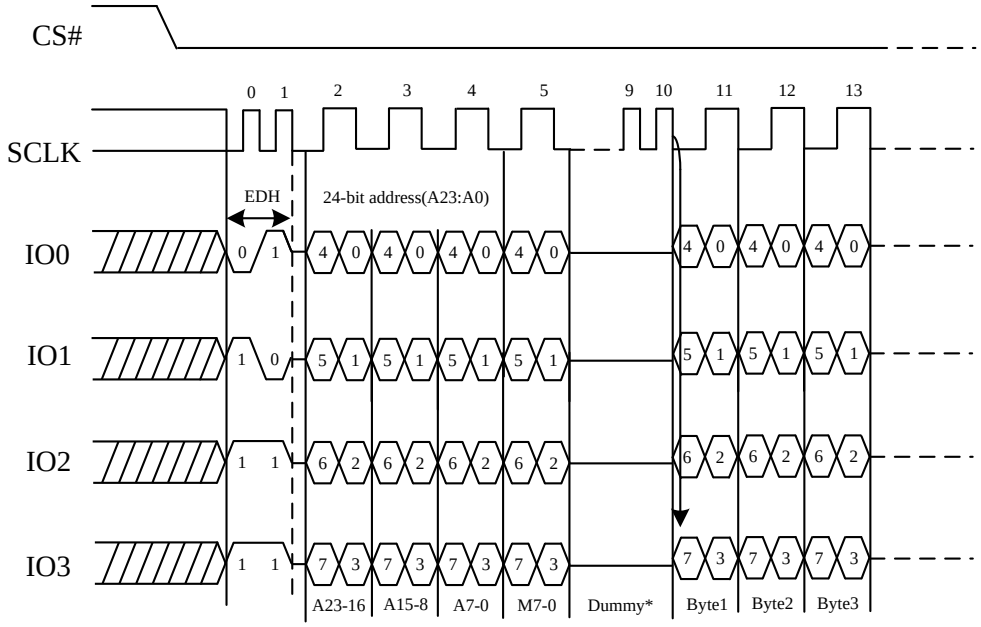
The DTR Fast Read Quad I/O instruction is also supported in QPI mode, as shown in the figure below. In QPI mode, the "Continuous Read Mode" bits M7-0 are also considered as dummy clocks.

The "Wrap Around" feature is also available in QPI mode for DTR Fast Read Quad I/O command. The "Wrap Length" can be configured by the "Set Read Parameters (C0H)" command. However, the number of dummy clocks is set by LC bit in status register and cannot be configured by the "Set Read Parameters (C0H)" command for DTR Fast Read Quad I/O instruction. Also EBH and ECH are alternative ways to perform "Wrap Around" under QPI mode.

"Continuous Read Mode" feature is also available in QPI mode for DTR Fast Read Quad I/O instruction. Please refer to the description on previous pages.

The number of dummy clocks for "DTR Fast Read Quad IO" (EDH) under QPI can be set by the Latency Code (LC) in status register. When the LC (LC1, LC0) bits are set to (0,0), which is default, the number of dummy clock cycles is 8. When the LC (LC1, LC0) bits are set to (0,1), the dummy clock cycles is 6. When the LC (LC1, LC0) bits are set to (1,0), the dummy clock cycles is 12.

Figure 39. DTR Fast Read Quad I/O (Initial instruction or previous M5-4≠10, QPI Mode)



* The number of dummy clocks can be set by LC bit

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.10. Page Program (02H/12H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

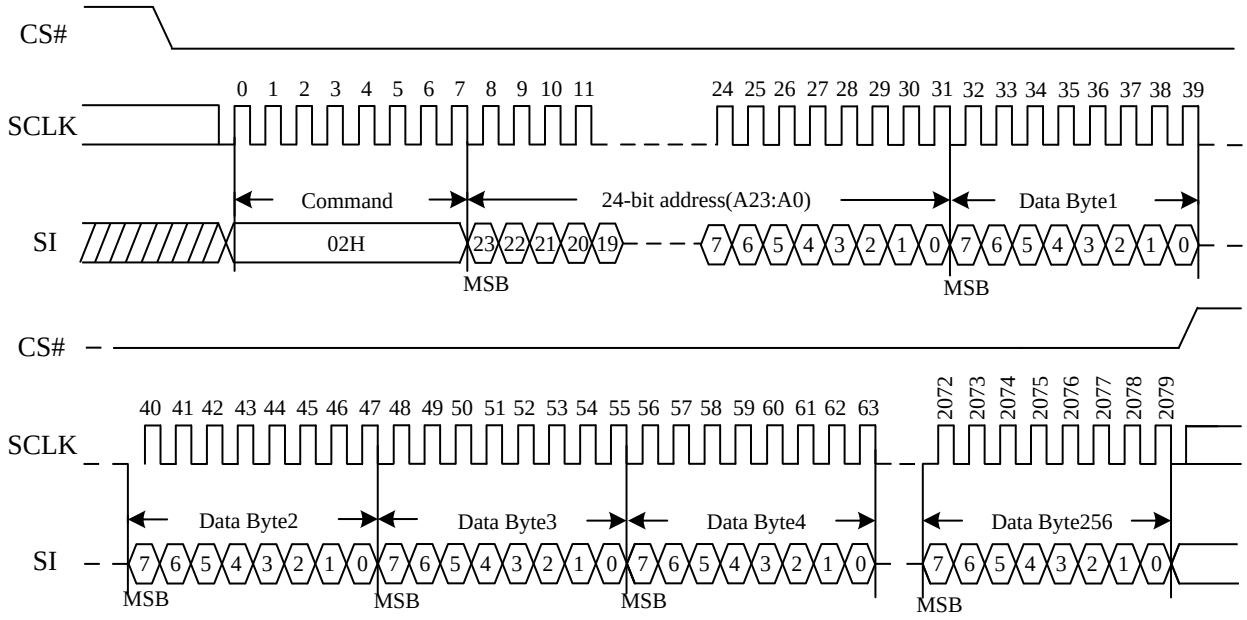
The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low → Sending Page Program command → 3-byte address on SI → at least 1 byte data on SI → CS# goes high. The command sequence is shown in the figure below. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is tPP) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Page Program (PP) command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) is not executed.

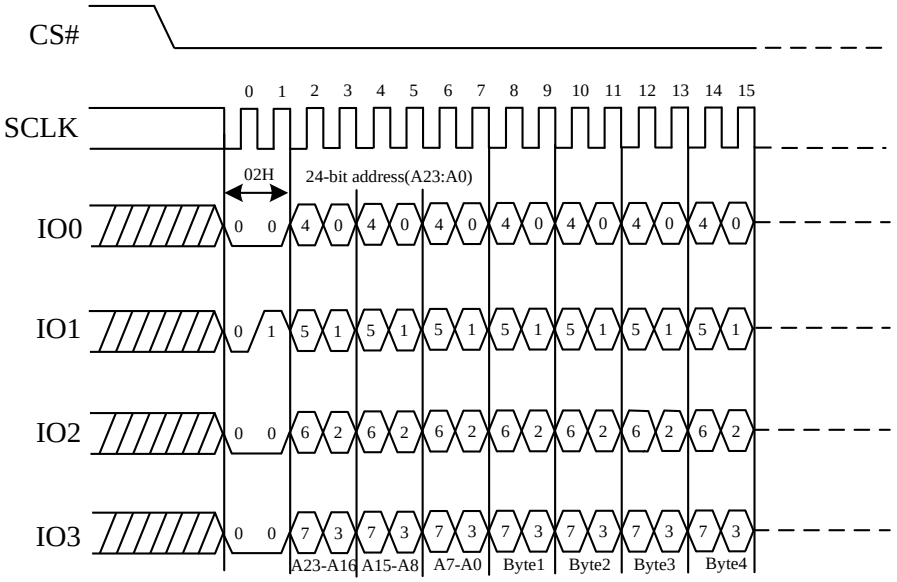
The "12H" instruction is similar to "02H" instruction except the address length becomes 32-bit.

Figure 40. Page Program Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 41. Page Program Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.11. Quad Page Program (32H/34H)

The Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. To use Quad Page Program, the Quad Enable bit in status register Bit9 must be set (QE=1). A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Quad Page Program command. The Quad Page Program command is entered by driving CS# Low, followed by the command code (32H), three address bytes and at least one data byte on IO pins.

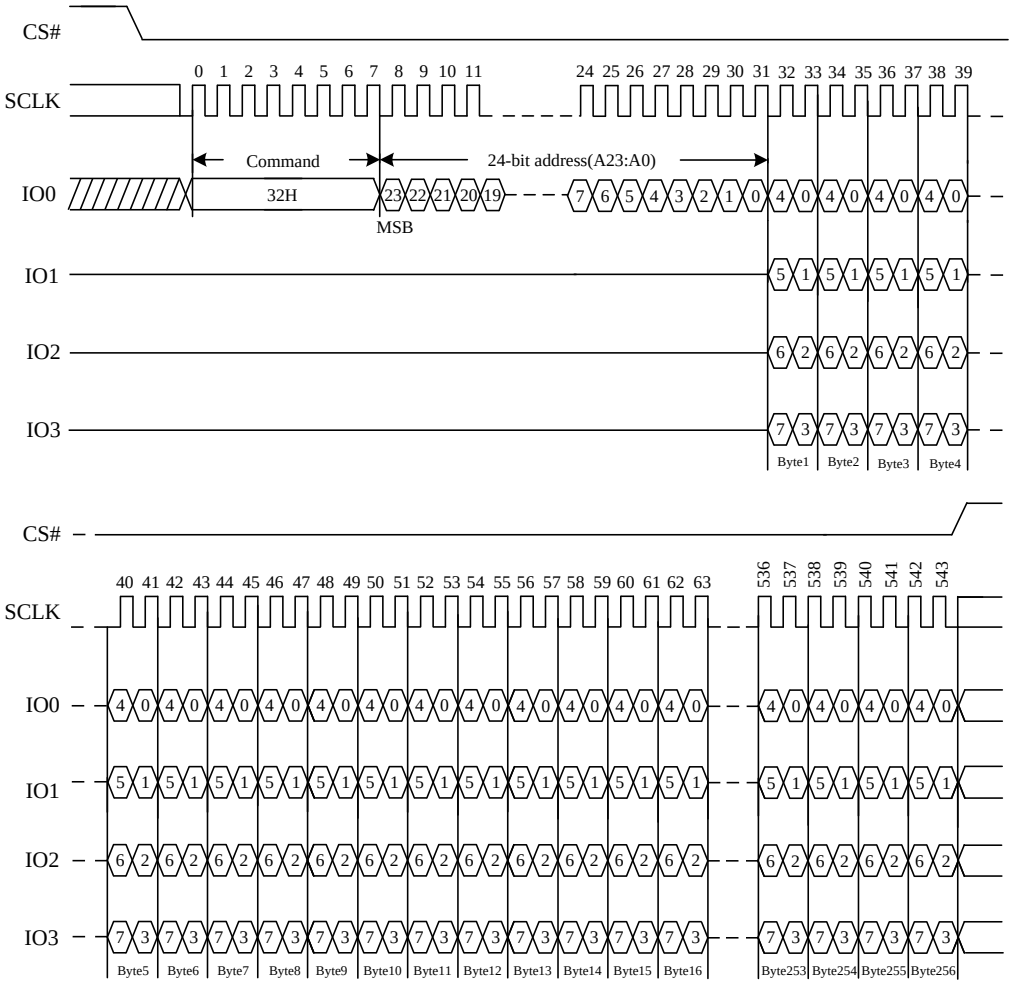
The command sequence is shown in the figure below. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Quad Page Program command will not be executed.

As soon as CS# is driven high, the self-timed Quad Page Program cycle (whose duration is tPP) is initiated. While the Quad Page Program cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

A Quad Page Program command applied to a page which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) will not be executed.

The “34H” instruction is similar to “32H” instruction except the address length becomes 32-bit.

Figure 42. Quad Page Program Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.12. Extend Quad Page Program (C2H/3EH)

The Extend Quad Page Program command is for programming the memory using four pins: IO0, IO1, IO2, and IO3. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command. The extend quad Page Program command is entered by driving CS# Low, followed by the command code (C2H), three or four address bytes and at least one data byte on IO pins.

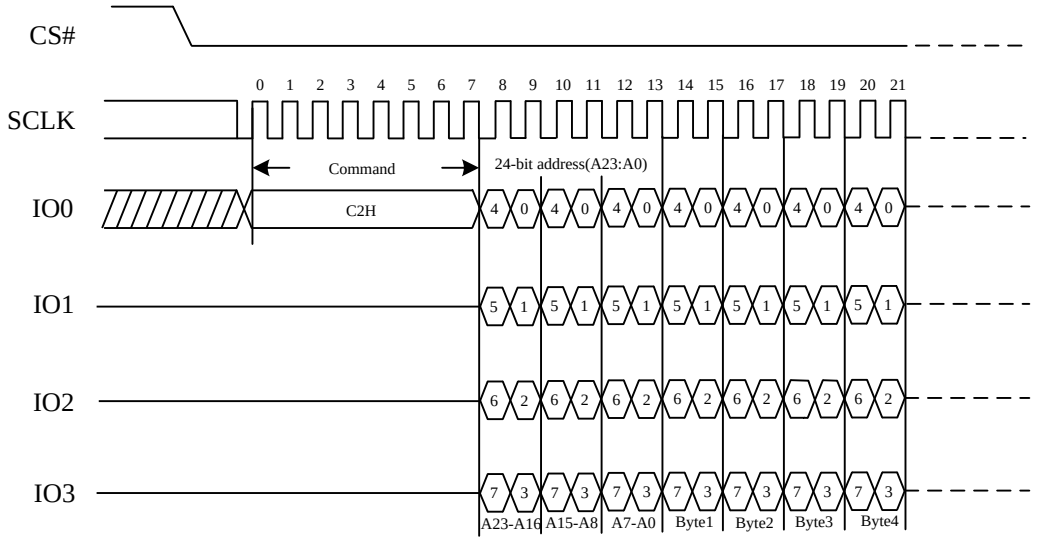
If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Extend Quad Page Program (EPP) command is not executed.

As soon as CS# is driven high, the self-timed Extend Quad Page Program cycle (whose duration is tPP) is initiated. While the Extend Quad Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write in Progress (WIP) bit is 1 during the self-timed Extend Quad Page Program cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

An Extend Quad Page Program command applied to a page which is protected by the Block Protect (T/B, BP3, BP2, BP1, and BP0) is not executed.

The “3EH” instruction is similar to “C2H” instruction except the address length becomes 32-bit.

Figure 43. Quad Page Program Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.13. Sector Erase (20H/21H)

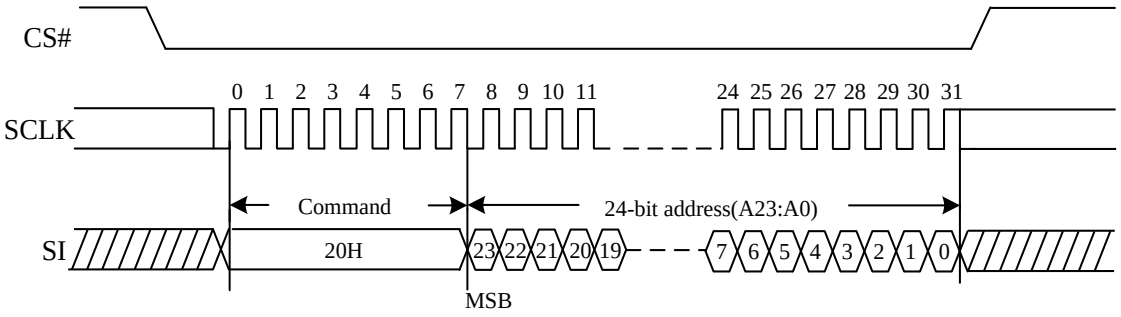
The Sector Erase (SE) command is for erasing all the data of the chosen sector. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Sector Erase command. The Sector Erase (SE) command is entered by driving CS# low, followed by the command code, and 3-address byte on SI. Any address inside the sector is a valid address for the Sector Erase (SE) command.

The Sector Erase command sequence: CS# goes low → Sending Sector Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the Sector Erase (SE) command will not be executed. As soon as CS# is driven high, the self-timed Sector Erase cycle (whose duration is tSE) is initiated. While the Sector Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Sector Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A Sector Erase (SE) command applied to a sector which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bit will not be executed.

The "21H" instruction is similar to "20H" instruction except the address length becomes 32-bit.

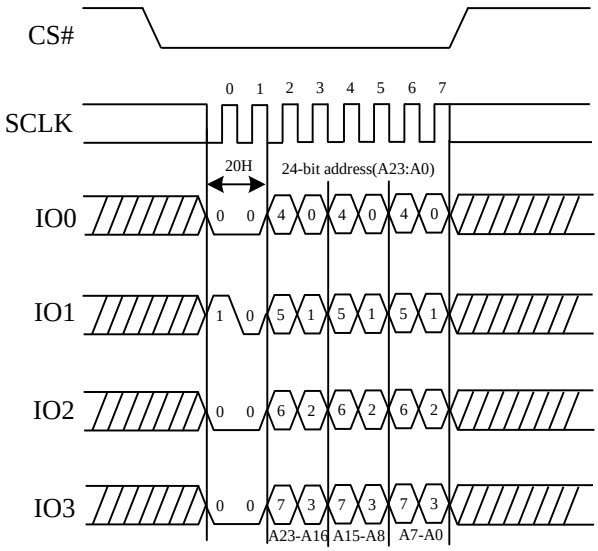
Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 44. Sector Erase Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 45. Sector Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.14. 32KB Block Erase (52H/5CH)

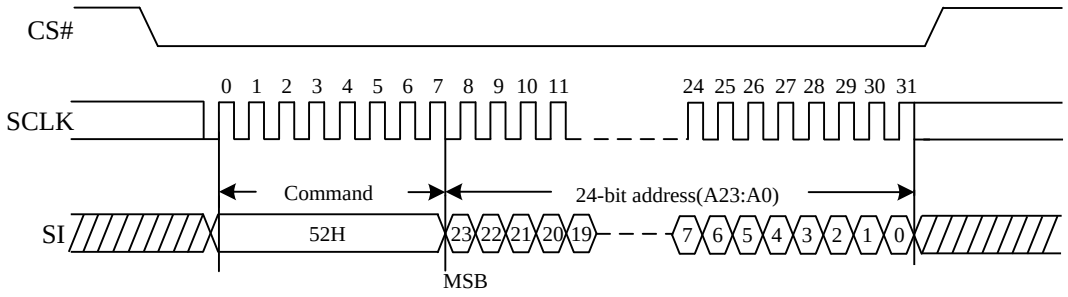
The 32KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the 32KB Block Erase command. The 32KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high. Any address inside the block is a valid address for the 32KB Block Erase (BE) command.

The 32KB Block Erase command sequence: CS# goes low → Sending 32KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 32KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE1) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 32KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits will not be executed.

The "5CH" instruction is similar to "52H" instruction except the address length becomes 32-bit.

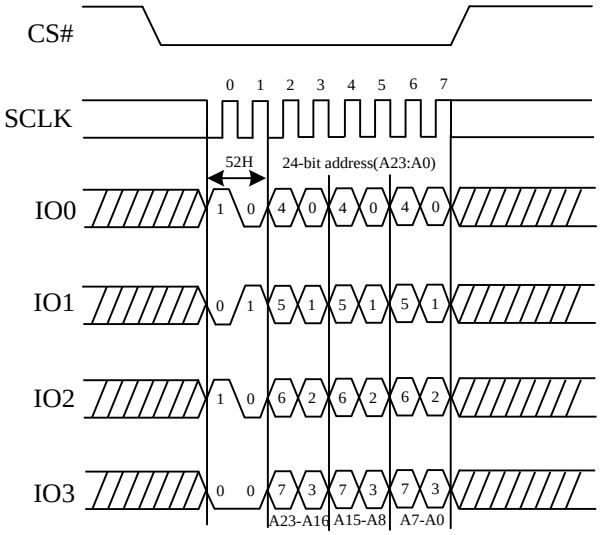
Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 46. 32KB Block Erase Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 47. 32KB Block Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.15. 64KB Block Erase (D8H/DCH)

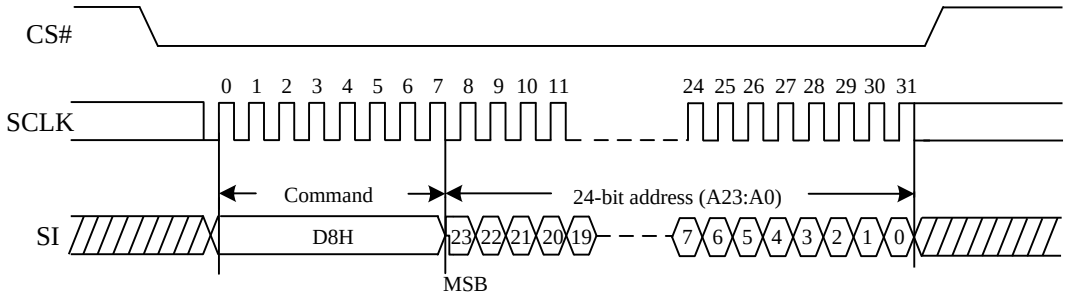
The 64KB Block Erase (BE) command is for erasing all the data of the chosen block. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the 64KB Block Erase command. The 64KB Block Erase (BE) command is entered by driving CS# low, followed by the command code, and three address bytes on SI, driving CS# high. Any address inside the block is a valid address for the 64KB Block Erase (BE) command.

The 64KB Block Erase command sequence: CS# goes low → Sending 64KB Block Erase command → 3-byte address on SI → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the last address byte has been latched in; otherwise the 64KB Block Erase (BE) command will not be executed. As soon as CS# is driven high, the self-timed Block Erase cycle (whose duration is tBE2) is initiated. While the Block Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Block Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. A 64KB Block Erase (BE) command applied to a block which is protected by the Block Protect (BP4, BP3, BP2, BP1, BP0) bits will not be executed.

The "DCH" instruction is similar to "D8H" instruction except the address length becomes 32-bit.

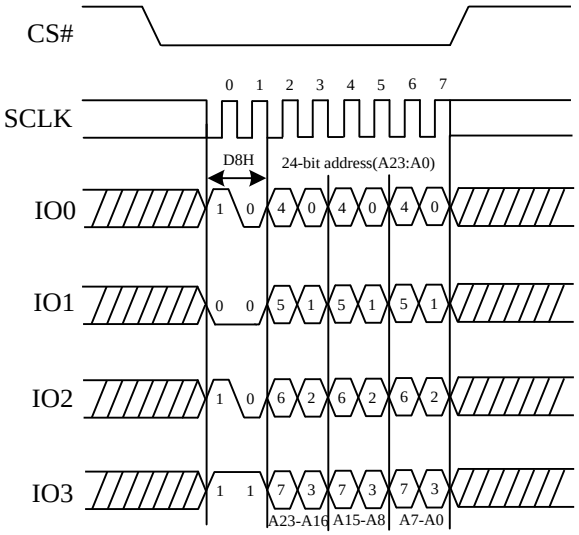
Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 48. 64KB Block Erase Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 49. 64KB Block Erase Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.4.16. Chip Erase (60H or C7H)

The Chip Erase (CE) command is for erasing all the data of the chip. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit, before sending the Chip Erase command .The Chip Erase (CE) command is entered by driving CS# Low, followed by the command code on SI.

The Chip Erase command sequence: CS# goes low → Sending Chip Erase command → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latch in, otherwise the Chip Erase command will not be executed. As soon as CS# is driven high, the self-timed Chip Erase cycle (whose duration is tCE) is initiated. While the Chip Erase cycle is in progress, the Status Register can be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Chip Erase cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Chip Erase (CE) command is ignored if one or more sectors are protected.

Note: Power disruption during the erase operation will cause incomplete erase, thus it is recommended to perform a re-erase once power resume.

Figure 50. Chip Erase Sequence Diagram

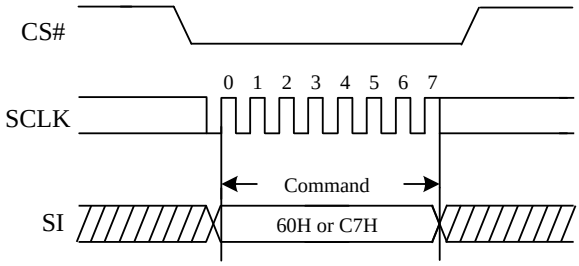
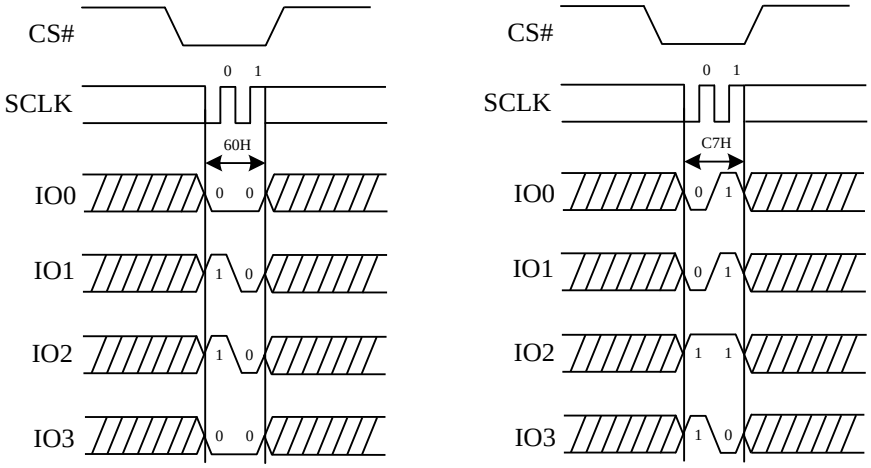


Figure 51. Chip Erase Sequence Diagram (QPI)



7.5. Device Operations

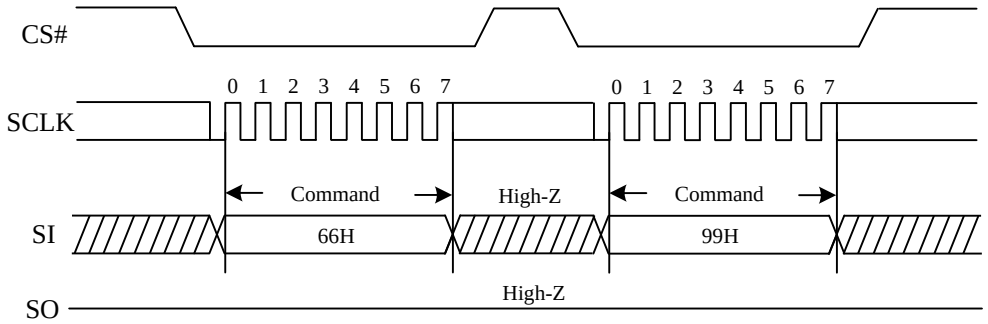
7.5.1. Enable Reset (66H) and Reset (99H)

If the Reset command is accepted, any on-going internal operation will be terminated and the device will return to its default power-on state and lose all the current volatile settings, such as Volatile Status Register bits, Write Enable Latch status (WEL), Read Parameter setting (P7-P0) and Wrap bit Setting (W6-W4).

The “Reset (99H)” command sequence as follow: CS# goes low → Sending Enable Reset command → CS# goes high → CS# goes low → Sending Reset command → CS# goes high. Once the Reset command is accepted by the device, the device will take approximately tRST_R to reset. During this period, no command will be accepted. Data corruption may happen if there is an on-going internal Erase or Program operation when Reset command sequence is accepted by the device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

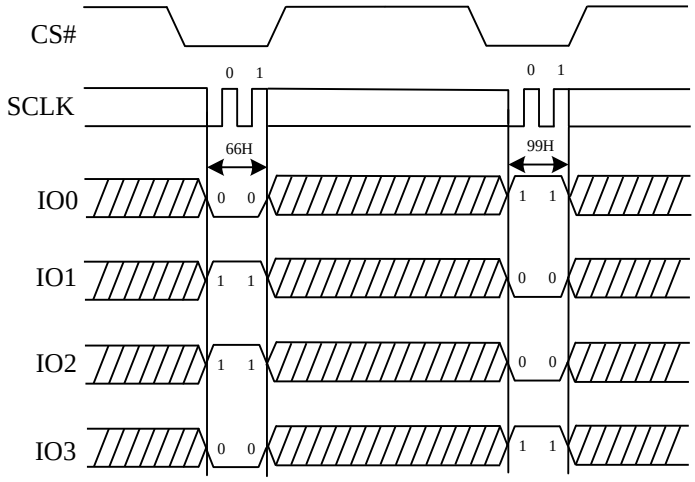
The Enable Reset (66H) command must be issued prior to a Reset(99H) command and any other commands can't be inserted between them. Otherwise, Enable Reset (66H) command will be cleared.

Figure 52. Enable Reset and Reset command Sequence Diagram (SPI)



Note: Enable Reset (66H) and Reset (99H) commands can exit SPI-BBH/SPI-EBH Continuous Read Mode.

Figure 53. Enable Reset and Reset command Sequence Diagram (QPI)



Note: Enable Reset (66H) and Reset (99H) commands can exit QPI-EBH Continuous Read Mode, and the only way to exit DTR Continuous Read Mode is to set the “Continuous Read Mode” bits (M5-4) not equal to (1,0).

7.5.2. Write Enable (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Write Status Register (WRSR), Write Extended Address Register (WEAR), Write Configuration Register (WCR) and Erase/Program Security Registers command. The Write Enable (WREN) command sequence: CS# goes low → Sending the Write Enable command → CS# goes high.

Figure 54. Write Enable Sequence Diagram

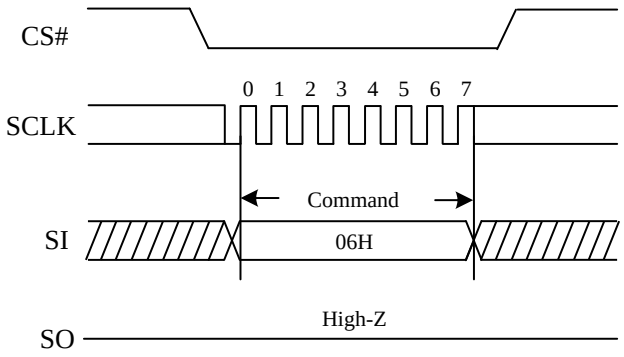
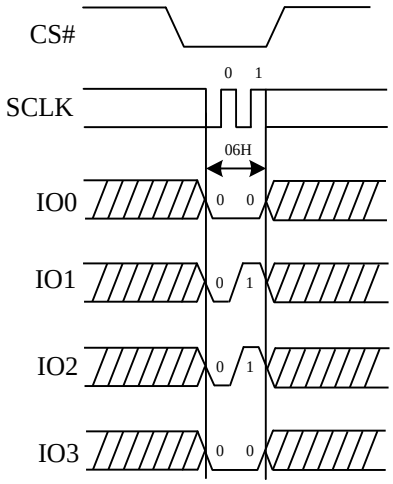


Figure 55. Write Enable Sequence Diagram (QPI)



7.5.3. Write Enable for Volatile Status Register (50H)

The non-volatile Status Register bits can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. The Write Enable for Volatile Status Register command must be issued prior to a Write Status Register command (01H/31H/11H) or Write Configuration Register command (B1H), and any other commands can't be inserted between them. Otherwise, Write Enable for Volatile Status Register will be cleared. The Write Enable for Volatile Status Register command will not set the Write Enable Latch bit, it is only valid for the Write Status Register command to change the volatile Status Register bit values.

Figure 56. Write Enable for Volatile Status Register Sequence Diagram

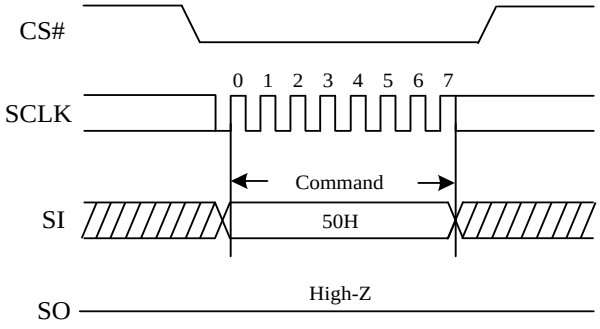
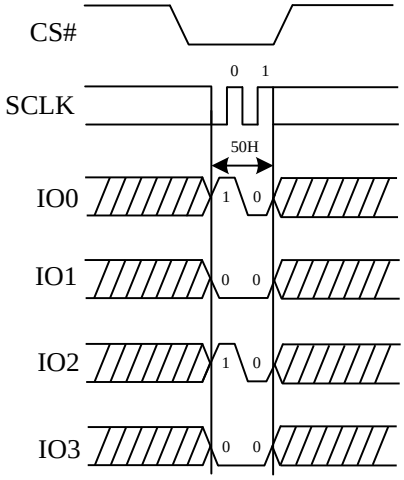


Figure 57. Write Enable for Volatile Status Register Sequence Diagram (QPI)



7.5.4. Write Disable (04H)

The Write Disable (WRDI) command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low → Sending the Write Disable command → CS# goes high. The WEL bit is reset by following condition: Write Disable command (WRDI); Power-up; upon completion of the Write Status Register (WRSR), Write Extended Address Register (WEAR), Write Configuration Register (WCR), Page Program (PP), Quad Page Program, Extended Quad Input Fast Program, Sector Erase (SE), Block Erase (BE), Chip Erase (CE), Erase/Program Security Registers and Reset commands.

Figure 58. Write Disable Sequence Diagram

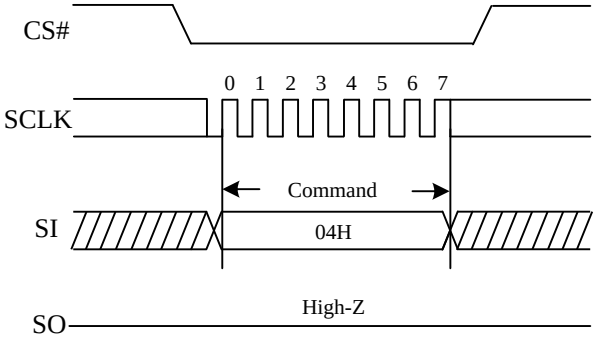
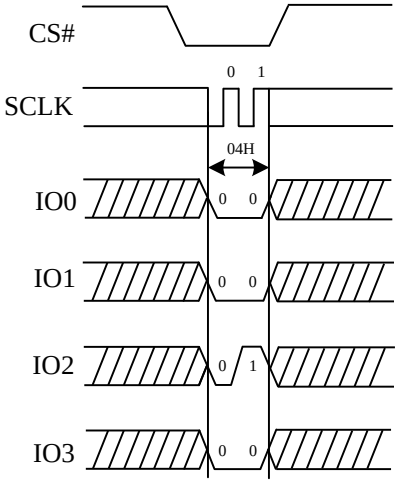


Figure 59. Write Disable Sequence Diagram (QPI)



7.5.5. Program/Erase Suspend (75H)

The Program/Erase Suspend command (75H), allows the system to interrupt a Page Program or Sector/Block Erase operation and then read data from any other sector or block. The Write Status Register command (01H, 31H, 11H) and Erase/Program Security Registers command (44H, 42H) and Erase commands (20H, 21H, 52H, 5CH, D8H, DCH, C7H, 60H) and Page Program command (02H, 12H, 32H, 34H, C2H, 3EH) are not allowed during Program Suspend. The Write Status Register command (01H, 31H, 11H) and Program/Erase Security Registers command (44H, 42H) and Erase commands (20H, 21H, 52H, 5CH, D8H, DCH, C7H, 60H) are not allowed during Erase Suspend. Program/Erase Suspend is valid only during the Page Program or Sector/Block Erase operation. A maximum of time of "tSUS" (See AC Characteristics) is required to suspend the Program/Erase operation.

The Program/Erase Suspend command will be accepted by the device only if the SUS bit in the Status Register equals to 0 and WIP bit equals to 1 while a Page Program or a Sector or Block Erase operation is on-going. If the SUS bit equals to 1 or WIP bit equals to 0, the Suspend command will be ignored by the device. The WIP bit will be cleared from 1 to 0 within "tSUS" and the SUS bit will be set from 0 to 1 immediately after Program/Erase Suspend. A power-off during the suspend period will reset the device and release the suspend state. The command sequence is shown in the figure below.

Figure 60. Program/Erase Suspend Sequence Diagram

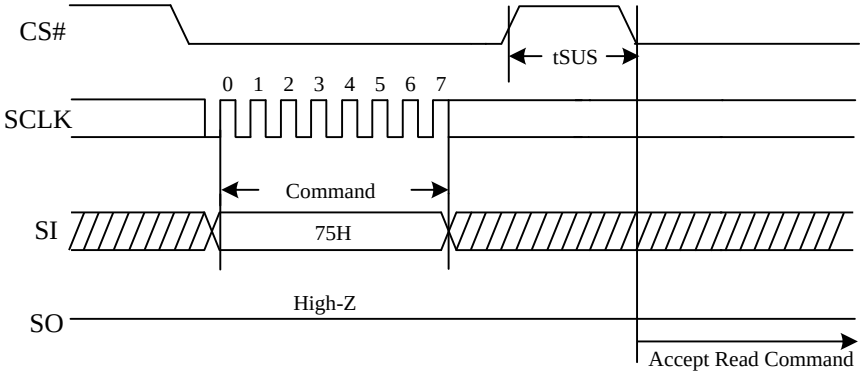
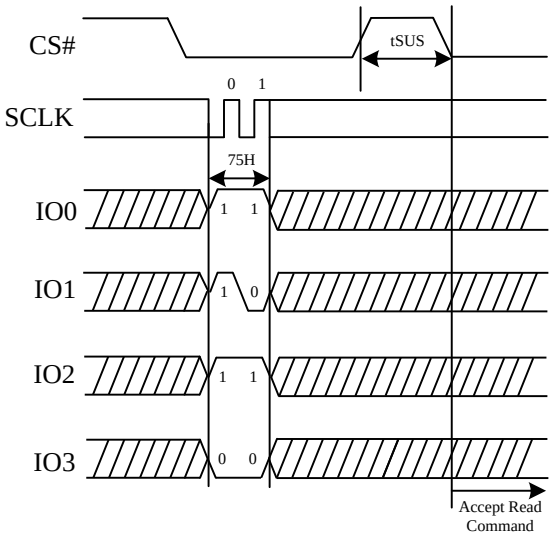


Figure 61. Program/Erase Suspend Sequence Diagram(QPI)



7.5.6. Program/Erase Resume (7AH)

The Program/Erase Resume command must be written to resume the Page Program or Sector/Block Erase operation after a Program/Erase Suspend command. The Program/Erase Resume command will be accepted by the device only if the SUS bit equals to 1 and the WIP bit equals to 0. The SUS bit in the status register will be cleared from 1 to 0 immediately after the Program/Erase Resume command is sent, the WIP bit will be set from 0 to 1 within 200ns and the Sector/Block Erase operation or the Page Program operation will continue. The Program/Erase Resume command will be ignored unless a Program/Erase Suspend is active. The command sequence is shown in the figure below.

Figure 62. Program/Erase Resume Sequence Diagram

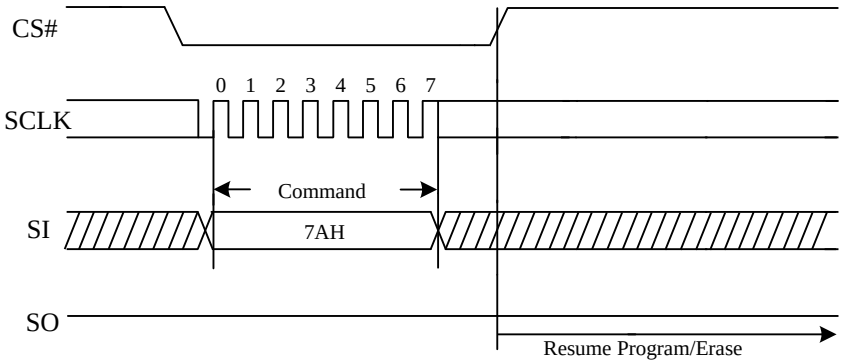
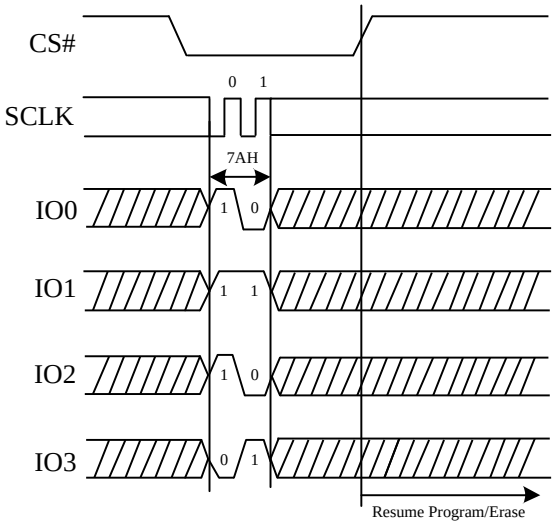


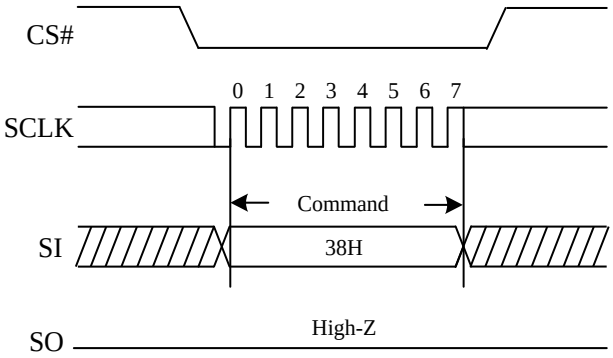
Figure 63. Program/Erase Resume Sequence Diagram (QPI)



7.5.7. Enable QPI (38H)

The device supports both Standard/Dual/Quad SPI and QPI mode. The “Enable QPI (38H)” command can switch the device from SPI mode to QPI mode. See the command Table for all supported QPI commands. In order to switch the device to QPI mode, the Quad Enable (QE) bit in Status Register must be set to 1 first, and “Enable QPI (38H)” command must be issued. If the QE bit is 0, the “Enable QPI (38H)” command will be ignored and the device will remain in SPI mode. When the device is switched from SPI mode to QPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged.

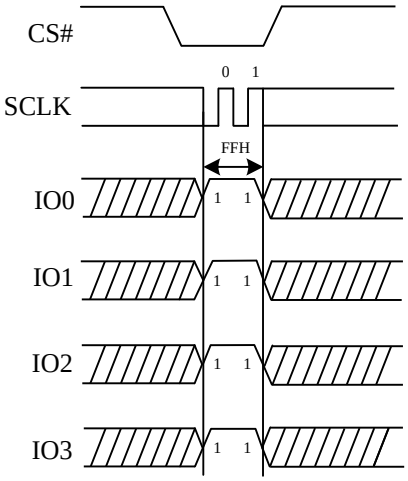
Figure 64. Enable QPI mode command Sequence Diagram



7.5.8. Disable QPI (FFH)

To exit the QPI mode and return to Standard/Dual/Quad SPI mode, the “Disable QPI (FFH)” command must be issued. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch and the Wrap Length setting will remain unchanged.

Figure 65. Disable QPI mode command Sequence Diagram (QPI)



7.5.9. Set Burst With Wrap (77H)

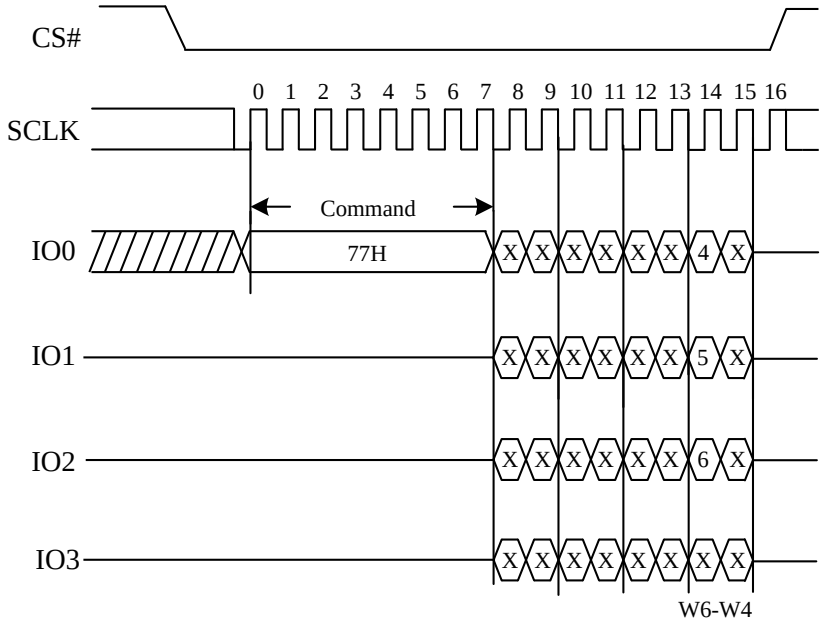
The Set Burst with Wrap command is used in conjunction with "Quad I/O Fast Read (EBH)" and "DTR Fast Read Quad I/O (EDH)" commands to access a fixed length of 16/32/64-byte section within a 256-byte page in standard SPI mode. The Set Burst with Wrap command sequence: CS# goes low →Send Set Burst with Wrap command →Send 24 dummy bits →Send 8 bits "Wrap bits"→CS# goes high.

W6, W5	W4=0		W4=1 (default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0,0 (Default)	Yes	16-byte	No	N/A
0,1	Yes	16-byte	No	N/A
1,0	Yes	32-byte	No	N/A
1,1	Yes	64-byte	No	N/A

If the W6-W4 bits are set by the Set Burst with Wrap command, all the following "Quad I/O Fast Read (EBH)" and "DTR Fast Read Quad I/O (EDH)" command will use the W6-W4 setting to access the 16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap command should be issued to set W4=1.

The Wrap Length set by W5-W6 in Standard SPI mode is still valid in QPI mode and can also be re-configured by "Set Read Parameters (C0H) command, and vice versa.

Figure 66. Set Burst with Wrap Sequence Diagram



7.5.10. Set Read Parameters (C0H)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, “Set Read Parameters (C0H)” instruction can be used to configure the number of dummy clocks for “Fast Read (0BH)”, “Fast Read Quad I/O (EBH)”, “Read SFDP (5AH)”, “Read Unique ID (4BH)”, “Read Security Register (48H)” instructions, and to configure the number of bytes of “Wrap Length” for “Quad I/O Fast Read (EBH)” and “DTR Fast Read Quad I/O (EDH)” instruction. In Standard SPI mode, the “Set Read Parameters (C0H)” instruction is not accepted.

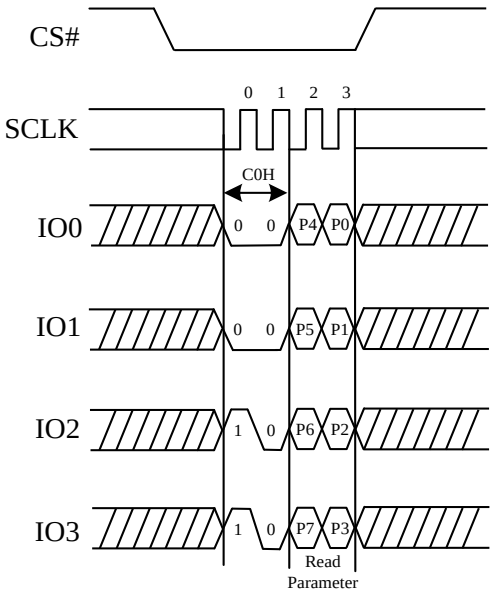
The number of dummy clocks in QPI mode is determined by the setting of C0H. The dummy clock clocks in SPI mode is set to the default value or determined by the LC bit setting.

The default “Wrap Length” after a power up or a Reset instruction is 16 bytes, the default number of dummy clocks is 8. The “Wrap Length” is set by W6-4 bit in the “Set Burst with Wrap (77H)” instruction in Standard SPI mode and by P1-P0 in the “Set Read Parameters (C0H)” in the QPI mode. The Wrap Length set by P1-P0 in QPI mode is still valid in SPI mode and can also be re-configured by “Set Burst with Wrap (77H)”, and vice versa.

“C0H” adds an extra bit P2 for Disable/Enable Wrap function. Execute C0H and then follows EBH/ECH or EDH/EEH, performs the read operation with “Wrap Around” in QPI mode. This function is similar to the “Fast Read (0BH)” command in QPI mode, except the addressing of the read operation will “Wrap Around” to the beginning boundary of the “Wrap Around” once the ending boundary is reached. The “Wrap Length” and the number of dummy clocks can be configured by the “Set Read Parameters (C0H)” command.

P5-P4	Dummy Clocks	P2	P1-P0	Wrap Length
0 0 (Default)	8	Enable Wrap=0	0 0 (Default)	16-byte
0 1	6	Disable Wrap=1 (Default)	0 1	16-byte
1 0	12		1 0	32-byte
1 1	16		1 1	64-byte

Figure 67. Set Read Parameters command Sequence Diagram (QPI)



7.5.11. Enable 4-byte Mode (B7H)

The Enable 4-byte Mode command enables accessing the address length of 32-bit for the memory area of the higher density (larger than 128Mb). The device default is in 24-bit address mode. After sending the Enable 4-byte Mode command, the ADS bit will be set to 1 to indicate the 4-byte address mode has been enabled. Once the 4-byte address mode is enabled, the address length becomes 32-bit instead of the default 24 bit. The Disable 4-byte mode or Reset or Power-off will disable 4-byte mode.

Figure 68. Enable 4-byte Mode Sequence Diagram (SPI)

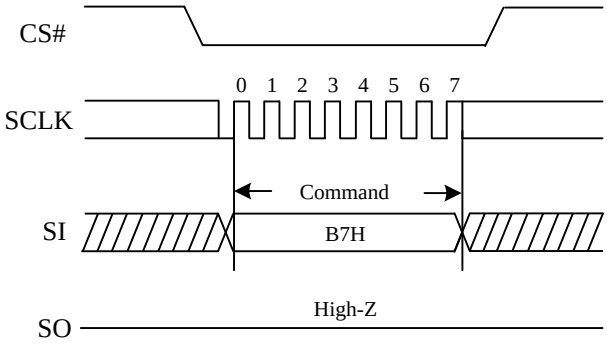
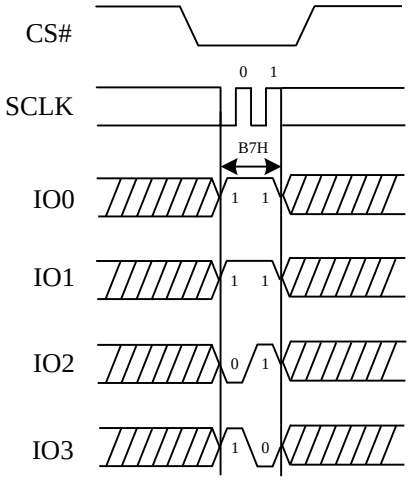


Figure 69. Enable 4-byte Mode Sequence Diagram (QPI)



7.5.12. Disable 4-byte Mode (E9H)

The Disable 4-byte Mode command is executed to exit the 4-byte address mode and return to the default 3-byte address mode. After sending the Disable 4-byte Mode command, the ADS bit will be clear to be 0 to indicate the 4-byte address mode has been disabled, and then the address length will return to 24-bit.

Figure 70. Disable 4-byte Mode Sequence Diagram (SPI)

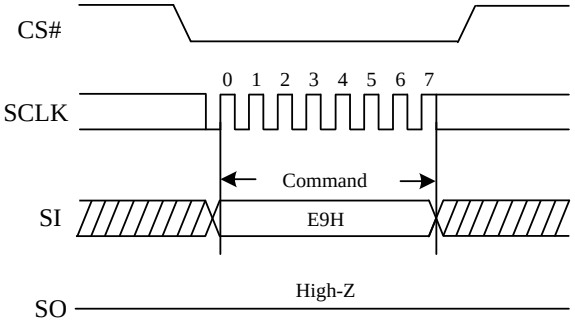
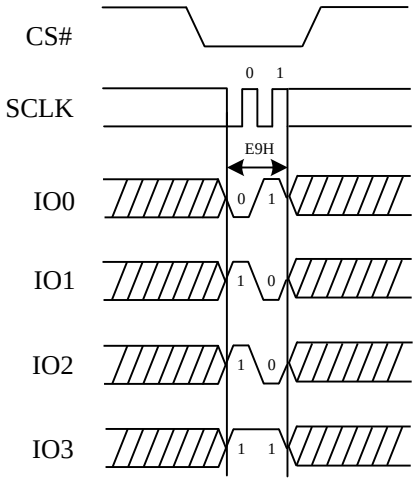


Figure 71. Disable 4-byte Mode Sequence Diagram (QPI)



7.5.13. Clear SR Flags (30H)

The Clear Status Register Flags command resets S18 (Program Error bit) and S19 (Erase Error bit) from status register. It is not necessary to set the WEL bit before the Clear Status Register command is executed. The Clear SR command will be not accepted when the device remains busy with WIP set to 1, as the device does remain busy when either error bit is set. The WEL bit will be unchanged after this command is executed.

Figure 72. Clear Status Register Flags Sequence Diagram (SPI)

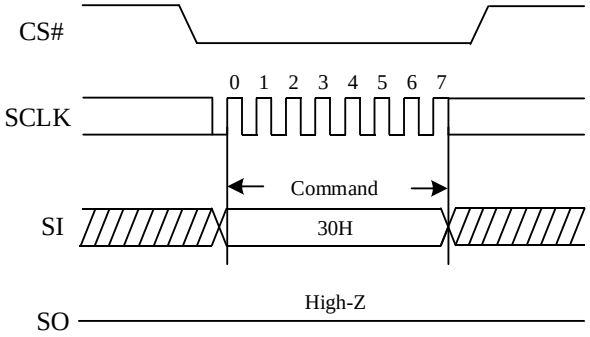
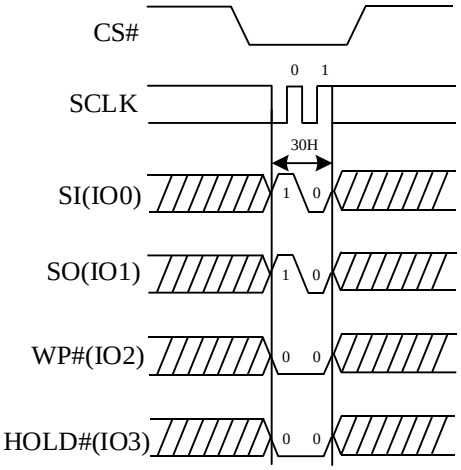


Figure 73. Clear Status Register Flags Sequence Diagram (QPI)



7.5.14. Deep Power-Down (B9H)

Executing the Deep Power-Down (DPD) command is the only way to put the device in the lowest power consumption mode (the Deep Power-Down Mode). It can also be used as an extra software protection mechanism, since in this mode, the device ignores all Write, Program and Erase commands. Driving CS# high deselects the device, and puts the device in the Standby Mode (if there is no internal cycle currently in progress). But the Standby Mode is different from the Deep Power-Down Mode. The Deep Power-Down Mode can only be entered by executing the Deep Power-Down (DPD) command. Once the flash memory has entered the Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down and Read Device ID command (ABH) and Software Reset command (66H+99H). This command releases the device from the Deep Power-Down Mode.

The Deep Power-Down Mode automatically stops at Power-Off, and the device always Power-Up in the Standby Mode.

The Deep Power-Down command sequence: CS# goes low → Sending Deep Power-Down command → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latched in; otherwise the Deep Power-Down (DPD) command will not be executed. As soon as CS# is driven high, it requires a time duration of tDP before the supply current is reduced to ICC2 and the Deep Power-Down Mode is entered. Any input of Deep Power-Down (DPD) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

Figure 74. Deep Power-Down Sequence Diagram

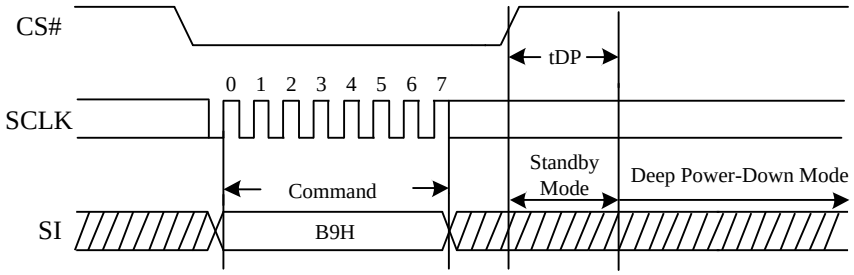
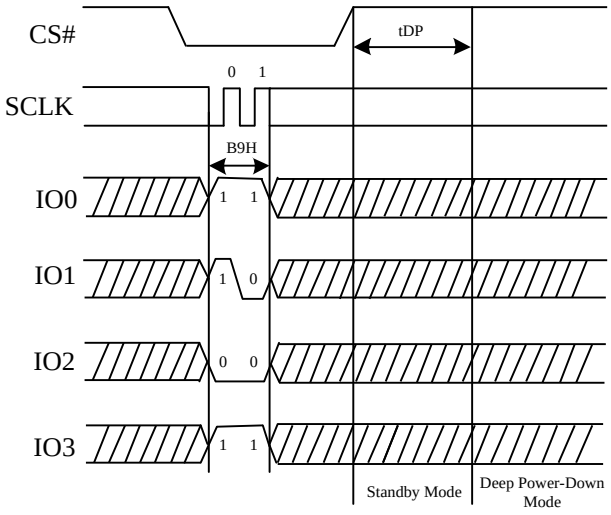


Figure 75. Deep Power-Down Sequence Diagram (QPI)



7.5.15. Release From Deep Power-Down (ABH)

The Release from Deep Power-Down and Read Device ID command is a multi-purpose command. It can be used to release the device from Deep Power-Down Mode or obtain the devices electronic identification (ID) number.

To release the device from Deep Power-Down Mode, the command is issued by driving the CS# pin low, shifting the instruction code (ABH) and driving CS# high as shown in the Figure below. Release from Deep Power-Down Mode will take the time duration of tRES1 (See AC Characteristics) before the device resume to normal state and other command are accepted. The CS# pin must remain high during the tRES1 time duration.

When the command is used only to obtain the Device ID while the flash memory is not in Deep Power-Down Mode, the command is initiated by driving the CS# pin low and shifting the instruction code (ABH) followed by 3 dummy bytes. The Device ID bits are then shifted out on the falling edge of SCLK with most significant bit (MSB) first as shown in the Figure below. The Device ID value is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The command is completed by driving CS# high.

When the command is used to release the device from Deep Power-Down Mode and obtain the Device ID, the command is the same as previously described, and shown in the Figure below, except that after CS# is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume to normal mode and other command will be accepted. If the Release from Deep Power-Down and Read Device ID command is issued while an Erase, Program or Write cycle is in process (when WIP equals to 1) the command will be ignored and will not affect the current cycle.

Figure 76. Release Power-Down Sequence Diagram

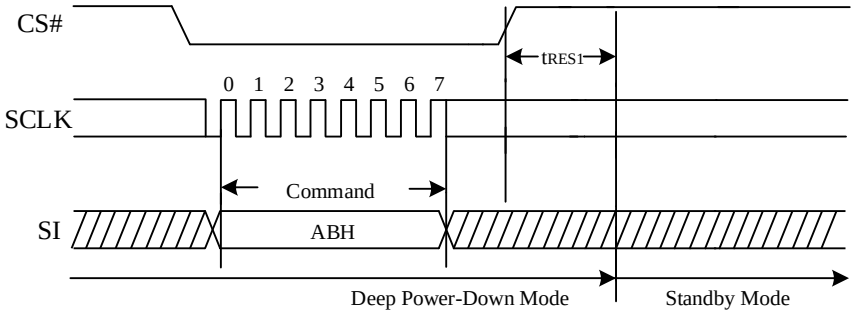


Figure 77. Release Power-Down Sequence Diagram (QPI)

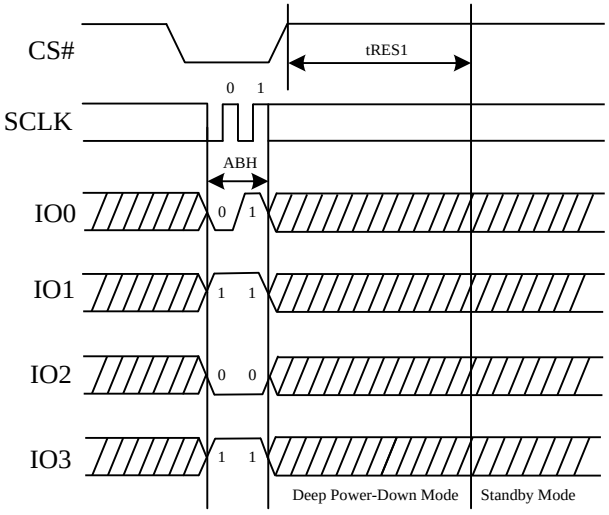
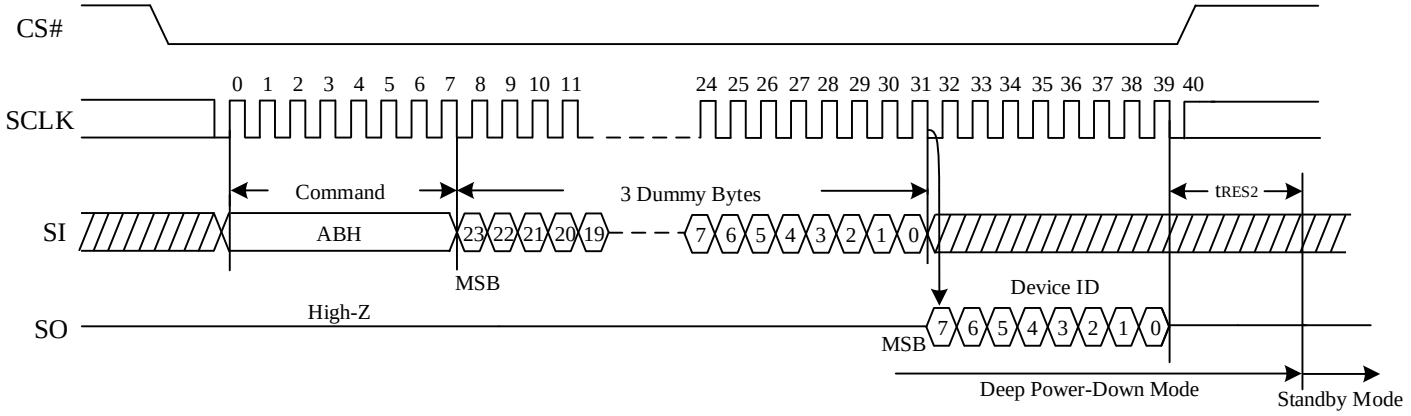


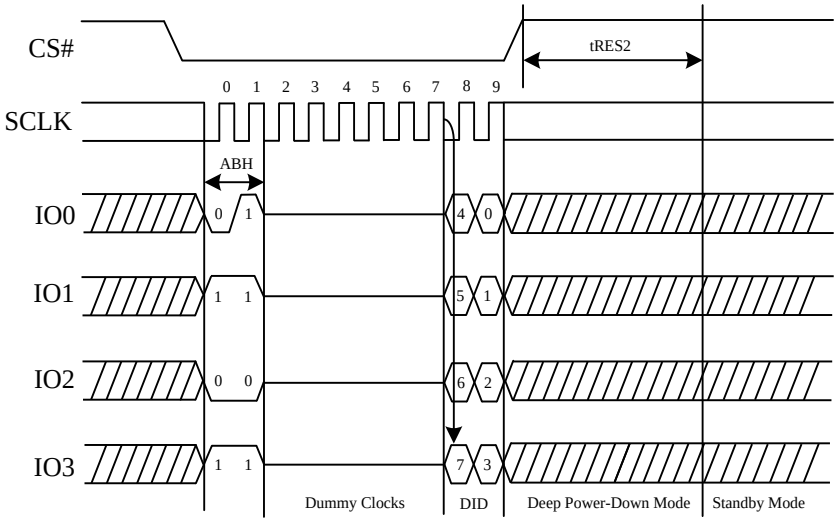
Figure 78. Release from Deep Power-Down/Read Device ID Sequence Diagram



Release from Deep Power-Down/Read Device ID (ABH) in QPI mode

The Release from Deep Power-Down/Read Device ID command is also supported in QPI mode. See the figure below. The number of Dummy clocks for "Release from Deep Power-Down/Read Device ID (ABH)" is 6.

Figure 79. Release Power-Down/Read Device ID Sequence Diagram (QPI)



7.6. One-Time Programmable (OTP) Operations

7.6.1. Erase Security Register (44H)

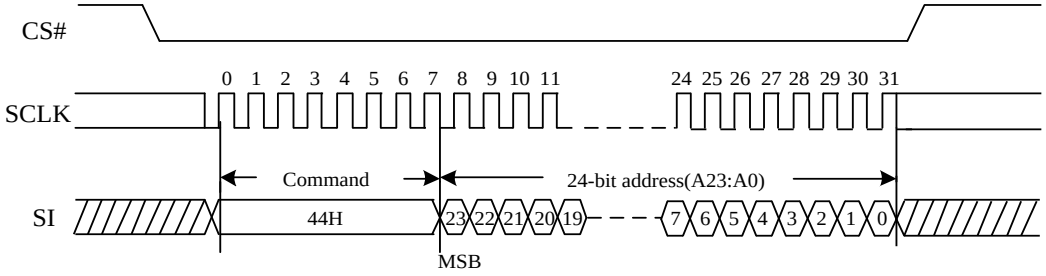
The device provides 3x1024-byte Security Registers which can be erased per 1024-byte at a time. These registers may be used by the system manufacturers to store security and other important information separately from the main memory array.

The Erase Security Registers command is similar to Sector/Block Erase command. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit.

The Erase Security Registers command sequence: CS# goes low → Sending Erase Security Registers Command → Sending 24-bit Address → CS# goes high. The command sequence is shown in the figure below. CS# must be driven high after the eighth bit of the command code has been latched in, otherwise the Erase Security Registers command is not executed. As soon as CS# is driven high, the self-timed Erase Security Registers cycle (whose duration is tSE) is initiated. While the Erase Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Erase Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset. The Security Registers Lock bit (LB1, LB2, LB3) in the Status Register can be used to OTP protect the security registers. Once the lock bit is set to 1, the corresponding Security Registers (#1, #2, #3) will be permanently locked; the Erase Security Registers command will be ignored.

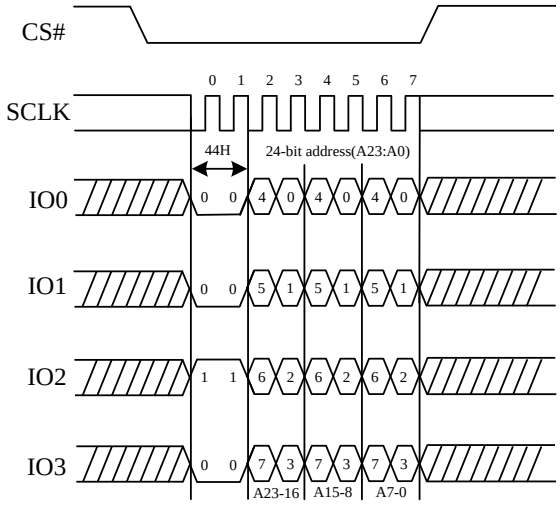
Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Registers #1	00000000b	0001b	00b	Don't Care
Security Registers #2	00000000b	0010b	00b	Don't Care
Security Registers #3	00000000b	0011b	00b	Don't Care

Figure 80. Erase Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 81. Erase Security Registers command Sequence Diagram (QPI)



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

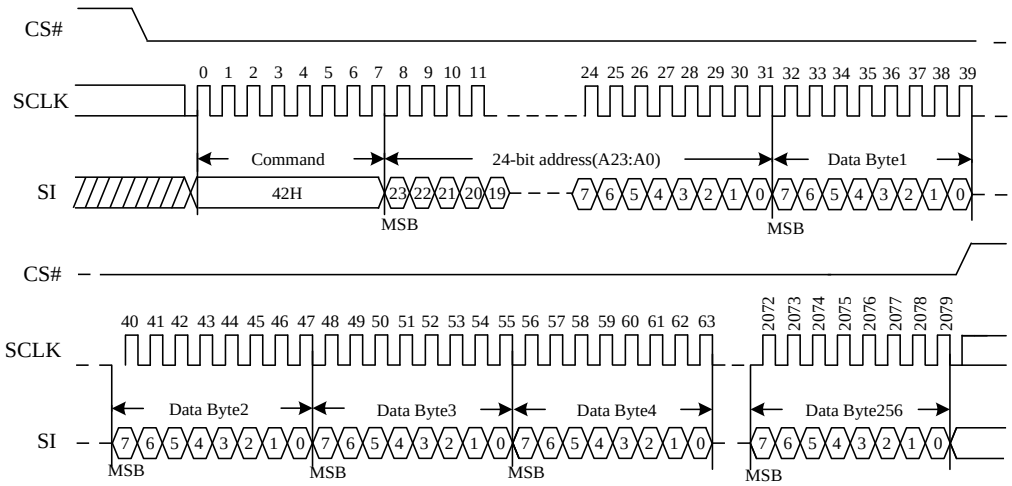
7.6.2. Program Security Register (42H)

The Program Security Registers command is similar to the Page Program command. It allows from 1 to 1024 bytes Security Registers data to be programmed. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Program Security Registers command. The Program Security Registers command is entered by driving CS# Low, followed by the command code (42H), three address bytes and at least one data byte on SI. As soon as CS# is driven high, the self-timed Program Security Registers cycle (whose duration is tPP) is initiated. While the Program Security Registers cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Program Security Registers cycle, and is 0 when it is completed. At some unspecified time before the cycle is completed, the Write Enable Latch (WEL) bit is reset.

If the Security Registers Lock bit (LB1, LB2, LB3) is set to 1, the corresponding Security Registers (#1, #2, #3) will be permanently locked. Program Security Registers command will be ignored.

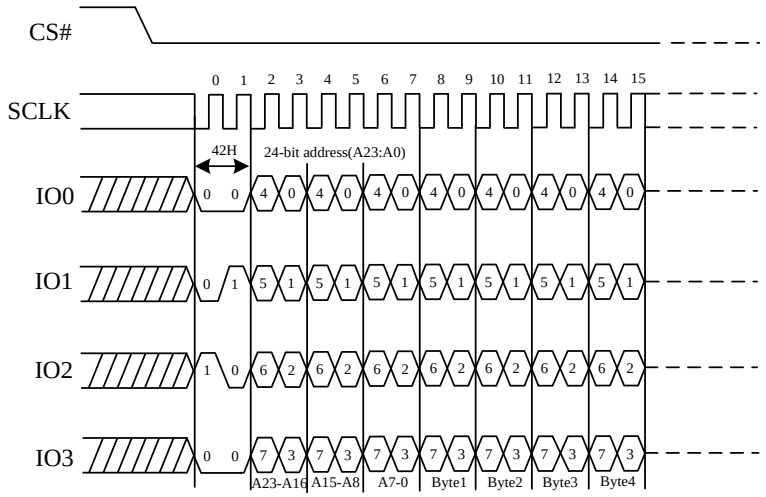
Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Registers #1	00000000b	0001b	00b	Byte Address
Security Registers #2	00000000b	0010b	00b	Byte Address
Security Registers #3	00000000b	0011b	00b	Byte Address

Figure 82. Program Security Registers command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 83. Program Security Registers command Sequence Diagram (QPI)



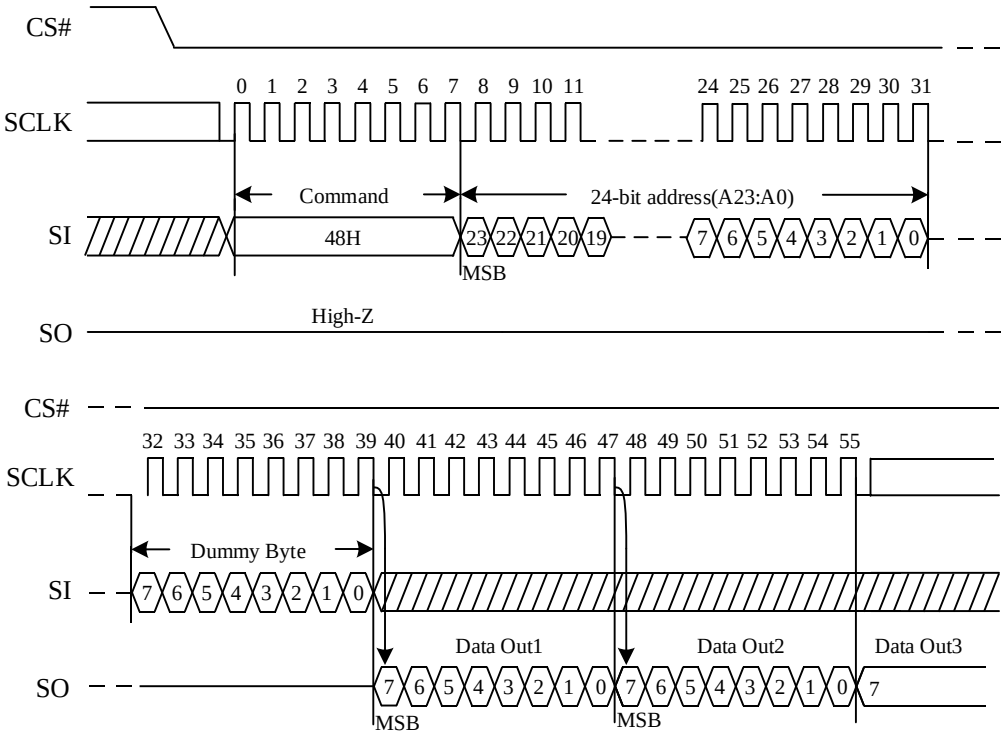
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.6.3. Read Security Register (48H)

The Read Security Registers command is similar to Fast Read command. The command is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency fC, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next address after each byte of data is shifted out. Once the A9-A0 address reaches the last byte of the register (Byte 3FFH), it will reset to 000H, the command is completed by driving CS# high.

Address	A23-A16	A15-A12	A11-A10	A9-A0
Security Registers #1	00000000b	0001b	00b	Byte Address
Security Registers #2	00000000b	0010b	00b	Byte Address
Security Registers #3	00000000b	0011b	00b	Byte Address

Figure 84. Read Security Registers command Sequence Diagram

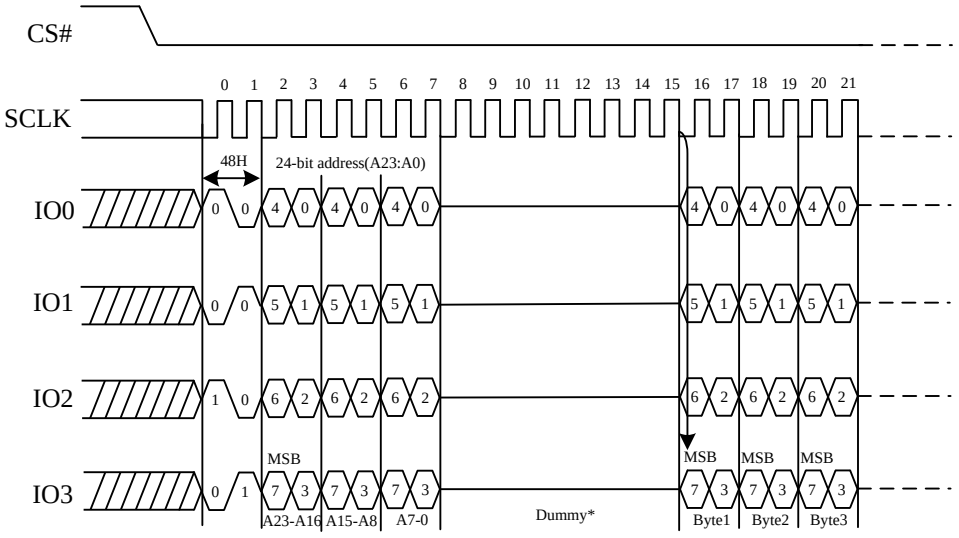


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.
Note: The Byte Address A2-A0 must be 000.

Read Security Register in QPI Mode"

The Read Security Register command is also supported in QPI mode. See the following figure. In QPI mode, the number of dummy clocks is configured by the "Set Read Parameters (C0H)" command to accommodate a wide range application with different needs for either maximum Fast Read frequency or minimum data access latency. Depending on the Read Parameter bits P[5:4] setting, the number of dummy clocks can be configured as either 8/6/12/16.

Figure 85. Read Security Registers command Sequence Diagram (QPI)



*Set Read Parameters Command (C0H) can set the number of Dummy clocks

Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

7.7. Advanced Sector Protection Operations

7.7.1. Global Block/Sector Lock (7EH) or Unlock (98H)

All Block/Sector Lock bits can be set to 1 by the Global Block/Sector Lock command, or can set to 0 by the Global Block/Sector Unlock command.

The Global Block/Sector Lock command (7EH) sequence: CS# goes low → SI: Sending Global Block/Sector Lock command → CS# goes high. The command sequence is shown in the Figure below.

The Global Block/Sector Unlock command (98H) sequence: CS# goes low → SI: Sending Global Block/Sector Unlock command → CS# goes high. The command sequence is shown in the Figure below.

Figure 86. The Global Block/Sector Lock Sequence Diagram

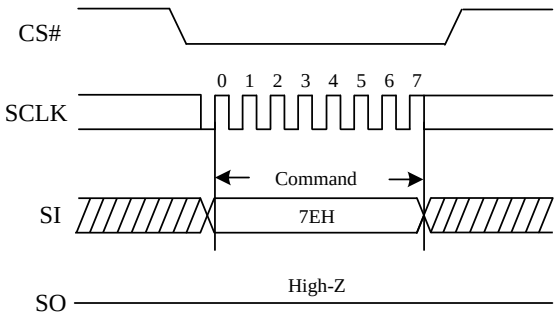


Figure 87. The Global Block/Sector Lock Sequence Diagram (QPI)

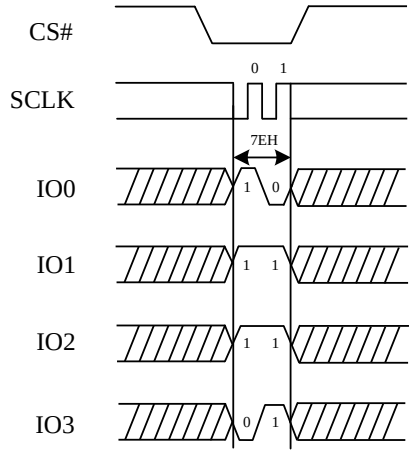


Figure 88. The Global Block/Sector Unlock Sequence Diagram

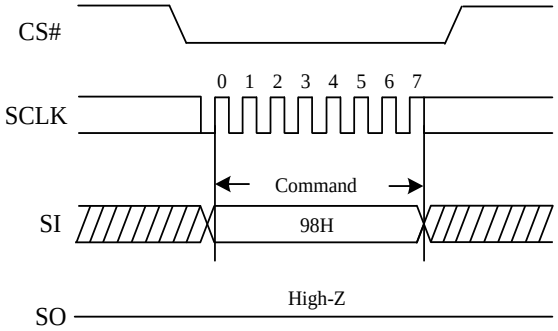
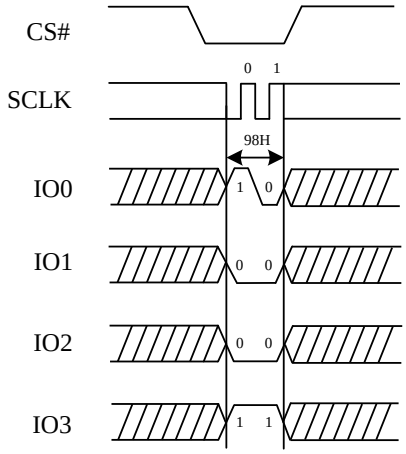


Figure 89. The Global Block/Sector Unlock Sequence Diagram (QPI)



7.7.2. Individual Block/Sector Lock (36H)/Unlock (39H)/Read (3DH)

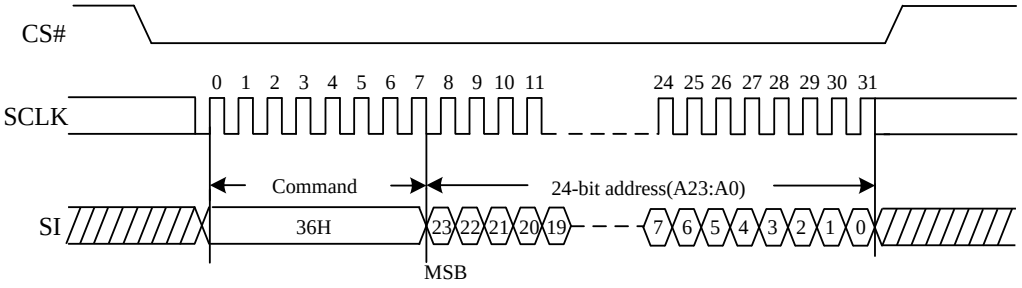
The individual block/sector lock provides an alternative way to protect the memory array from adverse Erase/Program. In order to use the Individual Block/Sector Locks, the WPS bit in Status Register must be set to 1. If WPS=0, the write protection will be determined by BP (4:0) bits in the Status Register. The Individual Block/Sector Lock bits are volatile bits, the default values of which after device power up or after a Reset are 1.

The individual Block/Sector Lock command (36H) sequence: CS# goes low → SI: Sending individual Block/Sector Lock command → SI: Sending 24bits individual Block/Sector Lock Address → CS# goes high. The command sequence is shown in the Figure below.

The individual Block/Sector Unlock command (39H) sequence: CS# goes low → SI: Sending individual Block/Sector Unlock command → SI: Sending 24bits individual Block/Sector Lock Address → CS# goes high. The command sequence is shown in the Figure below.

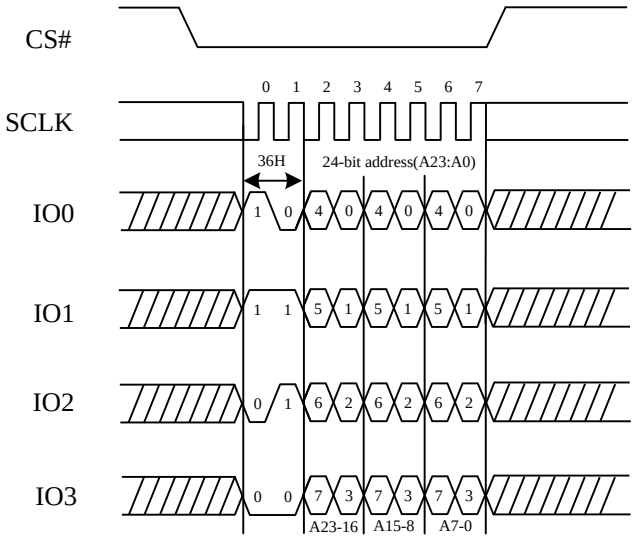
The Read individual Block/Sector lock command (3DH) sequence: CS# goes low → SI: Sending Read individual Block/Sector Lock command → SI: Sending 24bits individual Block/Sector Lock Address → SO: The Block/Sector Lock Bit will out → CS# goes high. If the least significant bit(LSB) is 1, the corresponding block/sector is locked, if the LSB is 0, the corresponding block/sector is unlocked, Erase/Program operation can be performed. The command sequence is shown in the Figure below.

Figure 90. Individual Block/Sector Lock command Sequence Diagram



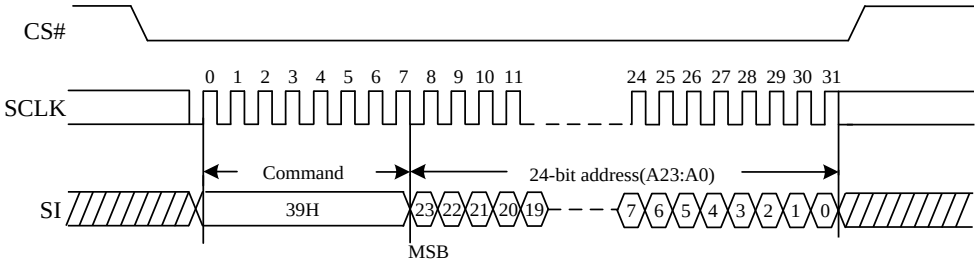
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 91. Individual Block/Sector Lock command Sequence Diagram (QPI)



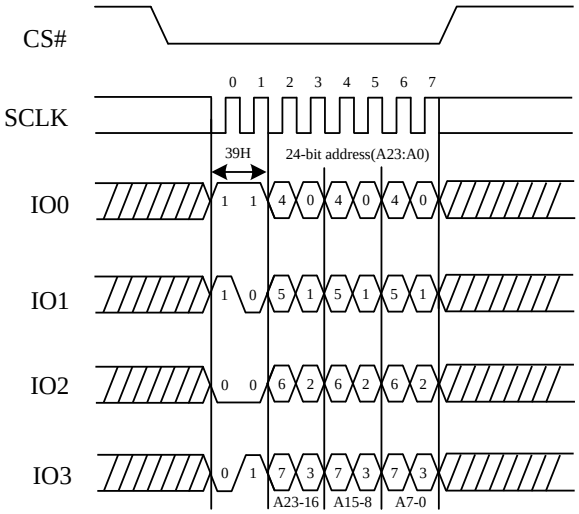
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 92. Individual Block/Sector Unlock command Sequence Diagram



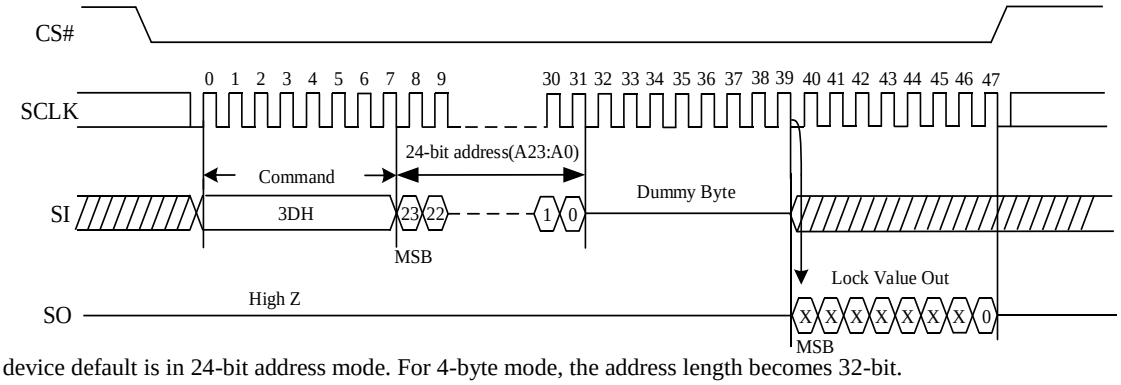
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 93. Individual Block/Sector Unlock command Sequence Diagram (QPI)



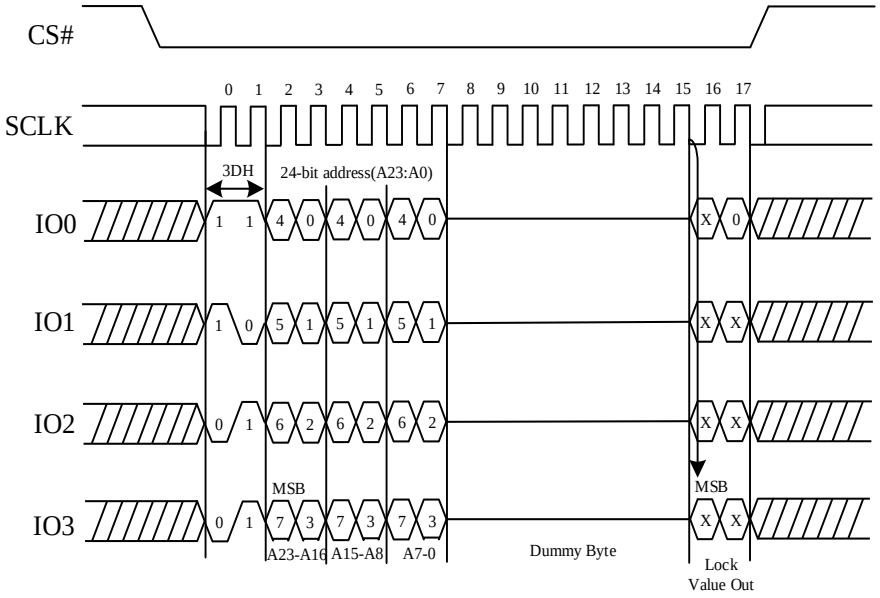
Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 94. Read Individual Block/Sector lock command Sequence Diagram



Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

Figure 95. Read Individual Block/Sector lock command Sequence Diagram (QPI)

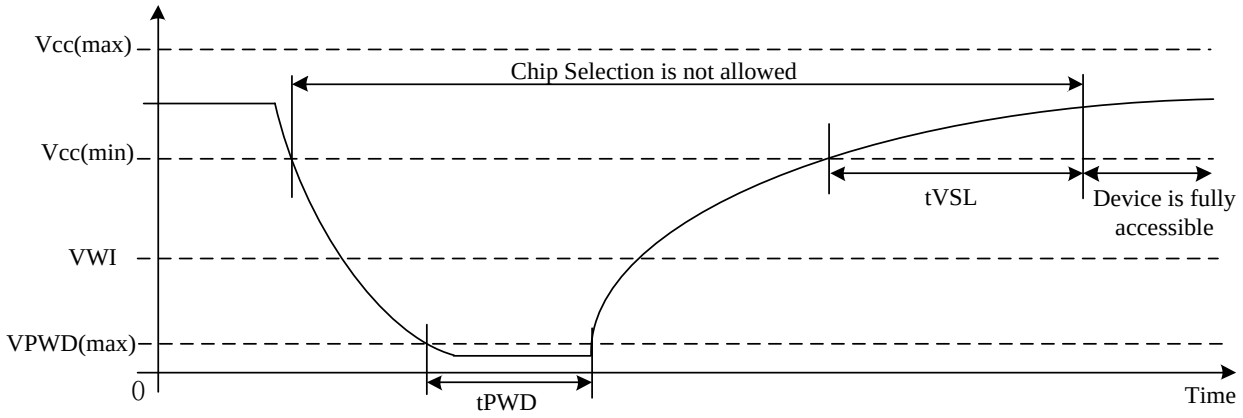


Note: The device default is in 24-bit address mode. For 4-byte mode, the address length becomes 32-bit.

8. ELECTRICAL CHARACTERISTICS

8.1. Power-Down & Power-On Timing

Figure 96. Power-On Timing Sequence Diagram



Power-Down & Power-Up Timing and Write Inhibit Threshold

Symbol	Parameter	Min.	Max.	Unit
tVSL	VCC (min) To CS# Low	200		μs
VWI	Write Inhibit Voltage	1	1.6	V
VPWD	VCC voltage needed to below VPWD for initialization	-	-	V
tPWD	The minimum duration for initialization	-	-	ms

8.2. Initial Delivery State

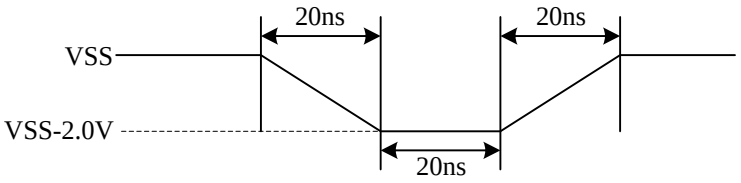
The device is delivered with the memory array erased: all bits are set to 1(each byte contains FFH). All Status Register bits except S22/CR0/CR6/CR7 bits are 0, S22/CR0/CR6/CR7 bits are 1.

8.3. Absolute Maximum Ratings

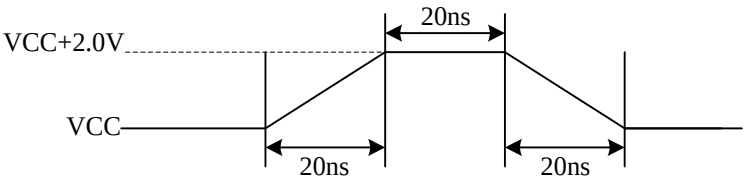
Parameter	Value	Unit
Ambient Operating Temperature	-40 to 85 -40 to 105	℃
Storage Temperature	-65 to 150	℃
Output Short Circuit Current	200	mA
Applied Input/Output Voltage	-0.5 to 2.5	V
VCC	-0.5 to 2.5	V

Figure 97. Input Test Waveform and Measurement Level

Maximum Negative Overshoot Waveform



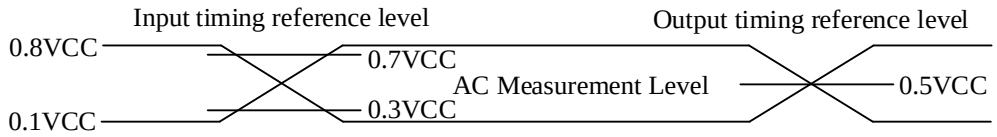
Maximum Positive Overshoot Waveform



8.4. Capacitance Measurement Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
CIN	Input Capacitance			6	pF	VIN=0V
COUT	Output Capacitance			8	pF	VOUT=0V
CL	Load Capacitance		30		pF	
	Input Rise And Fall time			5	ns	
	Input Pulse Voltage	0.1VCC to 0.8VCC			V	
	Input Timing Reference Voltage	0.3VCC to 0.7VCC			V	
	Output Timing Reference Voltage		0.5VCC		V	

Figure 98. Absolute Maximum Ratings Diagram



Note：Input pulse rise and fall time are <5ns

8.5. DC Characteristics

(TA=-40 ℃~85 ℃/TA=-40 ℃~105 ℃, VCC=1.7~2.0V)

Symbol	Parameter	Test Condition	Min.	Typ. (1)	Max. (85℃)	Max. (105℃)	Unit
ILI	Input Leakage Current				±20	±20	μA
ILO	Output Leakage Current				±20	±20	μA
ICC1	Standby Current	CS#=VCC VIN=VCC or VSS		30	300	600	μA
ICC2	Deep Power-Down Current	CS#=VCC VIN=VCC or VSS		8	100	200	μA
ICC3	Operating Current (Read)	CLK=0.1VCC/0.9VCC at 133MHz, Q=Open (*2 I/O)		24	30	35	mA
		CLK=0.1VCC/0.9VCC at 104MHz, Q=Open (*1,*2,*4 I/O)		21	25	30	mA
		CLK=0.1VCC/0.9VCC at 80MHz, Q=Open (*1,*2,*4 I/O)		14	20	25	mA
		CLK=0.1VCC/0.9VCC at 80MHz, DTR Q=Open (*4 I/O)		25	35	40	mA
ICC4	Operating Current (PP)	CS#=VCC			25	30	mA
ICC5	Operating Current (WRSR)	CS#=VCC			20	30	mA
ICC6	Operating Current (SE)	CS#=VCC			25	30	mA
ICC7	Operating Current (BE)	CS#=VCC			25	30	mA
ICC8	Operating Current (CE)	CS#=VCC			50	60	mA
VIL	Input Low Voltage		-0.5		0.3VCC	0.3VCC	V
VIH	Input High Voltage		0.7VCC		VCC+0.4	VCC+0.4	V
VOL	Output Low Voltage	IOL=100uA			0.2	0.2	V
VOH	Output High Voltage	IOH=-100uA	VCC-0.2				V

Note:

1. Typical values given for TA=25 ℃, VCC=1.8V.
2. Value guaranteed by design and/or characterization, not 100% tested in production.

8.6. AC Characteristics

(TA= -40 ℃~85 ℃, VCC=1.7~2.0V)

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
fC1(2)	Serial Clock Frequency For: all commands except DTR & Read (03H)			104	MHz
fC2(2)	Serial Clock Frequency For DTR			80	MHz
fR	Serial Clock Frequency For: Read (03H)			60	MHz
tCLH(3)	Serial Clock High Time	45% PC			ns
tCLL(3)	Serial Clock Low Time	45% PC			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	3			ns
tSHCH	CS# Not Active Setup Time	4			ns
tCHSL	CS# Not Active Hold Time	3			ns
tSHSL	CS# High Time (From Read to next Read)	40			ns
	CS# High Time (From Write/Erase/Program to Read Status Register)	40			ns
tSHQZ	Output Disable Time			12	ns
tECSV	ECS# Setup Time			10	ns
tCLQX	Output Hold Time	1.4			ns
tCLQV	Clock Low To Output Valid			6	ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5			ns
tHHCH	Hold# High Setup Time (relative to Clock)	5			ns
tCHHL	Hold# High Hold Time (relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			10	ns
tHHQX	Hold# High To Low-Z Output			10	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			15	µs
tRES1	CS# High To Standby Mode Without Electronic Signature Read			50	µs
tRES2	CS# High To Standby Mode With Electronic Signature Read			50	µs
tRST_R	CS# High To Next Command After Reset (from read)			50	µs
tRST_P	CS# High To Next Command After Reset (from program)			50	µs
tRST_E	CS# High To Next Command After Reset (from erase)			25	ms
tSUS1	CS# High To Next Command After Erase Suspend			50	µs
tSUS2	CS# High To Next Command After Program Suspend			50	µs
tRS	Latency Between Resume And Next Suspend	200			µs
tW	Write Status Register Cycle Time		1	10	ms
tBP	Byte Program Time (First Byte)		58	124	µs
tBP	Additional Byte Program Time (After First Byte)		3	9	µs
tPP	Page Program Time		0.4	2	ms
tSE	Sector Erase Time		45	2000	ms
tBE1	Block Erase Time (32K Bytes)		0.15	3.5	s

tBE2	Block Erase Time (64K Bytes)		0.3	5	s
tCE	Chip Erase Time		240	500	s

(TA= -40 ℃~105 ℃, VCC=1.7~2.0V)

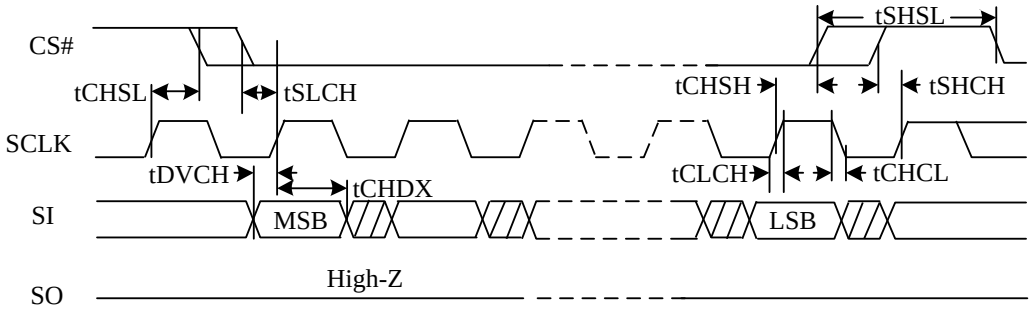
Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
fC1(2)	Serial Clock Frequency For: all commands except DTR & Read (03H)			104	MHz
fC2(2)	Serial Clock Frequency For DTR			80	MHz
fR	Serial Clock Frequency For: Read (03H)			60	MHz
tCLH(3)	Serial Clock High Time	45% PC			ns
tCLL(3)	Serial Clock Low Time	45% PC			ns
tCLCH	Serial Clock Rise Time (Slew Rate)	0.2			V/ns
tCHCL	Serial Clock Fall Time (Slew Rate)	0.2			V/ns
tSLCH	CS# Active Setup Time	5			ns
tCHSH	CS# Active Hold Time	3			ns
tSHCH	CS# Not Active Setup Time	4			ns
tCHSL	CS# Not Active Hold Time	3			ns
tSHSL	CS# High Time (From Read to next Read)	40			ns
	CS# High Time (From Write/Erase/Program to Read Status Register)	40			ns
tSHQZ	Output Disable Time			12	ns
tECSV	ECS# Setup Time			10	ns
tCLQX	Output Hold Time	1.4			ns
tCLQV	Clock Low To Output Valid			6	ns
tDVCH	Data In Setup Time	2			ns
tCHDX	Data In Hold Time	2			ns
tHLCH	Hold# Low Setup Time (relative to Clock)	5			ns
tHHCH	Hold# High Setup Time (relative to Clock)	5			ns
tCHHL	Hold# High Hold Time (relative to Clock)	5			ns
tCHHH	Hold# Low Hold Time (relative to Clock)	5			ns
tHLQZ	Hold# Low To High-Z Output			10	ns
tHHQX	Hold# High To Low-Z Output			10	ns
tWHSL	Write Protect Setup Time Before CS# Low	20			ns
tSHWL	Write Protect Hold Time After CS# High	100			ns
tDP	CS# High To Deep Power-Down Mode			15	µs
tRES1	CS# High To Standby Mode Without Electronic Signature Read			60	µs
tRES2	CS# High To Standby Mode With Electronic Signature Read			60	µs
tRST_R	CS# High To Next Command After Reset (from read)			60	µs
tRST_P	CS# High To Next Command After Reset (from program)			60	µs
tRST_E	CS# High To Next Command After Reset (from erase)			25	ms
tSUS1	CS# High To Next Command After Erase Suspend			60	µs
tSUS2	CS# High To Next Command After Program Suspend			60	µs
tRS	Latency Between Resume And Next Suspend	200			µs
tW	Write Status Register Cycle Time		1	10	ms
tBP	Byte Program Time (First Byte)		58	124	µs
tBP	Additional Byte Program Time (After First Byte)		3	9	µs
tPP	Page Program Time		0.4	3	ms
tSE	Sector Erase Time		45	2000	ms

tBE1	Block Erase Time (32K Bytes)		0.15	3.5	s
tBE2	Block Erase Time (64K Bytes)		0.3	5	s
tCE	Chip Erase Time		240	500	s

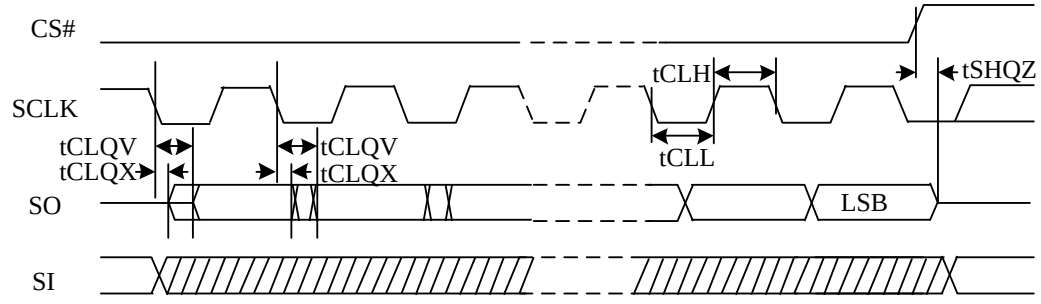
Note:

1. Typical values given for TA=25℃, VCC = 1.8V.
2. For specific speeds of different read commands, please refer to *7.1 Clock Frequencies.*
3. Clock high or Clock low must be more than or equal to 45%PC. PC=1/fC (MAX).
4. Value guaranteed by design and/or characterization, not 100% tested in production.

Serial Input Timing

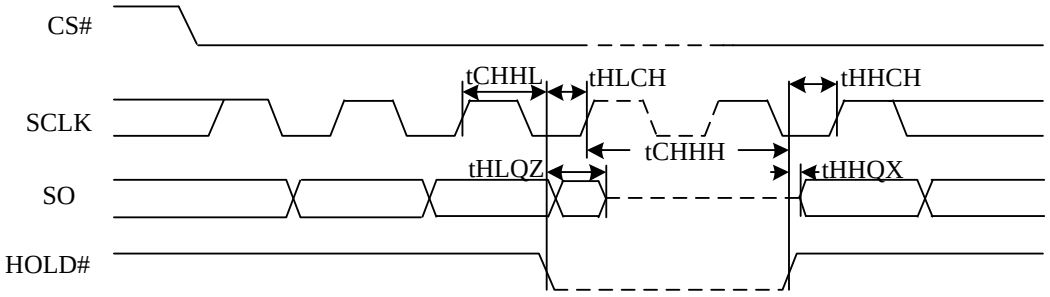


Output Timing



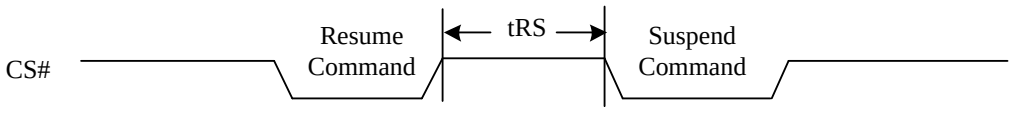
Least significant address bit (LSB) in

Hold Timing



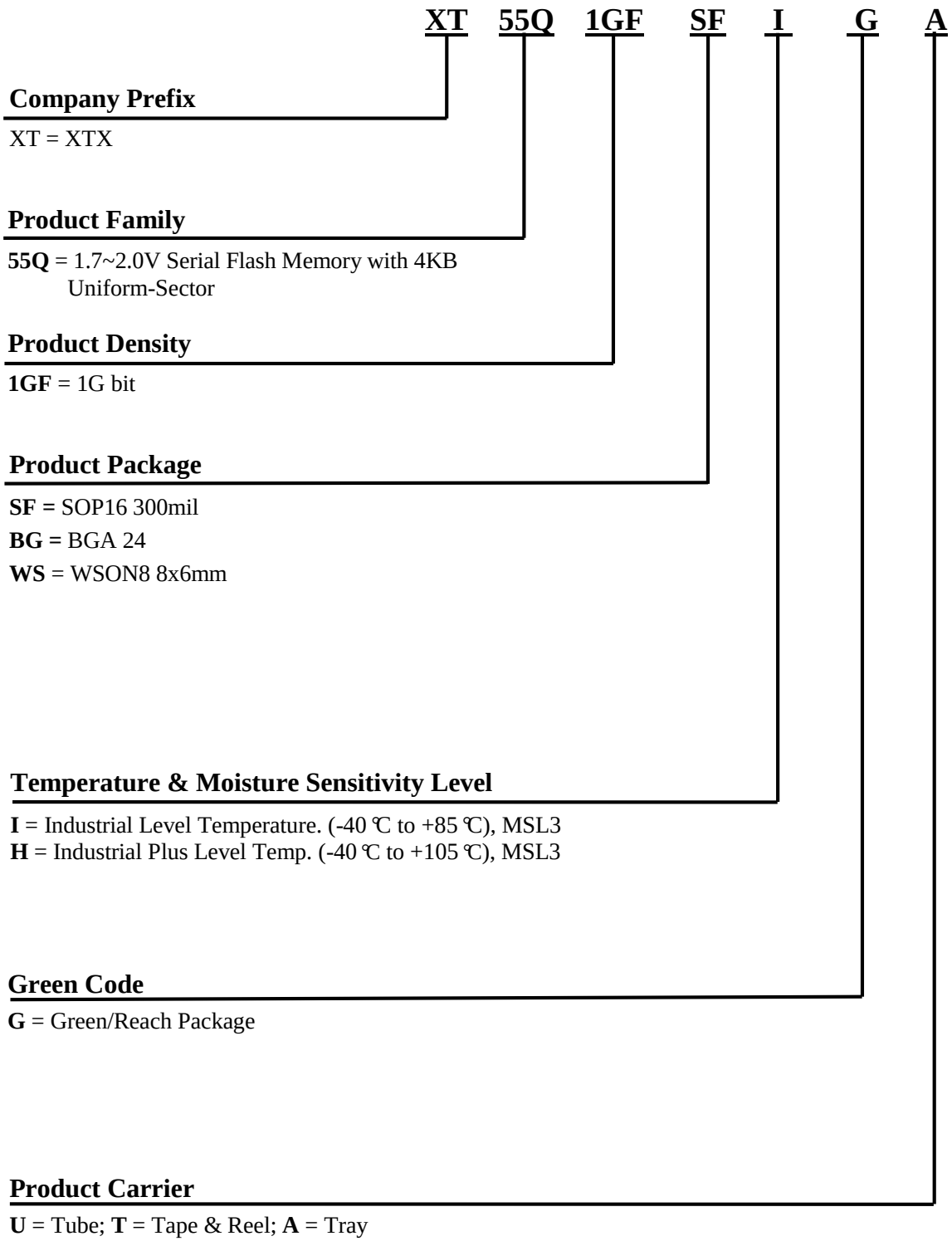
SI do not care during HOLD operation

Resume to Suspend Timing Diagram



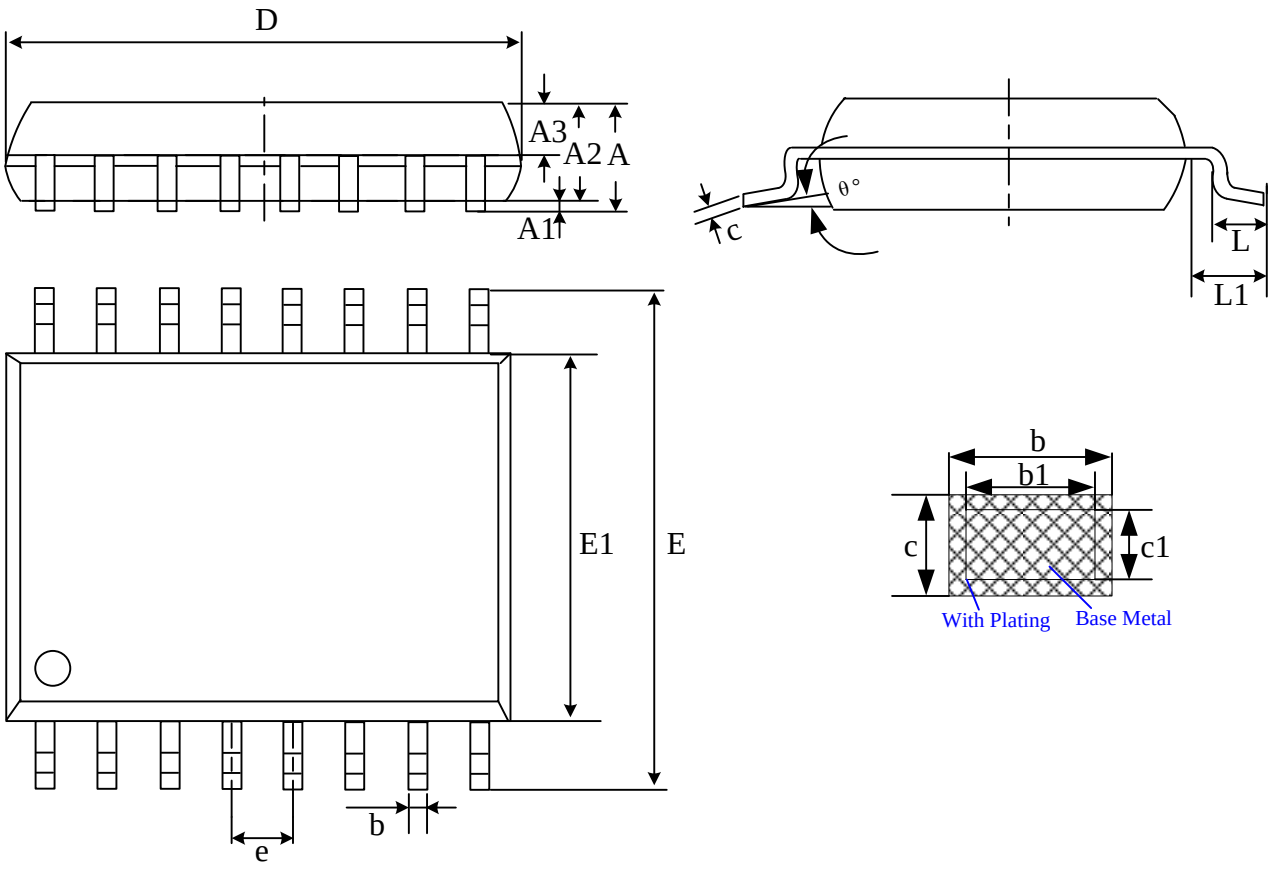
9. ORDERING INFORMATION

The ordering part number is formed by a valid combination of the following



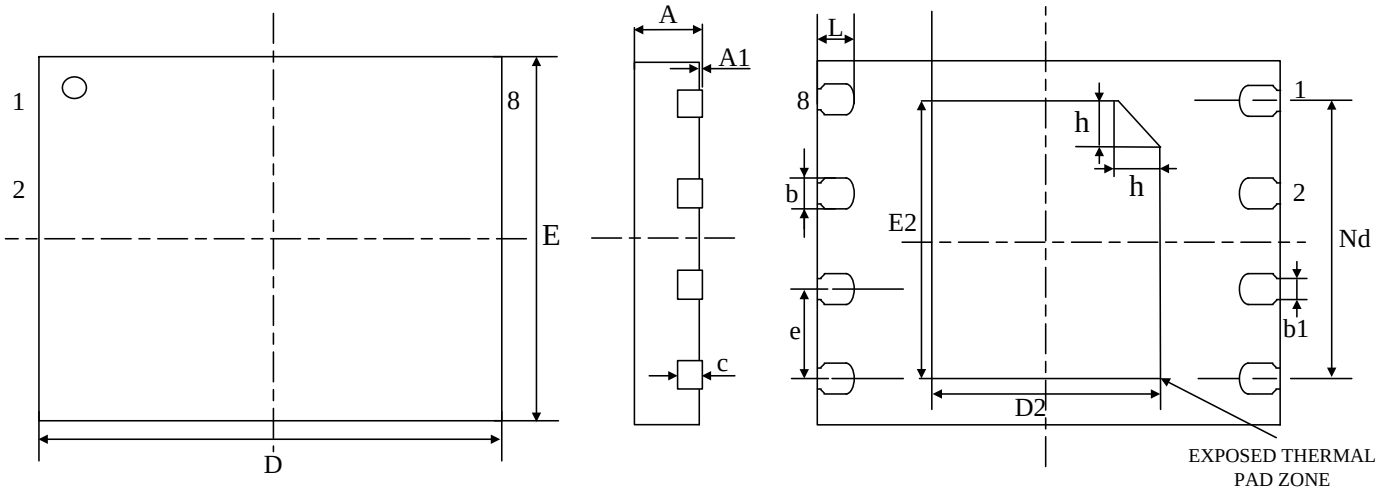
10. PACKAGE INFORMATION

10.1. Package SOP16 300mil

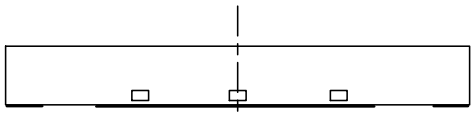


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	—	0.43
b1	0.34	0.37	0.40
c	0.25	—	0.29
c1	0.24	0.25	0.26
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27 BSC		
L	0.55	—	0.85
L1	1.40 REF		
θ	0 °	—	8 °

10.2. Package WSON8 8x6mm



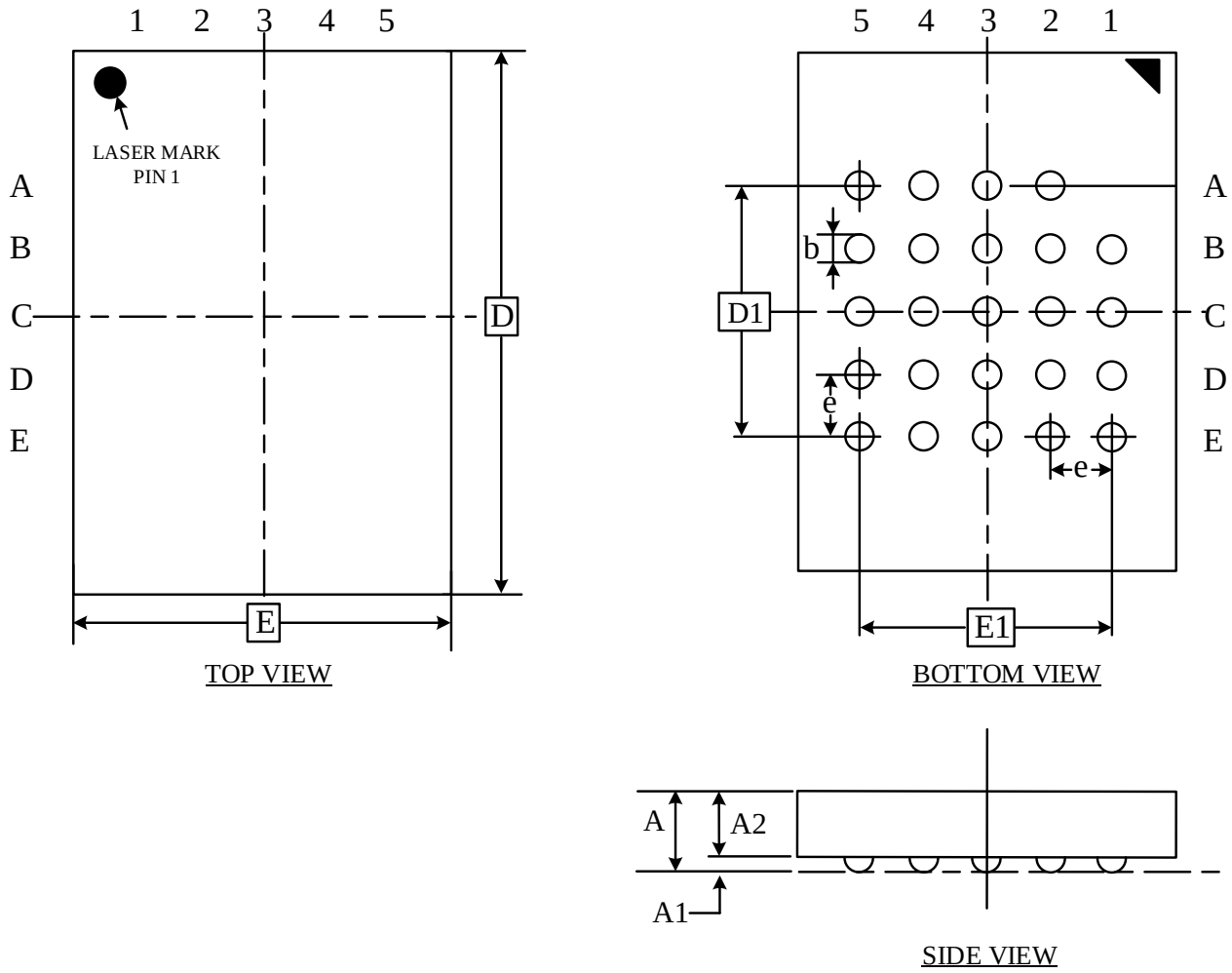
TOP VIEW **SIDE VIEW** **BOTTOM VIEW**



SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.35	0.40	0.45
b1		0.25REF	
c	0.18	0.20	0.25
D	7.90	8.00	8.10
Nd		3.81BSC	
e		1.27BSC	
E	5.90	6.00	6.10
D2	3.30	3.40	3.50
E2	4.20	4.30	4.40
L	0.45	0.50	0.55
h	0.30	0.35	0.40

10.3. Package BGA 24 ball (5x5)



Symbol / Unit		A	A1	A2	b	E	E1	D	D1	e
mm	Min.	-	0.25	0.75	0.35	5.90	4.00	7.90	4.00	1.00
	Nom.	-	0.30	0.80	0.40	6.00		8.00		
	Max.	1.20	0.35	0.85	0.45	6.10		8.10		

11. REVISION HISTORY

Revision	Description	Date
1.0	Initial version	Aug 18, 2023
1.1	Adjust the ECC status bit to the factory fixed value of 1 Optimize tSE max from 2500ms to 2000ms Optimize tBE32K max from 4s to 3.5s Optimize tBE64K max from 6s to 5s Add OPN XT55Q1GFBGIGA/XT55Q1GFBGHGA/XT55Q1GFWSIGA/XT55Q1GFWSHGA Add WSON8 8x6mm and BGA24 packages	Jul 25, 2024