National Semiconductor

# 54F/74F403A
# First-In First-Out (FIFO) Buffer Memory

## General Description

The 'F403A is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high-speed disk or tape controllers and communication buffer applications. It is organized as 16-words by 4-bits and may be expanded to any number of words or any number of bits in multiples of four. Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 'F403A has TRI-STATE® outputs which provide added versatility and is fully compatible with all TTL families.

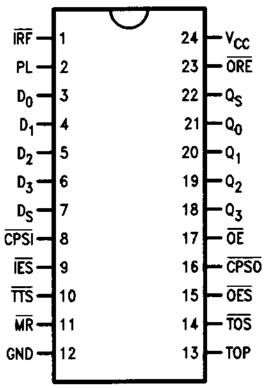
## Features

- Serial or parallel input
- Serial or parallel output
- Expandable without external logic
- TRI-STATE outputs
- Fully compatible with all TTL families
- Slim 24-pin package
- 9403A replacement
- Guaranteed 4000V minimum ESD protection

## Ordering Code: See Section 5

## Connection Diagrams

**Pin Assignment for DIP and SOIC**

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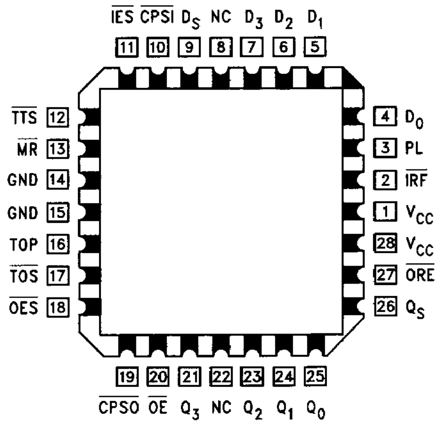
**Pin Assignment for PCC**

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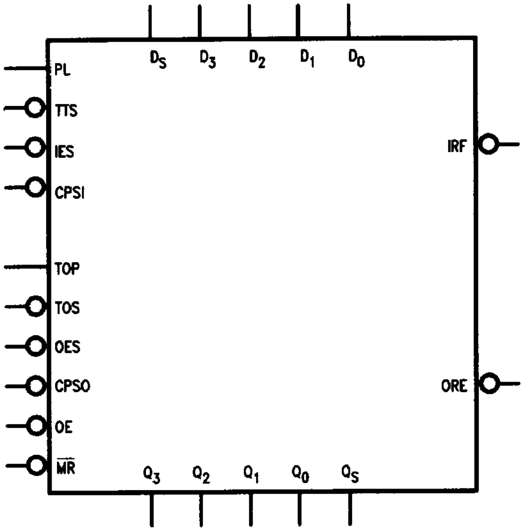
## Logic Symbol

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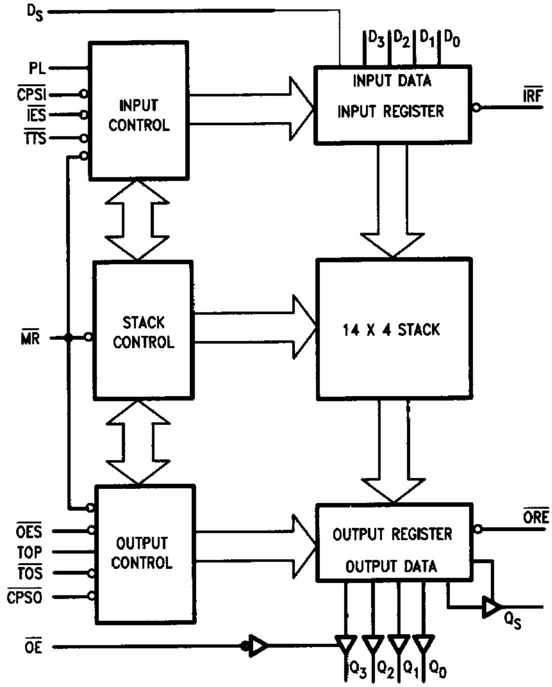
## Unit Loading/Fan Out: See Section 2 for U.L. definitions

| Pin Names | Description | 54F/74F U.L. HIGH/LOW | 54F/74F Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$ |
|---|---|---|---|
| $D_0$–$D_3$ | Parallel Data Inputs | 1.0/0.667 | 20 μA/400 μA |
| $D_S$ | Serial Data Input | 1.0/0.667 | 20 μA/400 μA |
| PL | Parallel Load Input | 1.0/0.667 | 20 μA/400 μA |
| $\overline{CPSI}$ | Serial Input Clock | 1.0/0.667 | 20 μA/400 μA |
| $\overline{IES}$ | Serial Input Enable | 1.0/0.667 | 20 μA/400 μA |
| $\overline{TTS}$ | Transfer to Stack Input | 1.0/0.667 | 20 μA/400 μA |
| $\overline{OES}$ | Serial Output Enable | 1.0/0.667 | 20 μA/400 μA |
| $\overline{TOS}$ | Transfer Out Serial | 1.0/0.667 | 20 μA/400 μA |
| TOP | Transfer Out Parallel | 1.0/0.667 | 20 μA/400 μA |
| $\overline{MR}$ | Master Reset | 1.0/0.667 | 20 μA/400 μA |
| $\overline{OE}$ | Output Enable | 1.0/0.667 | 20 μA/400 μA |
| $\overline{CPSO}$ | Serial Output Clock | 1.0/0.667 | 20 μA/400 μA |
| $Q_0$–$Q_3$ | Parallel Data Outputs | 285/26.7 | 5.7 mA/16 mA |
| $Q_S$ | Serial Data Output | 285/26.7 | 5.7 mA/16 mA |
| $\overline{IRF}$ | Input Register Full | 20/13.3 | −400 μA/8 mA |
| $\overline{ORE}$ | Output Register Empty | 20/13.3 | −400 μA/8 mA |

## Block Diagram

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## Functional Description

As shown in the block diagram the 'F403A consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14-word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below.

**INPUT REGISTER (DATA ENTRY)**

The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

*Figure 1* is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the $F_3$ flip-flop and resetting the other flip-flops. The $\overline{Q}$ output of the last flip-flop (FC) is brought out as the 'Input Register Full' output ($\overline{IRF}$). After initialization this output is HIGH.

**Parallel Entry**—A HIGH on the PL input loads the $D_0$–$D_3$ inputs into the $F_0$–$F_3$ flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section).

**Serial Entry**—Data on the $D_S$ input is serially entered into the $F_3$, $F_2$, $F_1$, $F_0$, FC shift register on each HIGH-to-LOW transition of the $\overline{CPSI}$ clock input, provided $\overline{IES}$ and PL are LOW.

After the fourth clock transition, the four data bits are located in the four flip-flops, $F_0$–$F_3$. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from affecting the register, *Figure 2* illustrates the final positions in a 'F403A resulting from a 64-bit serial bit train. $B_0$ is the first bit, $B_{63}$ the last bit.

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## Functional Description (Continued)

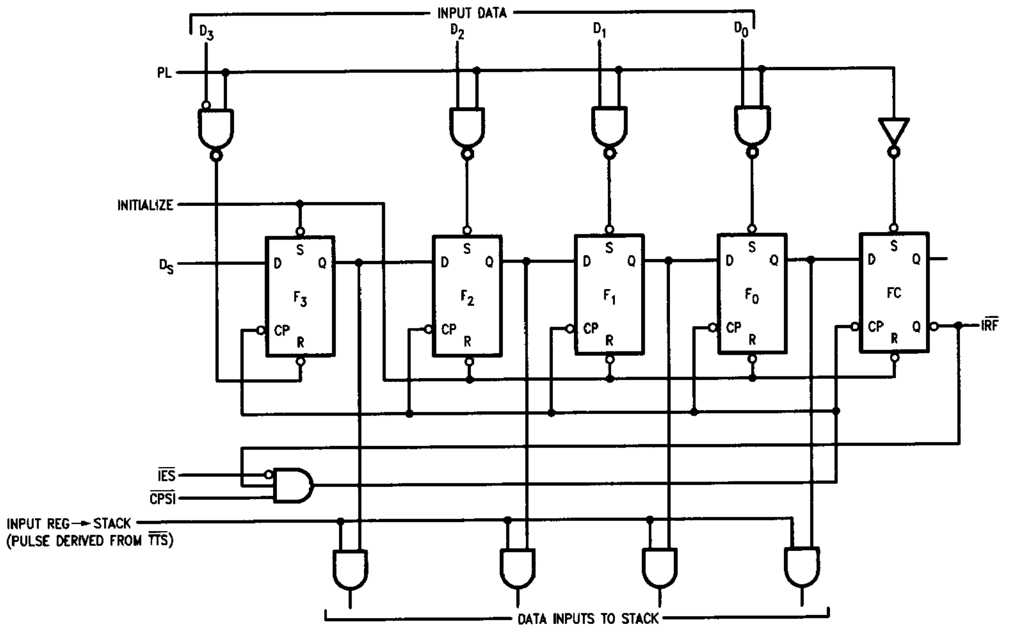


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**FIGURE 1. Conceptual Input Section**

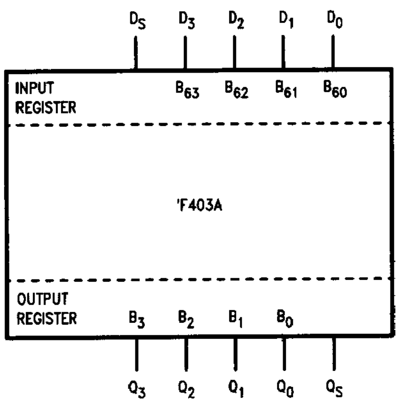


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**FIGURE 2. Final Positions in a 'F403A Resulting from a 64-Bit Serial Train**

**Transfer to the Stack**—The outputs of Flip-Flops $F_0$–$F_3$ feed the stack. A LOW level on the $\overline{TTS}$ input initiates a 'fall-through' action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 10*) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 'F403A as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

### OUTPUT REGISTER (DATA EXTRACTION)

The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a TRI-STATE 4-bit parallel data bus or on a TRI-STATE serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

## Functional Description (Continued)

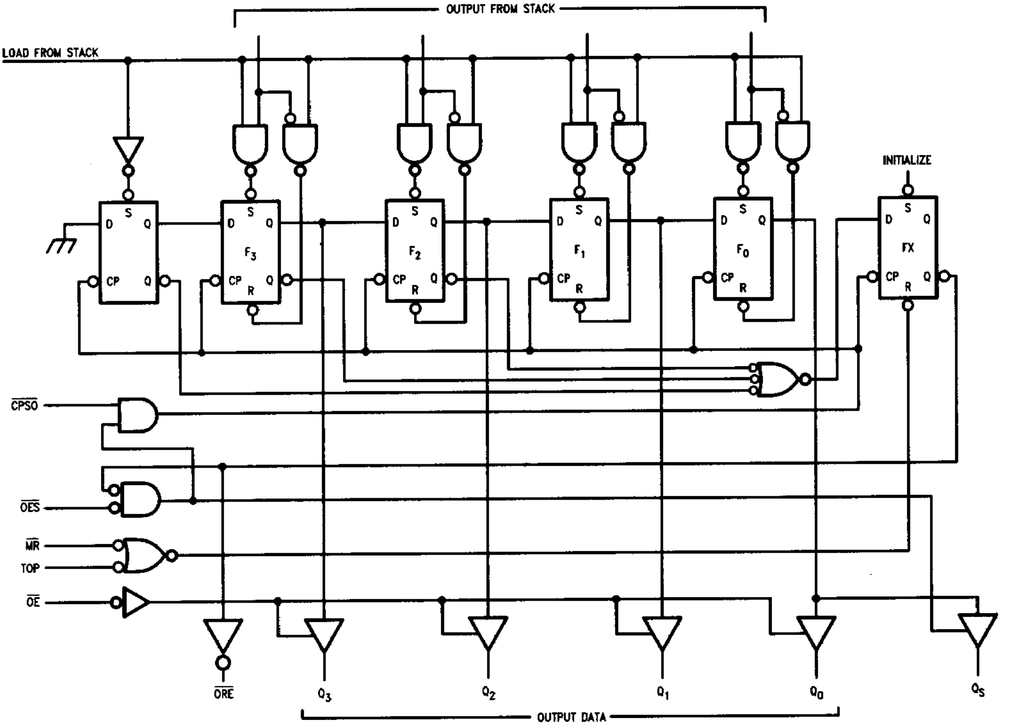


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**FIGURE 3. Conceptual Output Section**

**Parallel Data Extraction**—When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the 'Transfer Out Parallel' (TOP) input is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH, indicating valid data on the data outputs (provided the TRI-STATE buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{\text{ORE}}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{\text{CPSO}}$ should be LOW. TOS should be grounded for single slice operation or connected to the appropriate $\overline{\text{ORE}}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, $\overline{\text{ORE}}$ remains LOW indicating that there is no valid data at the outputs.

**Serial Data Extraction**—When the FIFO is empty after a LOW pulse is applied to $\overline{\text{MR}}$, the Output Register Empty ($\overline{\text{ORE}}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{\text{TOS}}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{\text{ORE}}$ goes HIGH indicating valid data in the register. The TRI-STATE Serial Data Output, $Q_S$, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{\text{CPSO}}$. To prevent false shifting, $\overline{\text{CPSO}}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{\text{ORE}}$ output LOW and disables the serial output, $Q_S$ (refer to *Figure 3*). For serial operation the $\overline{\text{ORE}}$ output may be tied to the $\overline{\text{TOS}}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

## Functional Description (Continued)

**EXPANSION**

**Vertical Expansion**—The 'F403A may be vertically expanded to store more words without external parts. The interconnection is necessary to form a 46-word by 4-bit FIFO are shown in *Figure 4*. Using the same technique, and FIFO of (15n + 1)-words by 4-bits can be constructed, where n is the number of devices. Note that expansion does not sacrifice any of the 'F403A's flexibility for serial/parallel input and output.

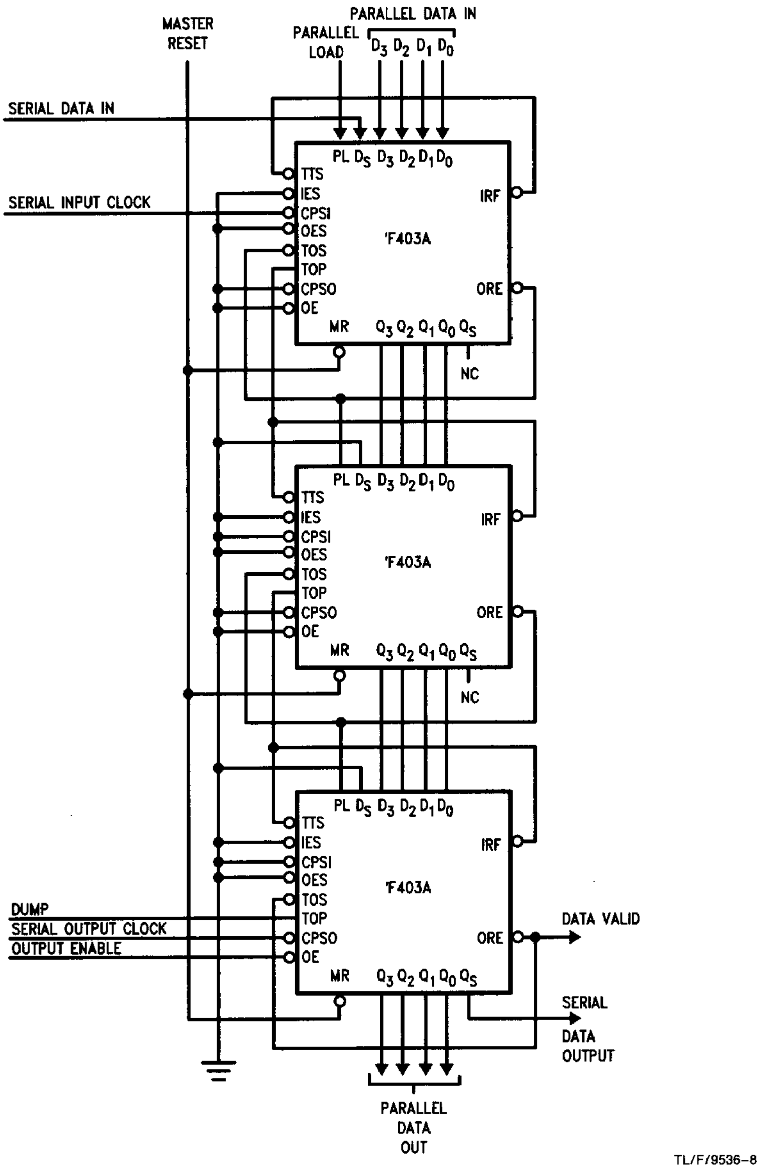


**FIGURE 4. A Vertical Expansion Scheme**

# Functional Description (Continued)

**Horizontal and Vertical Expansion**—The 'F403A can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 6*. Using the same technique, any FIFO of (15m + 1)-words by (4n)-bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row. *Figures 7* and *8* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 6*. The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 6* is shown in *Figure 9*.

**Interlocking Circuitry**—Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 'F403A incorporates simple but effective 'master/slave' interlocking circuitry to eliminate the need for external gating.

In the 'F403A array of *Figure 6* devices 1 and 5 are defined as 'row masters' and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes HIGH and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 'F403A FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. *Figure 10* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the $\overline{ORE}$ Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

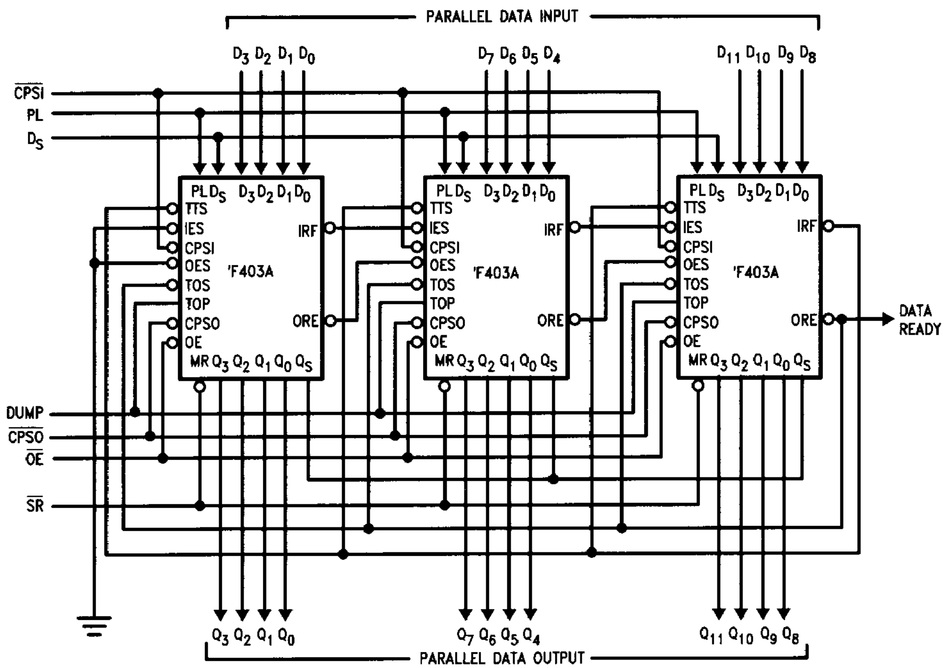


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**FIGURE 5. A Horizontal Expansion Scheme**

## Functional Description (Continued)

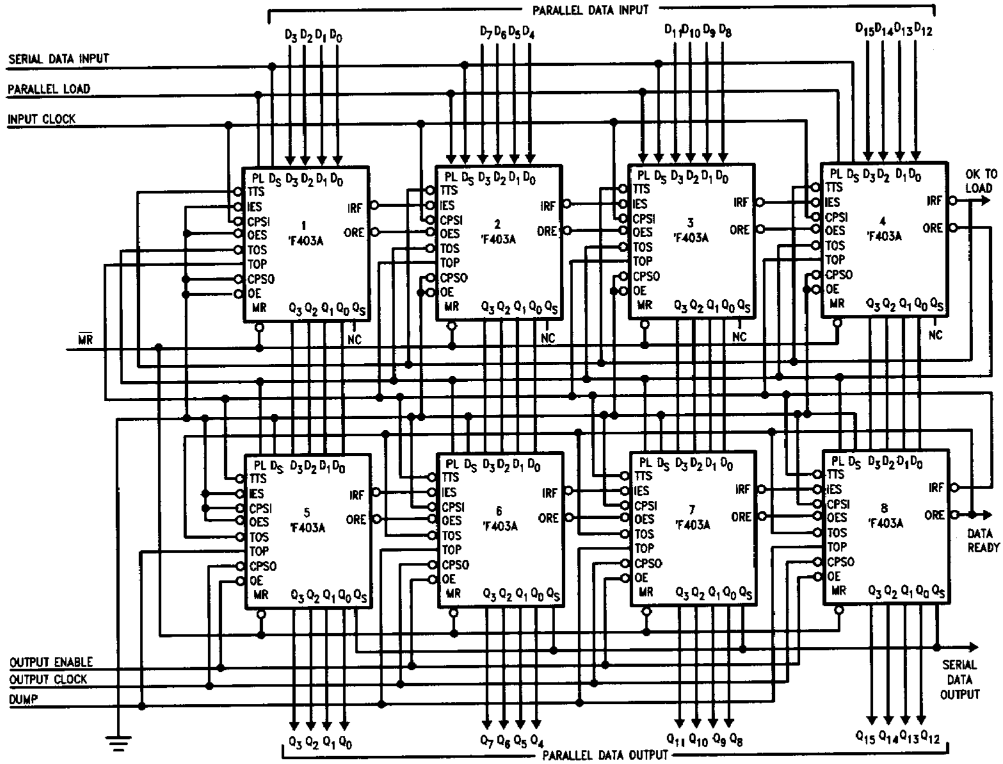


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**FIGURE 6. A 31 x 16 FIFO Array**

## Functional Description (Continued)

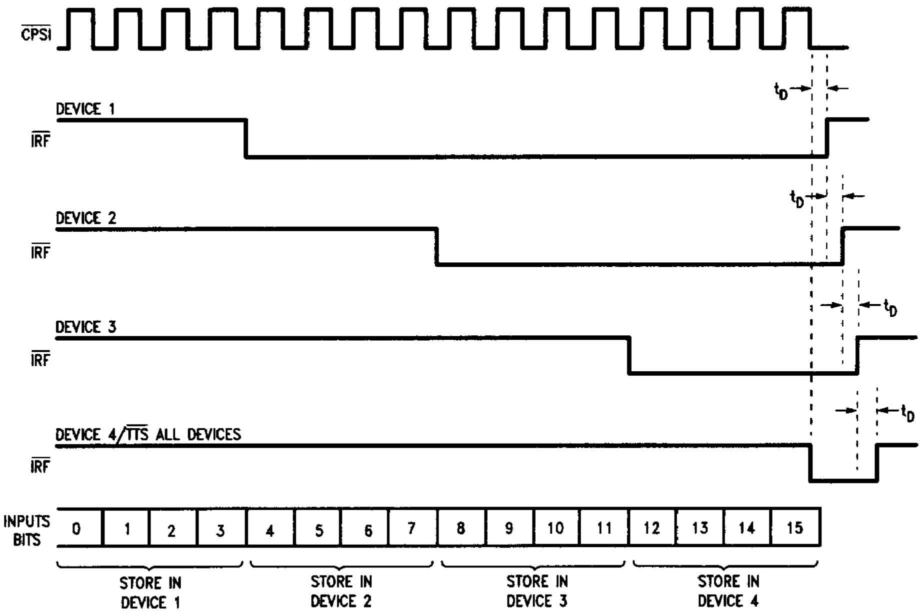


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**FIGURE 7. Serial Data Entry for Array of *Figure 6***

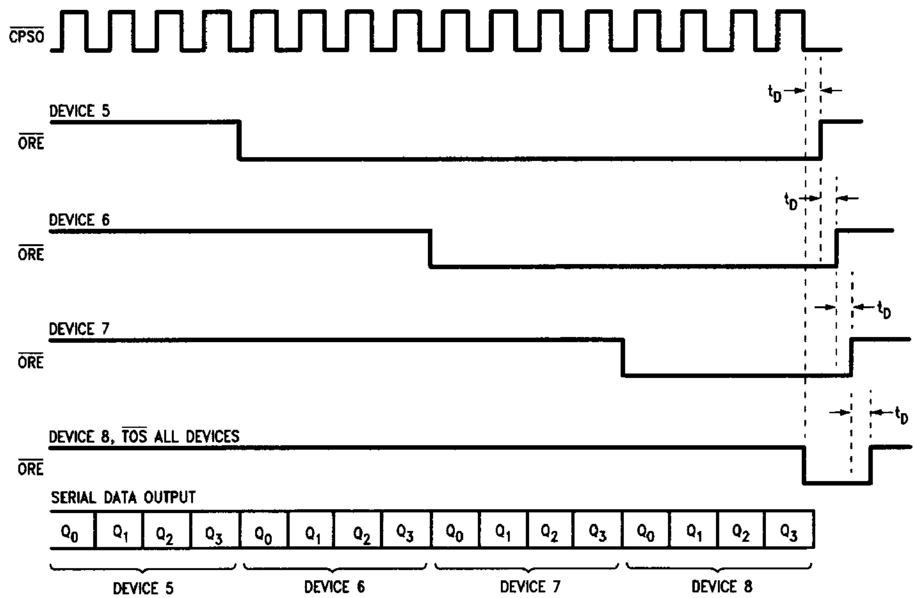


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**FIGURE 8. Serial Data Extraction for Array of *Figure 6***

## Functional Description (Continued)

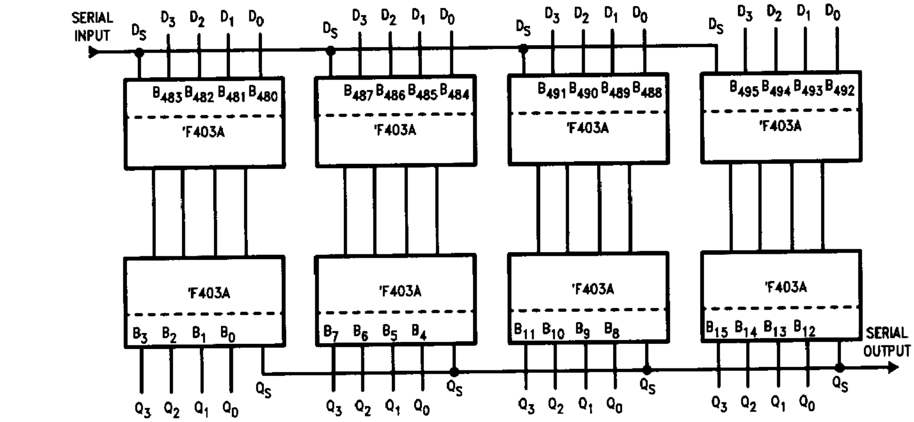


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**FIGURE 9. Final Position of a 496-Bit Serial Input**

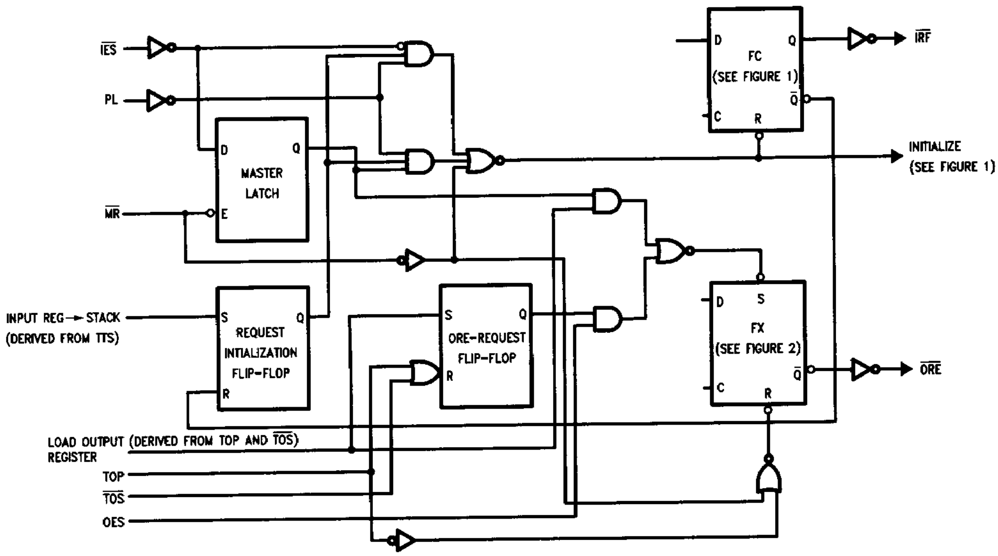


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**FIGURE 10. Conceptual Diagram, Interlocking Circuitry**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Storage Temperature | −65°C to +150°C |
| Ambient Temperature under Bias | −55°C to +125°C |
| Junction Temperature under Bias | −55°C to +175°C |
| $V_{CC}$ Pin Potential to Ground Pin | −0.5V to +7.0V |
| Input Voltage (Note 2) | −0.5V to +7.0V |
| Input Current (Note 2) | −30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with $V_{CC}$ = 0V) | |
| Standard Output | −0.5V to $V_{CC}$ |
| TRI-STATE Output | −0.5V to +5.5V |
| Current Applied to Output in LOW State (Max) | twice the rated $I_{OL}$ (mA) |
| ESD Last Passing Voltage (Min) | 4000V |

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

| | |
|---|---|
| Free Air Ambient Temperature | |
| Military | −55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

## DC Electrical Characteristics

| Symbol | Parameter | | 54F/74F Min | Typ | Max | Units | $V_{CC}$ | Conditions |
|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | | Recognized as a HIGH Signal |
| $V_{IL}$ | Input LOW Voltage | | | | 0.8 | V | | Recognized as a LOW Signal |
| $V_{CD}$ | Input Clamp Diode Voltage | | | | −1.5 | V | Min | $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 54F 10% $V_{CC}$ | 2.4 | | | V | Min | $I_{OH}$ = −400 μA ($\overline{IRF}$, $\overline{ORE}$) |
| | | 54F 10% $V_{CC}$ | 2.4 | | | | | $I_{OH}$ = −2.0 mA ($Q_n$, $Q_s$) |
| | | 74F 10% $V_{CC}$ | 2.5 | | | | | $I_{OH}$ = −400 μA ($\overline{IRF}$, $\overline{ORE}$) |
| | | 74F 10% $V_{CC}$ | 2.5 | | | | | $I_{OH}$ = −5.7 mA ($Q_n$, $Q_s$) |
| | | 74F 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −400 μA ($\overline{IRF}$, $\overline{ORE}$) |
| | | 74F 5% $V_{CC}$ | 2.7 | | | | | $I_{OH}$ = −5.7 mA ($Q_n$, $Q_s$) |
| $V_{OL}$ | Output LOW Voltage | 54F 10% $V_{CC}$ | | | 0.4 | V | Min | $I_{OL}$ = 4 mA ($\overline{IRF}$, $\overline{ORE}$) |
| | | 54F 10% $V_{CC}$ | | | 0.4 | | | $I_{OL}$ = 8 mA ($Q_n$, $Q_s$) |
| | | 74F 10% $V_{CC}$ | | | 0.5 | | | $I_{OL}$ = 8 mA ($\overline{IRF}$, $\overline{ORE}$) |
| | | 74F 10% $V_{CC}$ | | | 0.5 | | | $I_{OL}$ = 16 mA ($Q_n$, $Q_s$) |
| $I_{IH}$ | Input HIGH Current | | | | 20 | μA | Max | $V_{IN}$ = 2.7V |
| $I_{BVI}$ | Input HIGH Current Breakdown Test | | | | 100 | μA | Max | $V_{IN}$ = 7.0V |
| $I_{IL}$ | Input LOW Current | | | | −0.4 | mA | Max | $V_{IN}$ = 0.5V |
| $I_{OZH}$ | Output Leakage Current | | | | 50 | μA | Max | $V_{OUT}$ = 2.7V |
| $I_{OZL}$ | Output Leakage Current | | | | −50 | μA | Max | $V_{OUT}$ = 0.5V |
| $I_{OS}$ | Output Short-Circuit Current | | −20 | | −130 | mA | Max | $V_{OUT}$ = 0V |
| $I_{CEX}$ | Output HIGH Leakage Current | | | | 250 | μA | Max | $V_{OUT}$ = $V_{CC}$ |
| $I_{CCL}$ | Power Supply Current | | | | 170 | mA | Max | $V_O$ = LOW |

## AC Electrical Characteristics

| Symbol | Parameter | 74F $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF | | 54F $T_A, V_{CC}$ = Mil $C_L = 50$ pF | | 74F $T_A, V_{CC}$ = Com $C_L = 50$ pF | | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $t_{PHL}$ | Propagation Delay, Negative-Going $\overline{CPSI}$ to $\overline{IRF}$ Output | 7.5 | 14.0 | | | 7.0 | 15.0 | ns | *403-a, b* |
| $t_{PLH}$ | Propagation Delay, Negative-Going $\overline{TTS}$ to $\overline{IRF}$ | 11.0 | 20.5 | | | 10.0 | 22.5 | | |
| $t_{PLH}$ <br> $t_{PHL}$ | Propagation Delay, Negative-Going $\overline{CPSO}$ to $Q_S$ Output | 8.5 <br> 8.0 | 17.0 <br> 14.5 | | | 7.5 <br> 7.0 | 18.5 <br> 15.5 | ns | *403-c, d* |
| $t_{PLH}$ <br> $t_{PHL}$ | Propagation Delay, Positive-Going TOP to Outputs $Q_0$–$Q_3$ | 10.0 <br> 8.5 | 18.0 <br> 15.5 | | | 9.0 <br> 8.0 | 20.0 <br> 16.5 | ns | 403-e |
| $t_{PHL}$ | Propagation Delay, Negative-Going $\overline{CPSO}$ to $\overline{ORE}$ | 9.5 | 17.5 | | | 9.0 | 19.0 | ns | *403-c, d* |
| $t_{PHL}$ | Propagation Delay, Negative-Going TOP to $\overline{ORE}$ | 8.0 | 15.0 | | | 7.5 | 16.5 | ns | *403-e* |
| $t_{PLH}$ | Propagation Delay, Positive-Going TOP to $\overline{ORE}$ | 12.5 | 22.0 | | | 11.5 | 25.0 | | |
| $t_{PLH}$ | Propagation Delay, Negative-Going $\overline{TOS}$ to Positive Going $\overline{ORE}$ | 12.5 | 22.0 | | | 11.0 | 25.0 | ns | *403-c, d* |
| $t_{PHL}$ | Propagation Delay, Positive-Going PL to Negative-Going $\overline{IRF}$ | 7.0 | 13.0 | | | 6.5 | 14.0 | ns | *403-g, h* |
| $t_{PLH}$ | Propagation Delay, Negative-Going PL to Positive-Going $\overline{IRF}$ | 9.5 | 17.0 | | | 8.5 | 19.5 | | |

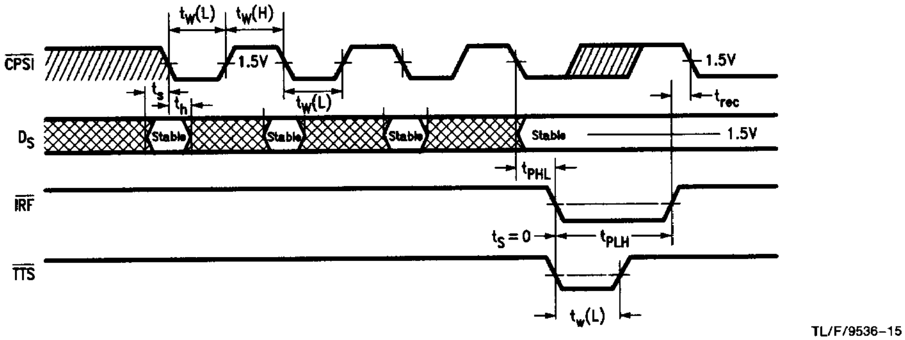
## AC Electrical Characteristics (Continued)

| Symbol | Parameter | 74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF Min | 74F Max | 54F $T_A, V_{CC}$ = Mil, $C_L = 50$ pF Min | 54F Max | 74F $T_A, V_{CC}$ = Com, $C_L = 50$ pF Min | 74F Max | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation Delay, Positive-Going $\overline{OES}$ to $\overline{ORE}$ | 10.0 | 18.0 | | | 9.0 | 20.5 | ns | |
| $t_{PLH}$ | Propagation Delay, Positive-Going $\overline{IES}$ to Positive-Going $\overline{IRF}$ | 8.5 | 15.5 | | | 7.5 | 17.5 | ns | *403-h* |
| $t_{PLH}$ | Propagation Delay, $\overline{MR}$ to $\overline{IRF}$ | 8.0 | 15.0 | | | 7.5 | 17.0 | ns | |
| $t_{PHL}$ | Propagation Delay, $\overline{MR}$ to $\overline{ORE}$ | 9.0 | 16.0 | | | 8.0 | 17.5 | ns | |
| $t_{PZH}$<br>$t_{PZL}$ | Propagation Delay, $\overline{OE}$ to $Q_0, Q_1, Q_2, Q_3$ | 2.5<br>2.5 | 6.5<br>7.5 | | | 2.0<br>2.0 | 8.0<br>8.5 | ns | |
| $t_{PHZ}$<br>$t_{PLZ}$ | Propagation Delay, $\overline{OE}$ to $Q_0, Q_1, Q_2, Q_3$ | 2.5<br>2.5 | 6.5<br>7.5 | | | 2.0<br>2.0 | 8.0<br>8.0 | ns | |
| $t_{PZH}$<br>$t_{PZL}$ | Propagation Delay, Negative-Going $\overline{OES}$ to $Q_S$ | 5.5<br>5.5 | 12.0<br>14.0 | | | 5.0<br>5.0 | 15.0<br>15.0 | ns | |
| $t_{PHZ}$<br>$t_{PLZ}$ | Propagation Delay, Negative-Going $\overline{OES}$ to $Q_S$ | 5.5<br>5.5 | 12.0<br>14.5 | | | 5.0<br>5.0 | 14.0<br>16.0 | ns | |
| $t_{PZH}$<br>$t_{PZL}$ | Turn On Time $\overline{TOS}$ to $Q_S$ | 8.5<br>8.5 | 21.0<br>20.0 | | | 8.0<br>8.0 | 24.0<br>21.0 | ns | |
| $t_{DFT}$ | Fall Through Time | 45.0 | 80.0 | | | 35.0 | 95.0 | ns | *403-f* |
| $t_{AP}$ | Parallel Appearance Time, $\overline{ORE}$ to $Q_0 - Q_3$ | −10.0 | −1.0 | | | −10.0 | −1.0 | ns | |
| $t_{AS}$ | Serial Appearance Time, $\overline{ORE}$ to $Q_S$ | −10.0 | 2.0 | | | −10.0 | 2.0 | ns | |

## AC Operating Requirements

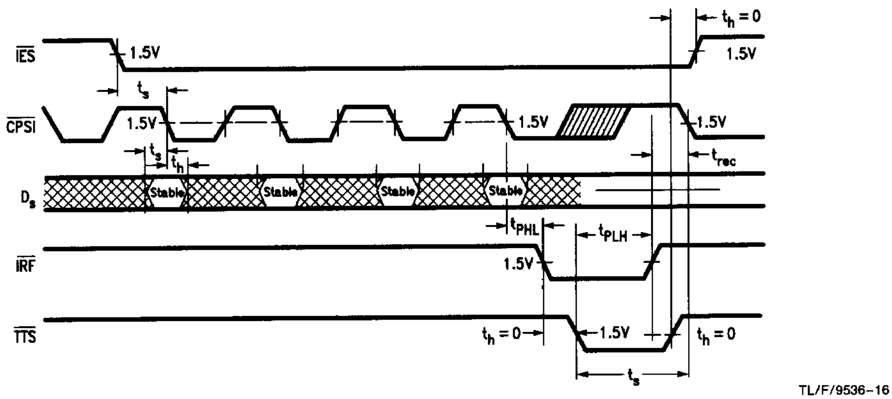
| Symbol | Parameter | 74F $T_A = +25°C$ $V_{CC} = +5.0V$ Min | Max | 54F $T_A, V_{CC}$ = Mil Min | Max | 74F $T_A, V_{CC}$ = Com Min | Max | Units | Fig. No. |
|---|---|---|---|---|---|---|---|---|---|
| $t_s(H)$<br>$t_s(L)$ | Set-up Time HIGH or LOW<br>$D_S$ to Negative $\overline{CPSI}$ | 1.0<br>1.0 | | | | 1.0<br>1.0 | | ns | *403-a, b* |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH or LOW<br>$D_S$ to $\overline{CPSI}$ | 3.5<br>3.5 | | | | 3.5<br>3.5 | | | |
| $t_s(L)$ | Set-up Time, LOW<br>$\overline{TTS}$ to $\overline{IRF}$<br>Serial or Parallel Mode | 0 | | | | 0 | | ns | 403-a, b, *g, h* |
| $t_s(L)$ | Set-up Time, LOW<br>Negative-Going $\overline{ORE}$ to<br>Negative-Going $\overline{TOS}$ | 0 | | | | 0 | | ns | *403-c, d* |
| $t_s(L)$ | Set-up Time, LOW<br>Negative-Going $\overline{IES}$ to $\overline{CPSI}$ | 3.0 | | | | 4.0 | | ns | *403-b* |
| $t_s(L)$ | Set-up Time, LOW<br>Negative-Going $\overline{TTS}$ to $\overline{CPSI}$ | 14.0 | | | | 15.5 | | ns | *403-b* |
| $t_s(H)$<br>$t_s(L)$ | Set-up Time, HIGH or LOW<br>Parallel Inputs to PL | 0<br>0 | | | | 0<br>0 | | ns | |
| $t_h(H)$<br>$t_h(L)$ | Hold Time, HIGH or LOW<br>Parallel Inputs to PL | 2.0<br>2.0 | | | | 2.5<br>2.5 | | | |
| $t_w(H)$<br>$t_w(L)$ | $\overline{CPSI}$ Pulse Width<br>HIGH or LOW | 5.0<br>3.0 | | | | 6.0<br>5.0 | | ns | *403-a, b* |
| $t_w(H)$ | PL Pulse Width, HIGH | 4.0 | | | | 5.0 | | ns | *403-g, h* |
| $t_w(L)$ | $\overline{TTS}$ Pulse Width, LOW<br>Serial or Parallel Mode | 3.5 | | | | 4.0 | | ns | *403-a, b, c, d* |
| $t_w(L)$ | $\overline{MR}$ Pulse Width, LOW | 3.5 | | | | 4.0 | | ns | *403-f* |
| $t_w(H)$<br>$t_w(L)$ | TOP Pulse Width<br>HIGH or LOW | 4.5<br>3.5 | | | | 5.5<br>4.0 | | ns | *403-e* |
| $t_w(H)$<br>$t_w(L)$ | $\overline{CPSO}$ Pulse Width<br>HIGH or LOW | 4.5<br>3.0 | | | | 5.5<br>4.0 | | ns | *403-c, d* |
| $t_{rec}$ | Recovery Time<br>$\overline{MR}$ to Any Input | 5.0 | | | | 5.5 | | ns | *403-f* |

## Timing Waveforms



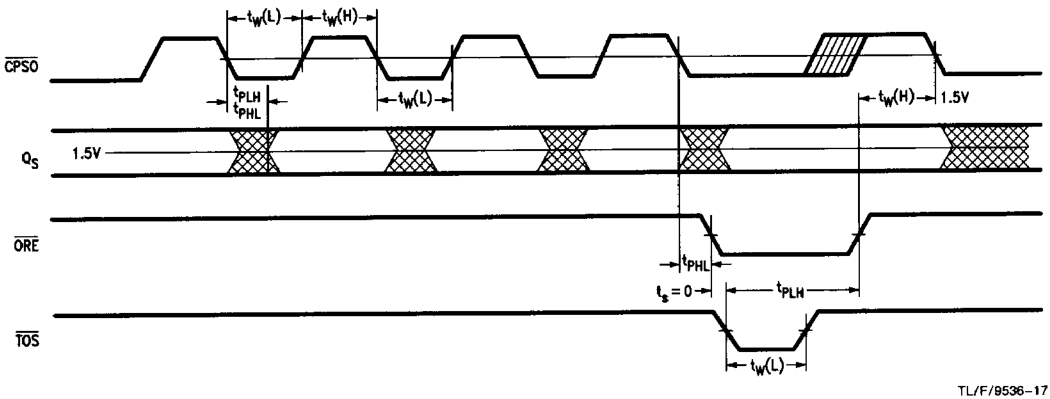

Conditions: stack not full, $\overline{IES}$, PL LOW

**FIGURE 403-a. Serial Input, Unexpanded or Master Operation**




Conditions: stack not full, $\overline{IES}$ HIGH when initiated, PL LOW

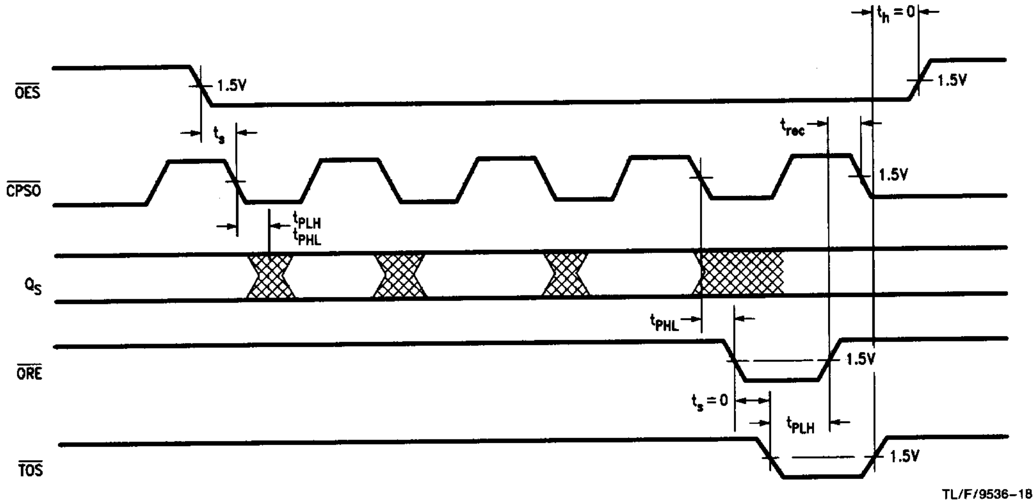
**FIGURE 403-b. Serial Input, Expanded Slave Operation**




Conditions: data in stack, TOP HIGH, $\overline{IES}$ LOW when initiated, $\overline{OES}$ LOW

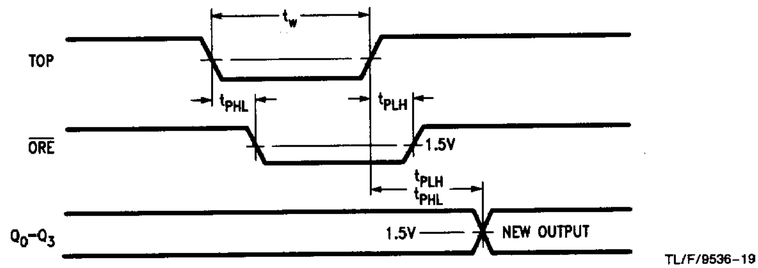
**FIGURE 403-c. Serial Output, Unexpanded or Master Operation**

## Timing Waveforms (Continued)



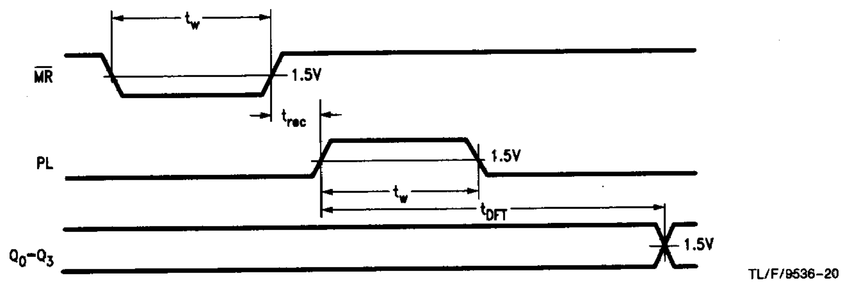

Conditions: data in stack, TOP HIGH, $\overline{IES}$ HIGH when initiated

**FIGURE 403-d. Serial Output, Slave Operation**




Conditions: $\overline{IES}$ LOW when initiated, $\overline{OE}$, $\overline{CPSO}$ LOW; data available in stack

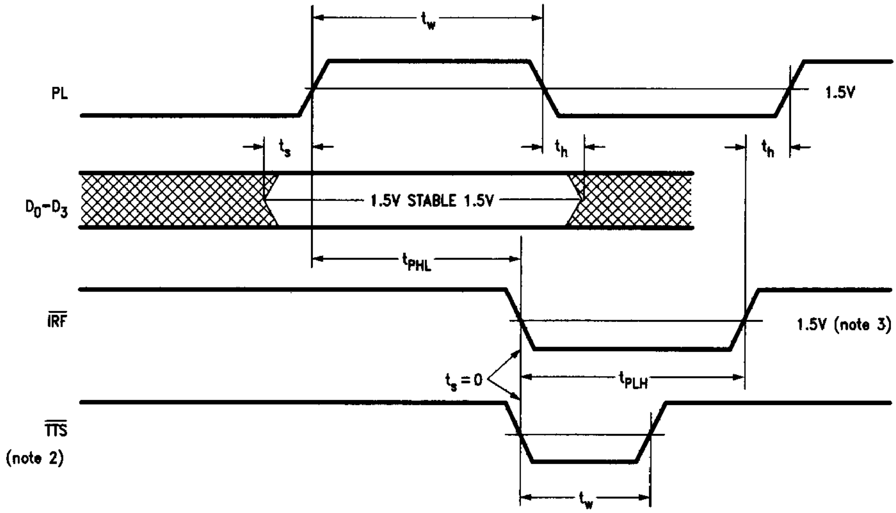
**FIGURE 403-e. Parallel Output, 4-Bit Word or Master in Parallel Expansion**




Conditions: $\overline{TTS}$ connected to $\overline{IRF}$, $\overline{TOS}$ connected to $\overline{ORE}$, $\overline{IES}$, $\overline{OES}$, $\overline{OE}$, $\overline{CPSO}$ LOW, TOP HIGH

**FIGURE 403-f. Fall Through Time**

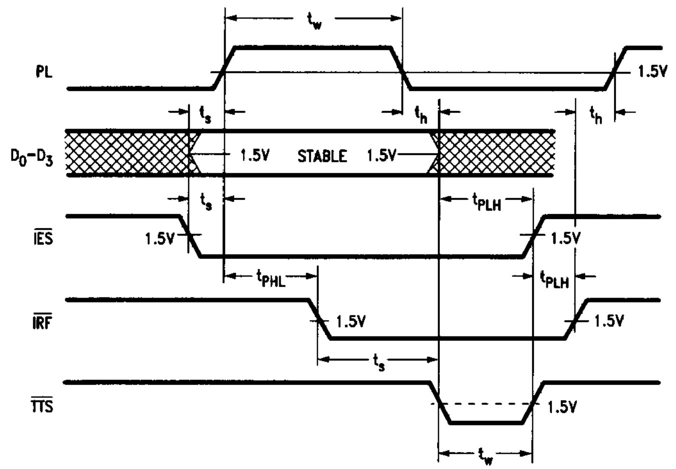
## Timing Waveforms (Continued)




TL/F/9536–21

Conditions: stack not full, $\overline{IES}$ LOW when initialized

**FIGURE 403-g. Parallel Load Mode, 4-Bit Word (Unexpanded) or Master in Parallel Expansion**




TL/F/9536–22

Conditions: stack not full, device initialized (Note 1) with $\overline{IES}$ HIGH

**FIGURE 403-h. Parallel Load, Slave Mode**

**Note 1:** Initialization requires a master reset to occur after power has been applied.

**Note 2:** $\overline{TTS}$ normally connected to $\overline{IRF}$.

**Note 3:** If stack is full, $\overline{IRF}$ will stay LOW.