

Description

The F1429MB is a differential input / single-ended output 3.0GHz to 4.2GHz high-gain RF amplifier. The combination of impedance translation, high gain, high linearity, and low noise performance makes this device an ideal first-stage amplifier for a variety of transmitter applications.

The F1429MB is optimized to operate with a single 5V power supply and a nominal 73mA of I_{CC} . When operated at 3.55GHz, the device provides 21dB typical gain with 1.8dB noise figure, +40dBm OIP3, and +21dBm OP1dB.

The F1429MB is pin-compatible with Renesas' F1429xx family of RF amplifiers (shown below). Each F1429 variant is packaged in a 2 × 2 mm, 12-pin DFN, with a 100Ω differential RF input and 50Ω single-ended RF output impedances for ease of integration into the signal path.

F1429xx Base Part Number	Differential Input Impedance	DC Feed	Frequency Band	Frequency Coverage
F1429LB	100Ω	No	Low	1.4GHz to 3.2GHz
F1429MB	100Ω	No	Mid	3.0GHz to 4.2GHz
F1429HB	100Ω	No	High	4.0GHz to 6.0GHz

Competitive Advantage

- High Gain and Excellent Gain Flatness Over Frequency
- Standby (STBY) Feature
- Differential Input to Directly Interface with Transceiver Outputs

Typical Applications

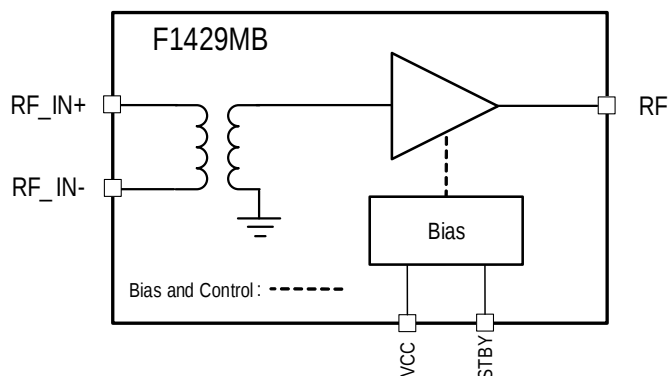
- 5G Massive MIMO Base Stations
- 4G TDD and FDD Base Stations
- Repeaters and DAS
- Point to Point Infrastructure

Features

- RF range: 3.0GHz to 4.2GHz
- Gain = 21dB at 3.55GHz
- Noise figure = 1.8dB at 3.55GHz
- OIP3 = +40dBm at 3.55GHz
- Output P1dB = +21dBm at 3.55GHz
- Gain variation over temperature = ±0.2 typical
- 100Ω differential input impedance
- 50Ω single-ended output impedance
- 3.3V or 5V power supply
- I_{CC} = 73mA at 5V
- 1.3mA standby current
- 1.8V and 3.3V logic support for STBY control
- Operating temperature (T_{EP}) range: -40°C to +115°C
- 2 × 2 mm 12-pin DFN package

Block Diagram

Figure 1. F1429MB Block Diagram



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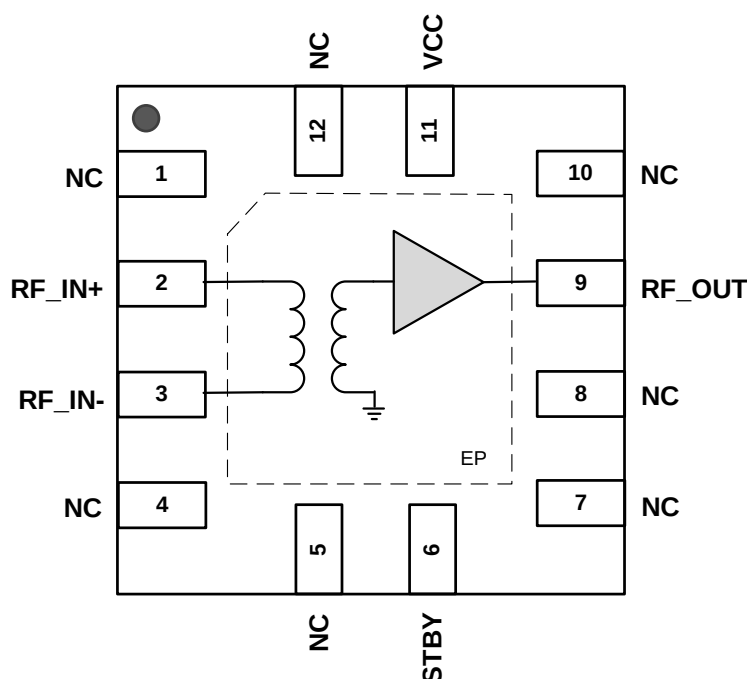
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Pin Assignments

Figure 2. Pin Assignments for 2 × 2 × 0.75 mm 12-pin DFN Package – Top View



Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Description
1, 4, 5, 7, 8, 10, 12	NC	No internal connection. It is highly recommended that these pins be connected to a ground via that is located as close to each pin as possible.
2	RF_IN+	Differential RF input +. Internally tied to ground. Recommendation: Use an external DC block to prevent shorting of any DC voltage that may be present on the preceding RF stage.
3	RF_IN-	Differential RF input -. Internally tied to ground. Recommendation: Use an external DC block to prevent shorting of any DC voltage that may be present on the preceding RF stage.
6	STBY	Standby. If this pin is not connected or is logic LOW, the F1429MB will operate under its normal operating condition. Apply a logic HIGH for STBY.
9	RF_OUT	Single-ended RF output. An external DC block is required.
11	VCC	Connect to the supply voltage via a choke. An external bypass capacitor must be placed as close to the pin as possible.
	– EPAD	Exposed paddle. Internally connected to ground. Solder this exposed paddle to a printed circuit board (PCB) pad that uses multiple ground vias to provide heat transfer out of the F1429MB into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F1429MB at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
VCC to GND	V _{CC}	-0.3	+5.5	V
STBY	V _{STBY}	-0.3	Lower of (5V, V _{CC} + 0.25V)	V
RF Input Power Applied for 24 Hours Maximum (V _{CC} applied, f = 3.55GHz, T _{EP} = +115°C, and input/output VSWR = 1:1 based on a 100Ω system) ^[b]	P _{MAX24}		+20	dBm
Storage Temperature Range	T _{STOR}	-65	+150	°C
Lead Temperature (soldering, 10s)	T _{LEAD}		+260	°C
Electrostatic Discharge – Human Body Model (HBM) (JEDEC/ESDA JS-001-2012)	V _{ESDHBM}		1000	V
Electrostatic Discharge – Charge Device Model (CDM) (JEDEC 22-C101F)	V _{ESDCDM}		1500	V

[a] Exposure to these maximum RF levels can result in significant V_{CC} current draw due to overdriving the amplifier stages.

[b] Tested using an external 2:1 transformer at the RF input.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Power Supply Voltage ^[a]	V _{CC}	V _{CC} pins	4.75		5.25	V
Operating Temperature Range	T _{EP}	Exposed paddle temperature	-40		+115	°C
Junction Temperature	T _{JMAX}				150	°C
RF Frequency Range ^[b]	f _{RF}		3.0		4.2	GHz
RF_IN Source Impedance	Z _{RF_IN}	Differential		100		Ω
RF_OUT Load Impedance	Z _{RF_OUT}	Single-ended		50		Ω

[a] Although the device will operate with a minimum supply voltage of 3.15V, the performance of the device has been optimized to operate within a supply voltage range of 4.75V to 5.25V.

[b] To optimize RF performance, different matching components can be used as described in the BOM.

Electrical Characteristics - 5V Supply

See the F1429MB application circuit. Specifications apply when operated at $V_{CC} = +5.0V$, $f_{RF} = 3.55GHz$, $T_{EP} = +25^{\circ}C$, STBY = logic LOW, $Z_S = 100\Omega$ differential, $Z_L = 50\Omega$ single-ended, and EVKit traces and connectors are de-embedded, unless otherwise stated.

Table 4. Electrical Characteristics with a 5V Supply

Note: See important table notes at the end of the table.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input HIGH Threshold	V_{IH}		1.17 ^[a]			V
Logic Input LOW Threshold	V_{IL}				0.63	V
Logic Current	I_{IH}, I_{IL}	STBY pin using 1.8V logic	-3		+70	μA
Supply Current	I_{CC}			73	86	mA
Standby Current	I_{CC_STBY}			1.3		mA
Settling Time	t_{SETTLE}	From 50% STBY control to within $\pm 0.5dB$ of final gain		400		ns
RF Input Return Loss	RL_{IN}	$f_{RF} = 3.0GHz$		11		dB
		$f_{RF} = 3.3GHz$		20		
		$f_{RF} = 3.55GHz$		30		
		$f_{RF} = 3.8GHz$		30		
		$f_{RF} = 4.2GHz$		27		
RF Output Return Loss	RL_{OUT}	$f_{RF} = 3.0GHz$		8		dB
		$f_{RF} = 3.3GHz$		12		
		$f_{RF} = 3.55GHz$		15		
		$f_{RF} = 3.8GHz$		13		
		$f_{RF} = 4.2GHz$		10		
Gain	G	$f_{RF} = 3.0GHz$		20		dB
		$f_{RF} = 3.3GHz$		20.5		
		$f_{RF} = 3.55GHz$	18	21		
		$f_{RF} = 3.8GHz$		20		
		$f_{RF} = 4.2GHz$		19.5		
Gain Flatness (amplitude)	G_{VAR}	$f_{RF} = 3.1GHz, \pm 100MHz$		0.3		dB
		$f_{RF} = 3.3GHz, \pm 100MHz$		0.1		
		$f_{RF} = 3.55GHz, \pm 100MHz$		0.2		
		$f_{RF} = 3.8GHz, \pm 100MHz$		0.3		
		$f_{RF} = 4.1GHz, \pm 100MHz$		0.4		
Gain Variation over Temperature	G_{TEMP}	$T_{EP} = -40^{\circ}C$ to $+115^{\circ}C$		± 0.2		dB
Reverse Isolation	REV_{ISO}			32		dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Amplitude Imbalance	IMBAL _{AMP}	Measures RF_IN- to RF_OUT and compares RF_IN+ to RF_OUT amplitude		0.4		dB
Phase Imbalance	IMBAL _{PH}	Measures RF_IN- to RF_OUT and compares RF_IN+ to RF_OUT phase. Deviation is from ideal 180 degrees.		0.9		deg
Common Mode Rejection	CMR			31.5		dB
Noise Figure	NF	f _{RF} = 3.0GHz		1.6		dB
		f _{RF} = 3.3GHz		1.9		
		f _{RF} = 3.55GHz		1.8	2	
		f _{RF} = 3.8GHz		1.6		
		f _{RF} = 4.2GHz		1.8		
Noise Figure Variation over Temperature	NF _{TEMP}	T _{EP} = -40°C to +115°C		±0.65		dB
Output Third-Order Intercept Point ^[b]	OIP3	f _{RF} = 3.0GHz		38		dBm
		f _{RF} = 3.3GHz		37		
		f _{RF} = 3.55GHz	T _{EP} = 25°C	40		
			T _{EP} = -40°C to +115°C	32		
		f _{RF} = 3.8GHz		37		
		f _{RF} = 4.2GHz		37		
Output P1dB	OP1dB	f _{RF} = 3.0GHz		21		dBm
		f _{RF} = 3.3GHz		21		
		f _{RF} = 3.55GHz	18	21		
		f _{RF} = 3.8GHz		20		
		f _{RF} = 4.2GHz		20		
2 nd Order Harmonic Distortion ^[c]	HD2			-34		dBc
3 rd Order Harmonic Distortion ^[c]	HD3			-46		dBc

[a] Specifications in the minimum/maximum columns that are shown in ***bold italics*** are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] OIP3 test conditions: Tone spacing = 5MHz, P_{OUT} = +0dBm/tone.

[c] Harmonic Distortion test conditions: P_{OUT} = +0dBm/tone.

Electrical Characteristics - 3.3V Supply

See the F1429MB application circuit. Specifications apply when operated at $V_{CC} = +3.3V$, $f_{RF} = 3.55GHz$, $T_{EP} = +25^{\circ}C$, STBY = logic LOW, $Z_S = 100\Omega$ differential, $Z_L = 50\Omega$ single-ended, and EVKit traces and connectors are de-embedded, unless otherwise stated.

Table 5. Electrical Characteristics with a 3.3V Supply

Note: See important table notes at the end of the table.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Logic Input High Threshold	V_{IH}		1.17 ^[a]			V
Logic Input Low Threshold	V_{IL}				0.63	V
Logic Current	I_{IH}, I_{IL}	STBY pin using 1.8V logic	-3		+70	μA
Supply Current	I_{CC}			30		mA
Standby Current	I_{CC_STBY}			1.5		mA
RF Input Return Loss	RL_{IN}	$f_{RF} = 3.0GHz$		9		dB
		$f_{RF} = 3.3GHz$		17		
		$f_{RF} = 3.55GHz$		21		
		$f_{RF} = 3.8GHz$		19		
		$f_{RF} = 4.2GHz$		16		
RF Output Return Loss	RL_{OUT}	$f_{RF} = 3.0GHz$		10		dB
		$f_{RF} = 3.3GHz$		15		
		$f_{RF} = 3.55GHz$		15		
		$f_{RF} = 3.8GHz$		12		
		$f_{RF} = 4.2GHz$		8		
Gain	G	$f_{RF} = 3.0GHz$		19		dB
		$f_{RF} = 3.3GHz$		19		
		$f_{RF} = 3.55GHz$		19		
		$f_{RF} = 3.8GHz$		18.5		
		$f_{RF} = 4.2GHz$		17.5		
Gain Flatness (amplitude)	G_{VAR}	$f_{RF} = 3.1GHz, \pm 100MHz$		0.3		dB
		$f_{RF} = 3.3GHz, \pm 100MHz$		0.1		
		$f_{RF} = 3.55GHz, \pm 100MHz$		0.4		
		$f_{RF} = 3.8GHz, \pm 100MHz$		0.5		
		$f_{RF} = 4.1GHz, \pm 100MHz$		0.6		
Gain Variation over Temperature	G_{TEMP}	$T_{EP} = -40^{\circ}C$ to $+115^{\circ}C$		± 0.2		dB
Reverse Isolation	REV_{ISO}			31		dB
Amplitude Imbalance	$IMBAL_{AMP}$	Measures RF_IN- to RF_OUT and compares RF_IN+ to RF_OUT amplitude		0.4		dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Phase Imbalance	IMBAL _{PH}	Measures RF_IN- to RF_OUT and compares RF_IN+ to RF_OUT phase. Deviation is from ideal 180 degrees		0.9		deg
Common Mode Rejection	CMR			31.5		deg
Noise Figure	NF	f _{RF} = 3.0GHz		1.7		dB
		f _{RF} = 3.3GHz		1.9		
		f _{RF} = 3.55GHz		1.9		
		f _{RF} = 3.8GHz		1.8		
		f _{RF} = 4.2GHz		1.9		
Noise Figure Variation over Temperature	NF _{TEMP}	T _{EP} = -40°C to +115°C		±0.75		dB
Output Third-Order Intercept Point ^[b]	OIP3	f _{RF} = 3.0GHz		28		dBm
		f _{RF} = 3.3GHz		29		
		f _{RF} = 3.55GHz		28		
		f _{RF} = 3.8GHz		26		
		f _{RF} = 4.2GHz		25		
Output P1dB	OP1dB	f _{RF} = 3.0GHz		15.5		dBm
		f _{RF} = 3.3GHz		15.5		
		f _{RF} = 3.55GHz		15		
		f _{RF} = 3.8GHz		15		
		f _{RF} = 4.2GHz		14		

[a] Specifications in the minimum/maximum columns that are shown in bold italics are guaranteed by test. Specifications in these columns that are not shown in bold italics are guaranteed by design characterization.

[b] OIP3 test conditions: Tone spacing = 5MHz, POUT = +0dBm/tone.

Thermal Characteristics

Table 6. Thermal Characteristics

Parameter	Symbol	Value	Units
Junction-to-Ambient Thermal Resistance.	θ_{JA}	112.57	°C/W
Junction-to-Case Thermal Resistance. (Case is defined as the exposed paddle)	θ_{JC-BOT}	27.6	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions (TOC)

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- Evaluation kit connector and trace losses are de-embedded
- $V_{CC} = 5.0V$ (plots also taken with $V_{CC} = 3.3V$)
- $T_{EP} = 25^{\circ}C$
- STBY = not connected (internally pulled to logic LOW)
- Small signal parameters measured with $P_{OUT} = 0dBm$
- Two tone tests $P_{OUT} = 0dBm/tone$ with 5MHz tone spacing
- All unused ports properly terminated.
- S-parameters (S11, S21, S12, and S22) measured using a de-embedded Differential Board (EVKit) with $Z_S =$ differential 100 Ω and $Z_L =$ single-ended 50 Ω . The inputs are mathematically combined using an ideal 1:2 (50 Ω :100 Ω) transformer to produce the two port S-parameters.
- OIP3, Output P1dB, and Noise Figure measured using a Transformer Board EVKit with $Z_S = Z_L =$ single-ended 50 Ω .
- Amplitude and phase imbalances measures RF_IN+ to RF_OUT and compares to RF_IN- to RF_OUT.
- The phase imbalance is the deviation from an ideal 180 degrees.

Note: The use of the external transformer T1 is included for simple two-port evaluation purposes. At some frequencies, the external transformer interacts with the on-chip balun affecting the gain and noise figure flatness responses. These interactions have been removed from the noise figure TOCs.

Typical 5V Performance Characteristics

Figure 3. Gain

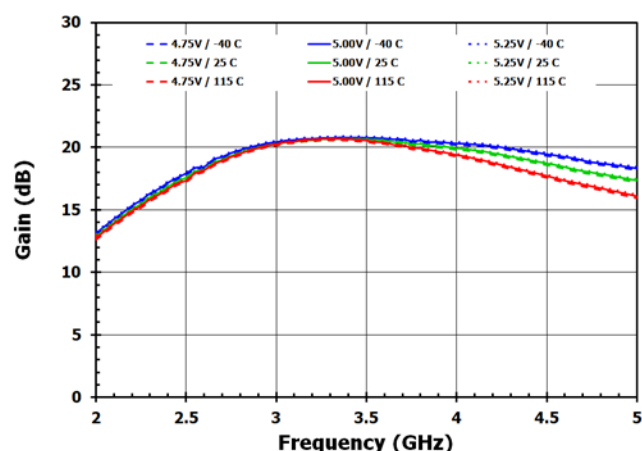


Figure 4. Reverse Isolation

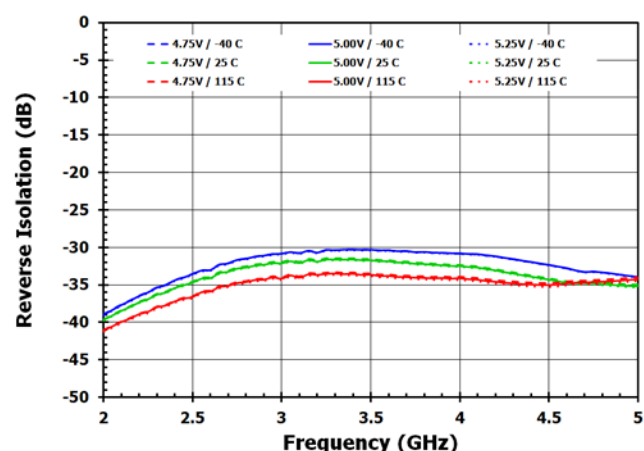


Figure 5. Input Return Loss

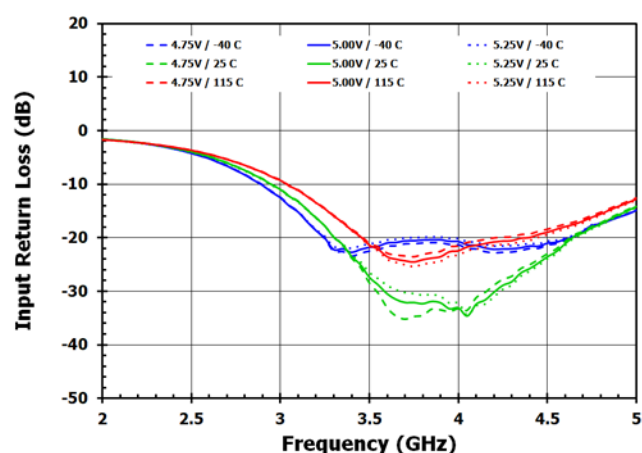


Figure 6. Output Return Loss

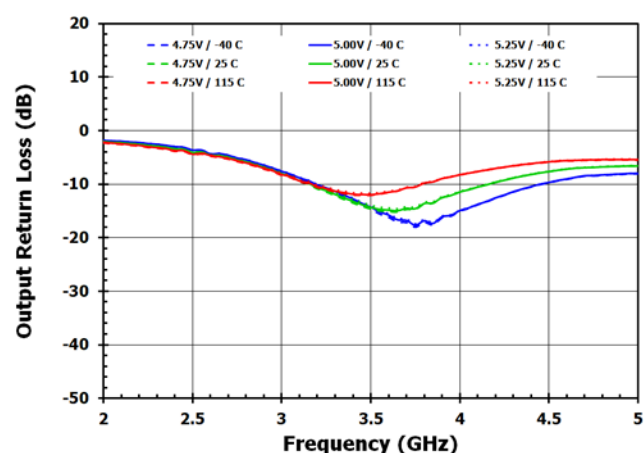


Figure 7. Output IP3

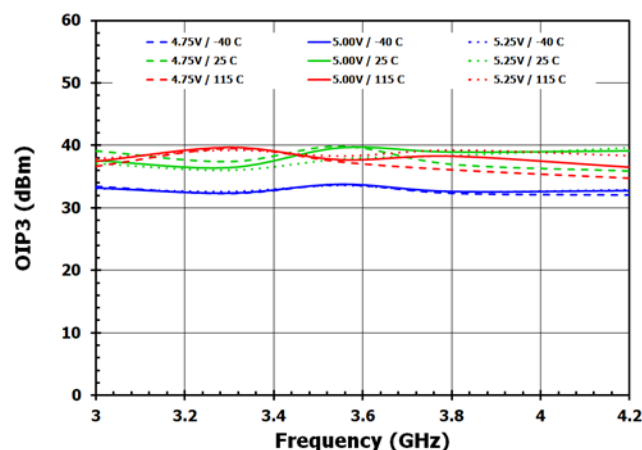


Figure 8. Output P1dB

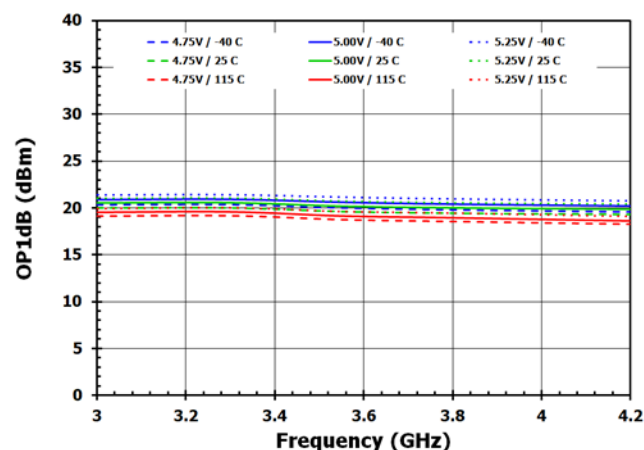


Figure 9. Noise Figure

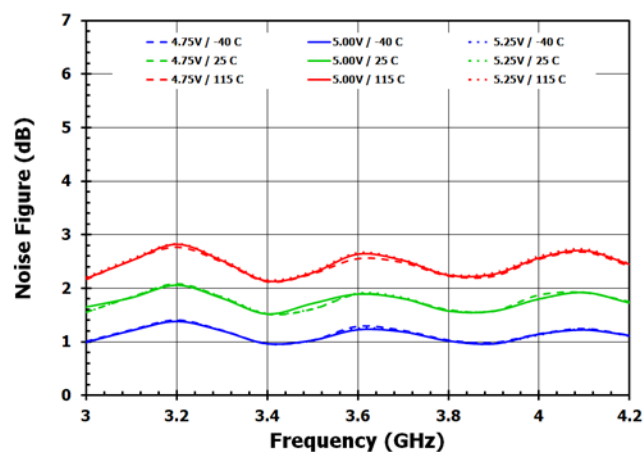


Figure 10. Amplitude Imbalance

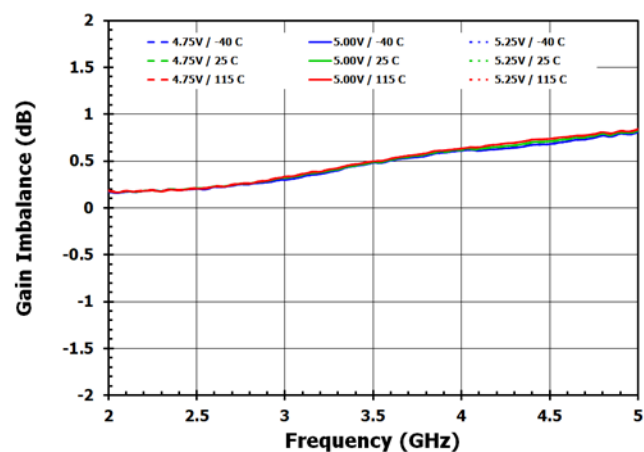


Figure 11. Phase Imbalance

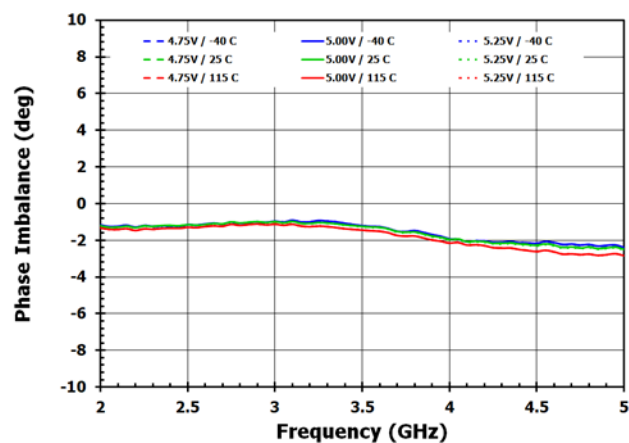
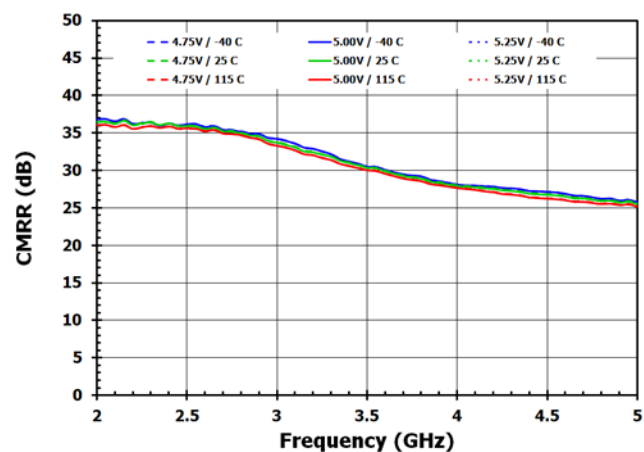


Figure 12. CMR



Typical 3.3V Performance Characteristics

Figure 13. Gain

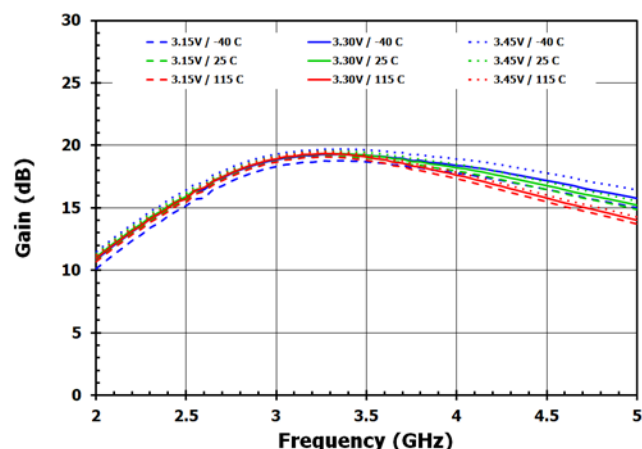


Figure 14. Reverse Isolation

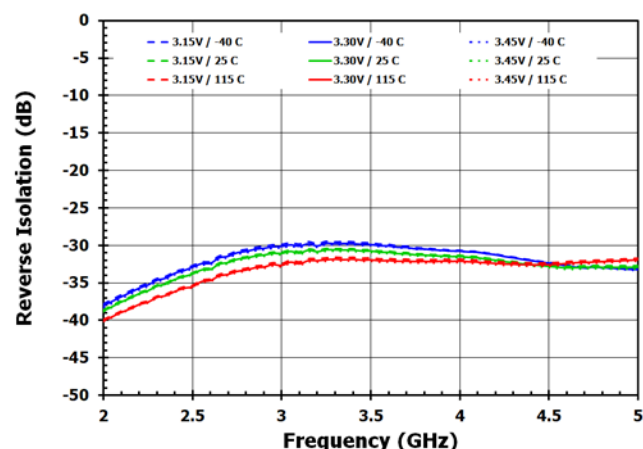


Figure 15. Input Return Loss

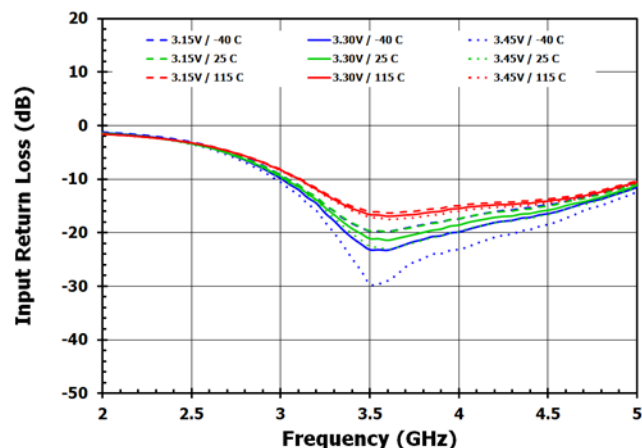


Figure 16. Output Return Loss

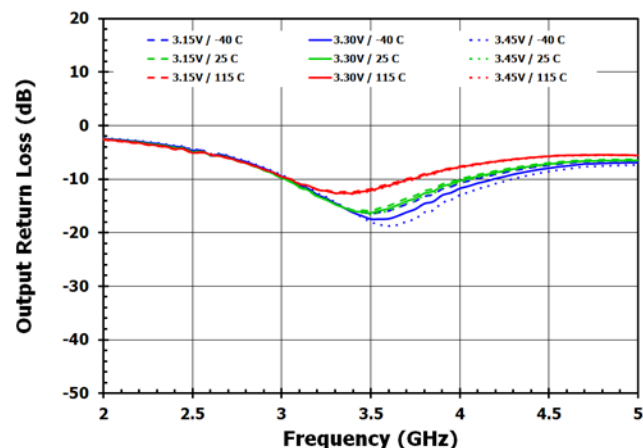


Figure 17. Output IP3

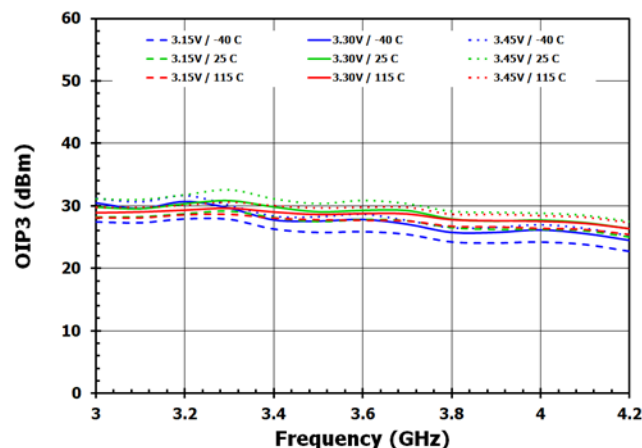


Figure 18. Output P1dB

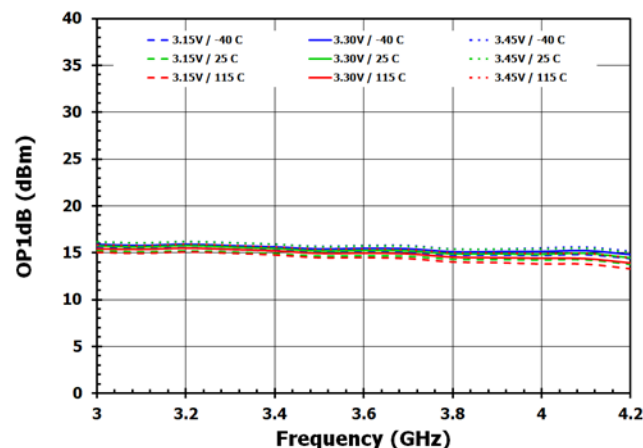


Figure 19. Noise Figure

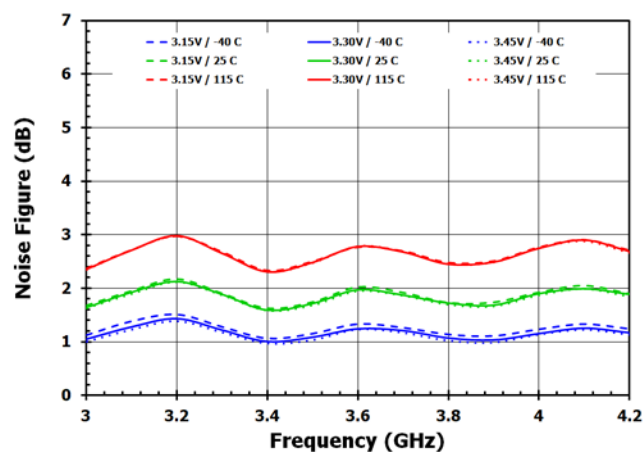


Figure 20. Amplitude Imbalance

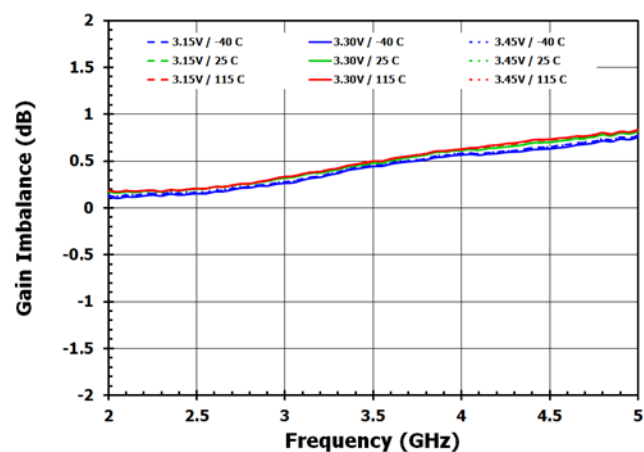


Figure 21. Phase Imbalance

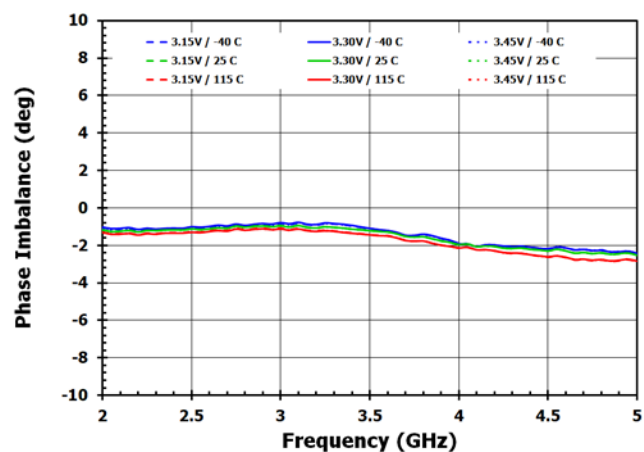
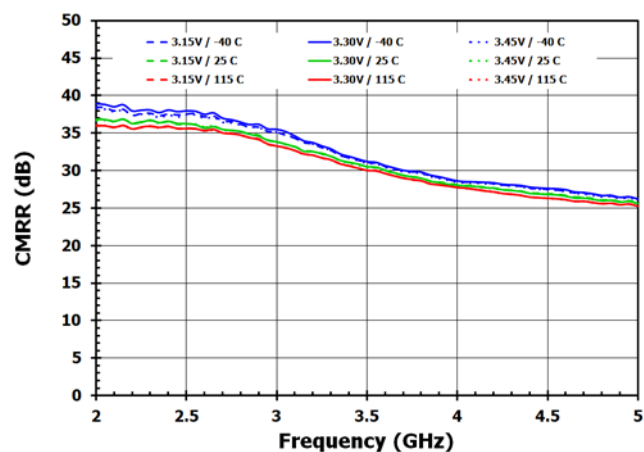


Figure 22. CMR



Evaluation Kit Picture

Figure 23. Evaluation Kit – Top View

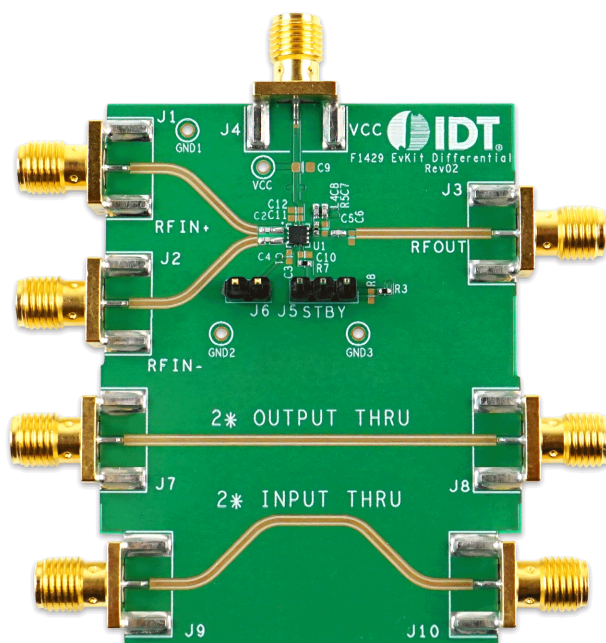
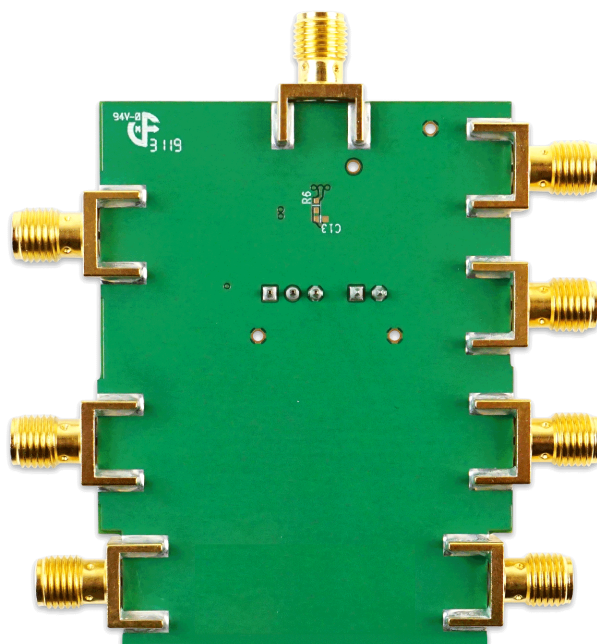


Figure 24. Evaluation Kit – Bottom View



Evaluation Kit Circuit

Figure 25. Evaluation Kit Electrical Schematic

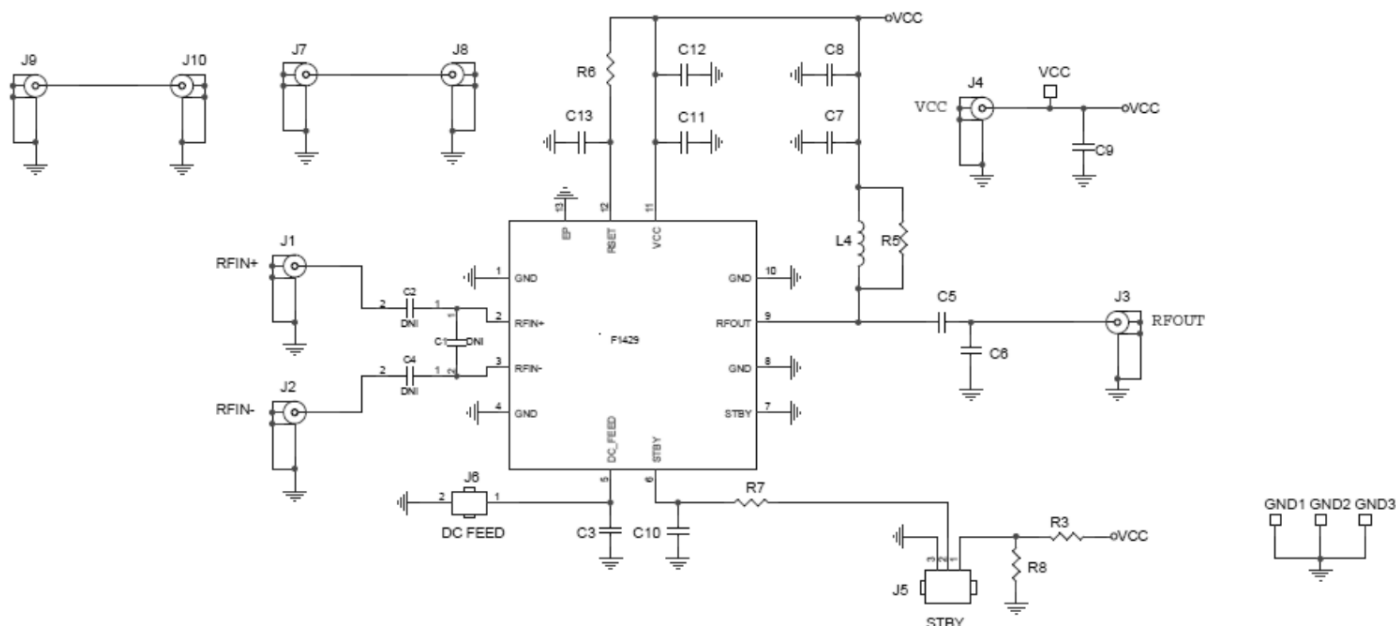


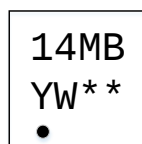
Table 7. Evaluation Kit Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
R7,R3	2	0 ohm Jumper 1/10W (0402)	ERJ2GE0R00X	Panasonic
C8	1	1000pF C0G 50v (0402)	GRM1555C1H102J	Murata
C11	1	Do not Install		
C7	1	100pF C0G 50v (0402)	GRM1555C1H101J	Murata
C2, C4	2	15pF C0G 50v (0402)	GJM1555C1H150J	Murata
C10	1	Do not Install		
L4	1	1.5nH +/-0.3 (0402)	LQG15HS1N5S02	Murata
C5	1	3.3pF COG 50V (0402)	GJM1555C1H3R3B	Murata
J5	1	CONN HEADER VERT 1x3 POS 2.54MM	61300311121	Würth Elektronik
J1,J2, J3, J4, J7, J8, J9, J10	6	SMA Edge Mount	142-0701-851	Cinch Connectivity
C1,C12, C3, C6, C9, R2, R5, R8, J6	0	Do not Install		
U1	1	F1429MB 100Ω DIFF-In — 50Ω SE-Out Amplifier	F1429MBNELI	IDT Renesas
	1	Printed Circuit Board	F1429 EVKIT DIFF Rev.02	Vector Fab

Package Outline Drawings

The [package outline drawings](#) are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram



Line 1: 14MB = abbreviated part number (F1429MB).

Line 2: Y = Year code, last digit of production year ("8" would correspond to 2018).

W = Work week code ("W" corresponds to week 30).

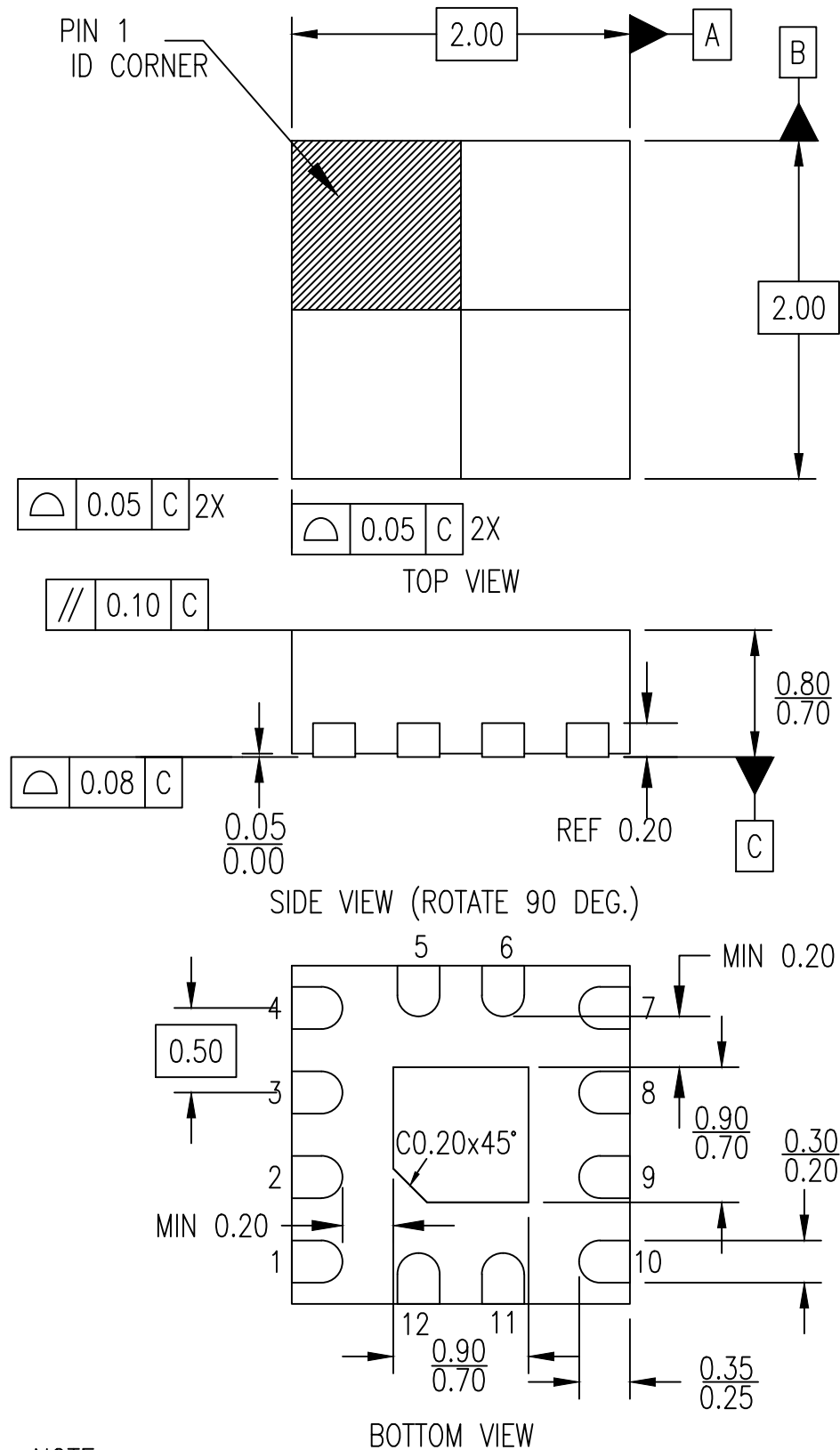
** = Sequential alpha characters for lot traceability.

Ordering Information

Orderable Part Number	Package	MSL Rating	Carrier Type	Temperature
F1429MBNELI	2 × 2 × 0.75 mm 12-DFN	1	Cut Reel	-40° to +115°C
F1429MBNELI8	2 × 2 × 0.75 mm 12-DFN	1	Reel	-40° to +115°C
F1429MBEVB	Evaluation Board			

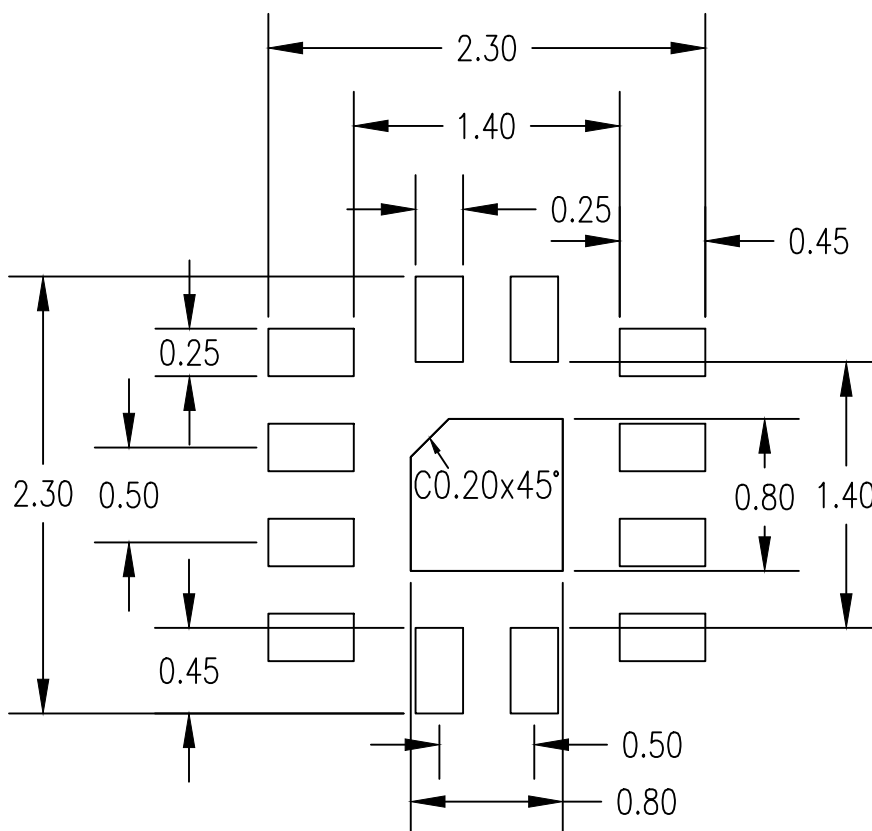
Revision History

Revision Date	Description of Change
January 31, 2021	- Updated the Package Outline Drawings website link - Updated the Carrier Type information in Ordering Information
May 21, 2020	- Updated base part number table in Description. - Updated Evaluation Kit Electrical Schematic.
April 29, 2020	Corrected typo in RF_OUT pin description (see Table 1).
January 28, 2020	Updated the evaluation kit pictures in Figure 23 and Figure 24.
November 22, 2019	Initial release.



NOTE:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASMEY14.5-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 5, 2018	Rev 01	Add "K" Value Minimum 0.20 mm, Correct L/F Thickness
July 31, 2017	Rev 00	Initial Release

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