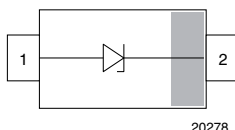
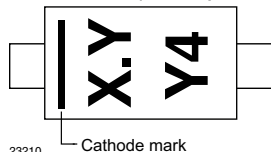


Small Signal Zener Diodes



20278

MARKING (example only)


X.Y = type code
Y4 = date code

23210

Cathode mark

LINKS TO ADDITIONAL RESOURCES



3D Models



Models

FEATURES

- Silicon planar Zener diodes
- Standard Zener voltage tolerance is $\pm 5\%$
- AEC-Q101 qualified available
- ESD capability according to AEC-Q101:
Human body model > 8 kV
Machine model > 800 V
- Base P/N-E3 - RoHS-compliant, commercial grade
- Base P/N-HE3_A - RoHS-compliant, AEC-Q101 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRIMARY CHARACTERISTICS

PARAMETER	VALUE	UNIT
V _Z range nom.	2.4 to 43	V
Test current I _{ZT}	0.05	mA
V _Z specification	Thermal equilibrium	
Circuit configuration	Single	

ORDERING INFORMATION

DEVICE NAME	ORDERING CODE	AEC-Q101 QUALIFIED	TAPED UNITS PER REEL	MINIMUM ORDER QUANTITY
MMSZ4681 to MMSZ4717	MMSZ4681-E3-08 to MMSZ4717-E3-08	no	3000 (8 mm tape on 7" reel)	15 000/box
	MMSZ4681-HE3_A-08 to MMSZ4717-HE3_A-08	yes		
	MMSZ4681-E3-18 to MMSZ4717-E3-18	no	10 000 (8 mm tape on 13" reel)	10 000/box
	MMSZ4681-HE3_A-18 to MMSZ4717-HE3_A-18	yes		

PACKAGE

PACKAGE NAME	WEIGHT	MOLDING COMPOUND FLAMMABILITY RATING	MOISTURE SENSITIVITY LEVEL	SOLDERING CONDITIONS
SOD-123	10.6 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	Peak temperature max. 260 °C

ABSOLUTE MAXIMUM RATINGS (T_{amb} = 25 °C, unless otherwise specified)

PARAMETER	TEST CONDITION	SYMBOL	VALUE	UNIT
Power dissipation	R _{thJL} = 250 K/W	P _{tot}	500	mW
	On FR-4 board with recommended soldering footprint	P _{tot}	300	mW
Thermal resistance junction to lead		R _{thJL}	250	K/W
Thermal resistance junction to ambient	According to JEDEC® 51-3 on FR-4 board with recommended soldering footprint	R _{thJA}	420	K/W
Junction temperature		T _j	150	°C
Storage temperature range		T _{stg}	-65 to +150	
Operating temperature range		T _{op}	-55 to +150	

**ELECTRICAL CHARACTERISTICS** ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

PART NUMBER	MARKING CODE	ZENER VOLTAGE RANGE ⁽¹⁾			TEST CURRENT	REVERSE CURRENT	
		V _Z at I _{ZT1}			I _{ZT1}	I _R at V _R	
		V			mA	μA	V
		MIN.	NOM.	max.		MAX.	
MMSZ4681	TF	2.28	2.4	2.52	0.05	2	1
MMSZ4682	TH	2.57	2.7	2.84	0.05	1	1
MMSZ4683	TJ	2.85	3	3.15	0.05	0.8	1
MMSZ4684	TK	3.14	3.3	3.47	0.05	7.5	1.5
MMSZ4685	TM	3.42	3.6	3.78	0.05	7.5	2
MMSZ4686	TN	3.71	3.9	4.1	0.05	5	2
MMSZ4687	TP	4.09	4.3	4.52	0.05	4	2
MMSZ4688	TT	4.47	4.7	4.94	0.05	10	3
MMSZ4689	TU	4.85	5.1	5.36	0.05	10	3
MMSZ4690	TV	5.32	5.6	5.88	0.05	10	4
MMSZ4691	TA	5.89	6.2	6.51	0.05	10	5
MMSZ4692	TX	6.46	6.8	7.14	0.05	10	5.1
MMSZ4693	TY	7.13	7.5	7.88	0.05	10	5.7
MMSZ4694	TZ	7.79	8.2	8.61	0.05	1	6.2
MMSZ4695	UC	8.27	8.7	9.14	0.05	1	6.6
MMSZ4696	UD	8.65	9.1	9.56	0.05	1	6.9
MMSZ4697	UE	9.5	10	10.5	0.05	1	7.6
MMSZ4698	UF	10.5	11	11.6	0.05	0.05	8.4
MMSZ4699	UH	11.4	12	12.6	0.05	0.05	9.1
MMSZ4700	UJ	12.4	13	13.7	0.05	0.05	9.8
MMSZ4701	UK	13.3	14	14.7	0.05	0.05	10.6
MMSZ4702	UM	14.3	15	15.8	0.05	0.05	11.4
MMSZ4703	UN	15.2	16	16.8	0.05	0.05	12.1
MMSZ4704	UP	16.2	17	17.9	0.05	0.05	12.9
MMSZ4705	UT	17.1	18	18.9	0.05	0.05	13.6
MMSZ4706	UU	18.1	19	20	0.05	0.05	14.4
MMSZ4707	UV	19	20	21	0.05	0.01	15.2
MMSZ4708	UA	20.9	22	23.1	0.05	0.01	16.7
MMSZ4709	UZ	22.8	24	25.2	0.05	0.01	18.2
MMSZ4710	UY	23.8	25	26.3	0.05	0.01	19
MMSZ4711	ZA	25.7	27	28.4	0.05	0.01	20.4
MMSZ4712	ZC	26.6	28	29.4	0.05	0.01	21.2
MMSZ4713	ZD	28.5	30	31.5	0.05	0.01	22.8
MMSZ4714	ZE	31.4	33	34.7	0.05	0.01	25
MMSZ4715	ZF	34.2	36	37.8	0.05	0.01	27.3
MMSZ4716	ZH	37.1	39	41	0.05	0.01	29.6
MMSZ4717	ZJ	40.9	43	45.2	0.05	0.01	32.6

Notes

- Maximum $V_F = 0.9\text{ V}$ at $I_F = 10\text{ mA}$
- (1) Measured with device junction in thermal equilibrium typ. R_{thJA} of 370 K/W

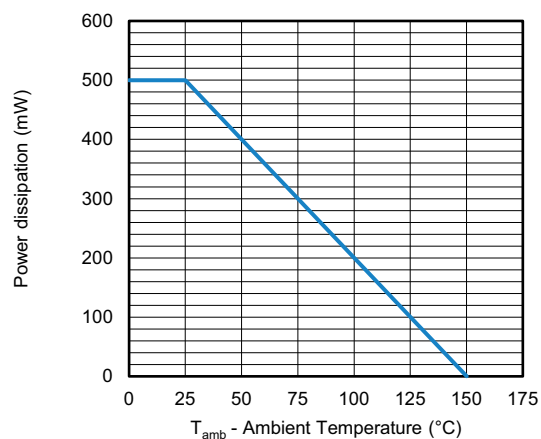
TYPICAL CHARACTERISTICS ($T_{amb} = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)


Fig. 1 - Admissible Power Dissipation vs. Ambient Temperature

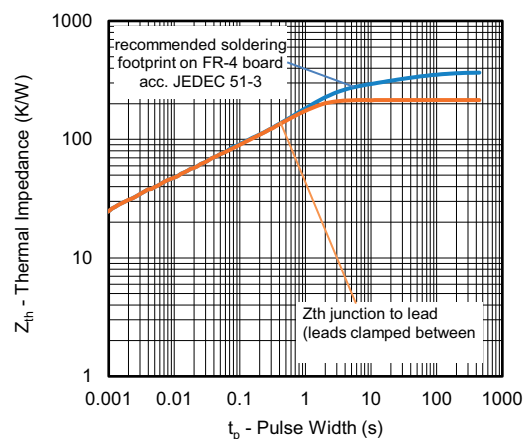
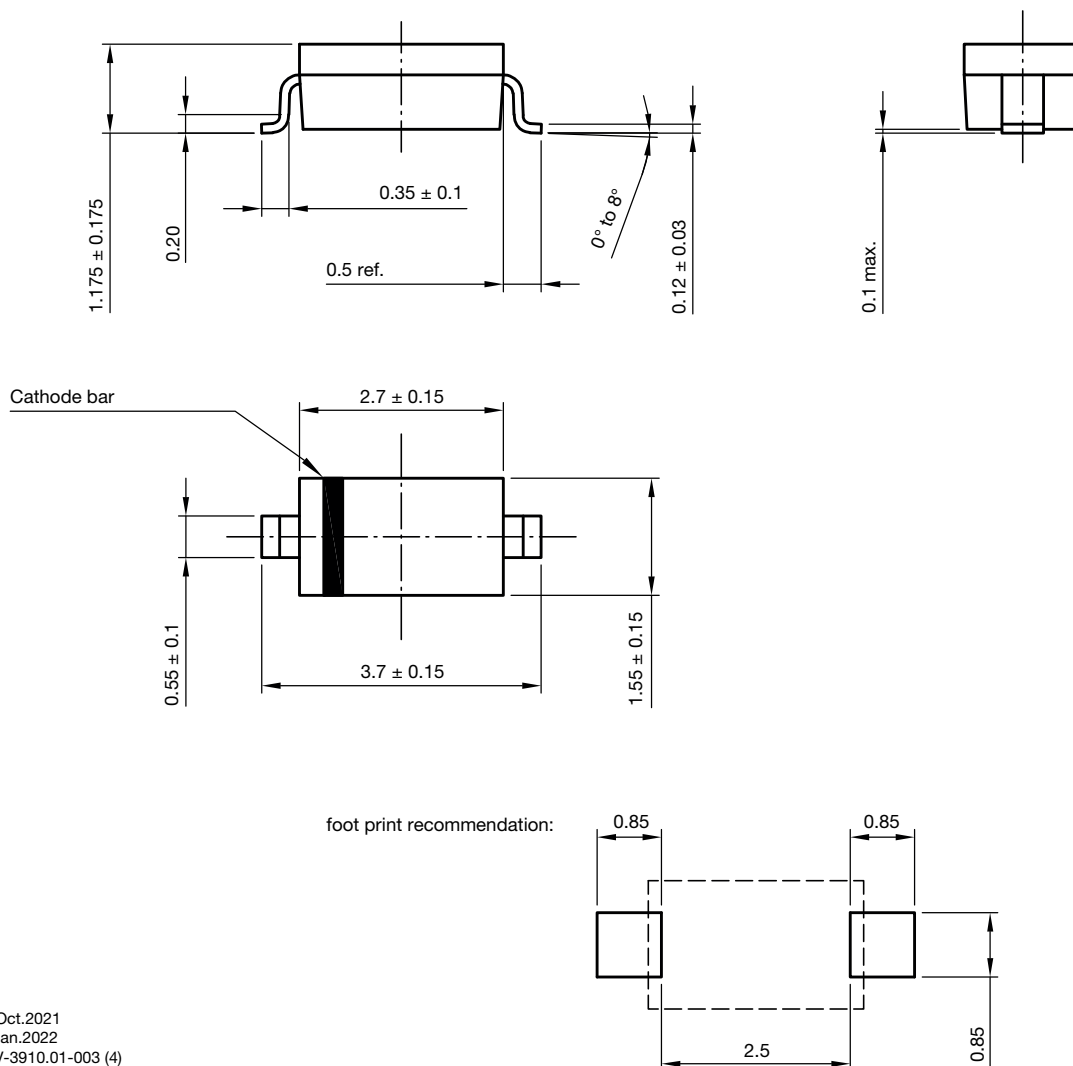


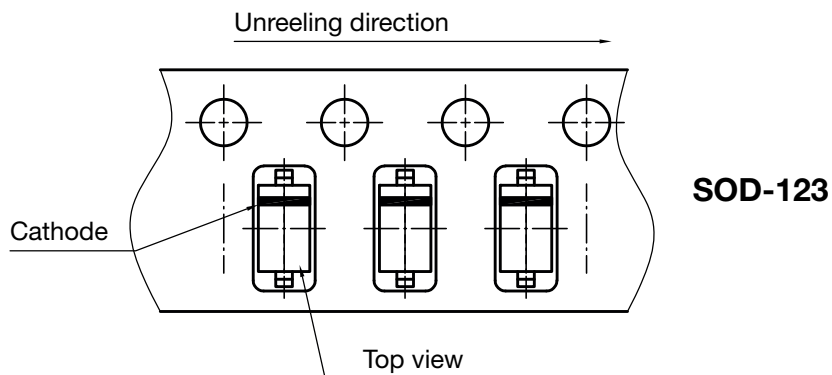
Fig. 2 - Thermal Impedance vs. Time

PACKAGE DIMENSIONS in millimeters (inches): **SOD-123**


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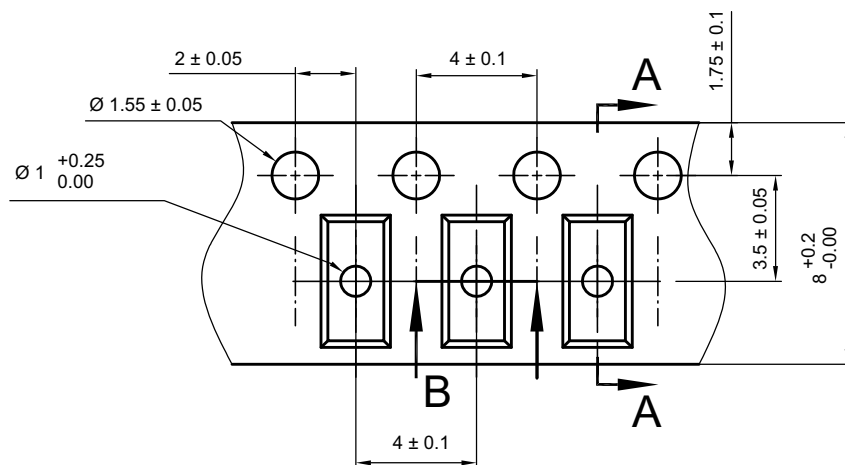


ORIENTATION IN CARRIER TAPE

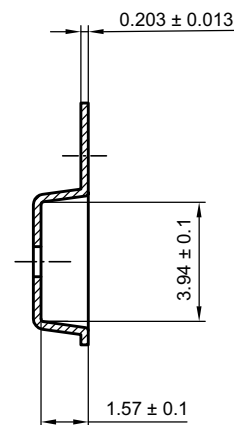


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Rev. 01 - Date: 07. Nov. 2022
Document no.: S8-V-3717.10-003 (4)

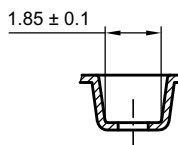
CARRIER TAPE



A-A Section



B-B Section



Created - Date: 07. Feb. 2013
Rev. 01 - Date: 01. Mar. 2014
Document no.: S8-V-3717.10-003 (4)



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