

LC7935AN

Allowable Operating Conditions at Ta = -10 to +70°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V _{DD}	V _{DD}	4.5		5.5	V
H-level input voltage	V _{IH}	S _{IN} , CLOCK, LATCH, BEO, STROBE	0.8V _{DD}		V _{DD}	V
L-level input voltage	V _{IL}	S _{IN} , CLOCK, LATCH, BEO, STROBE	V _{SS(L)}		0.2V _{DD}	V
Clock frequency	f _{CLK}	CLOCK: Duty: 50%			5.0	MHz
Clock pulse width	t _{Wφ}	CLOCK	75			ns
Clock rise/fall time	t _r , t _f	CLOCK			200	ns
Data setup time	t _{DS}	S _{IN} , CLOCK	100			ns
Data hold time	t _{DH}	S _{IN} , CLOCK	50			ns
Latch pulse width	t _{WL}	LATCH	100			ns

Electrical Characteristics at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
H-level input current	I _{IH1}	S _{IN} , CLOCK, LATCH			10	μA
	I _{IH2}	BEO	12		72	μA
L-level input current	I _{IL1}	S _{IN} , CLOCK, LATCH	-10			μA
	I _{IL2}	STROBE	-72		-12	μA
H-level output voltage	V _{OH}	S _{OUT} : V _{DD} =5V, I _{OH} =-0.5mA	V _{DD} -0.5			V
L-level output voltage	V _{OL1}	S _{OUT} : V _{DD} =5V, I _{OL} =0.5mA			0.5	V
	V _{OL2}	D1 to D32: V _{DD} =5V, I _{OL} =30mA			0.5	V
Output OFF-state leakage current	I _{OFF}	D1 to D32: V _O =24V			20	μA
Input capacitance	C _{IN}	CLOCK		5.0		pF
Operating current drain	I _{DD}	V _{DD} : V _{DD} =5V, f _{CLK} =5MHz, All outputs - no load			5	mA

Switching Characteristics at Ta = 25°C

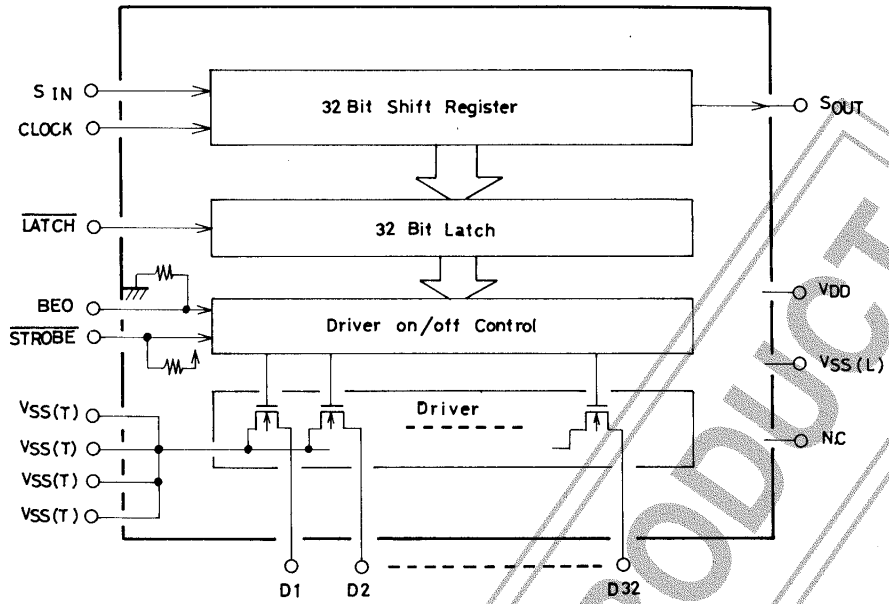
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Clock latch delay width	t _{CL}	CLOCK, LATCH: V _{DD} =5V	100			ns
Latch clock delay width	t _{LC}	CLOCK, LATCH: V _{DD} =5V	0			ns
H-level output propagation delay time	t _{PLH1}	LATCH, D1 to D32: V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			400	ns
	t _{PLH2}	BEO, STROBE: V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			300	ns
	t _{PLH3}	CLOCK, S _{OUT} : V _{DD} =5V, S _{OUT} : C _L =15pF			200	ns
L-level output propagation delay time	t _{PHL1}	LATCH, D1 to D32: V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			200	ns
	t _{PHL2}	BEO, STROBE, D1 to D32: V _{DD} =5V, Dn: R _L =1.0kΩ, C _L =15pF			100	ns
	t _{PHL3}	CLOCK, S _{OUT} : V _{DD} =5V, S _{OUT} : C _L =15pF			200	ns

Driver ON/OFF Truth Table

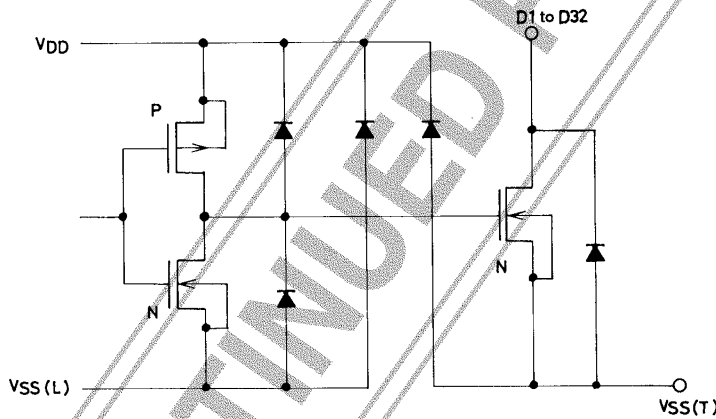
Latch Data (Q)	BEO	STROBE	Driver
0	0	0	OFF
1	0	0	OFF
0	1	0	OFF
1	1	0	ON Driver on
0	0	1	OFF
1	0	1	OFF
0	1	1	OFF
1	1	1	OFF

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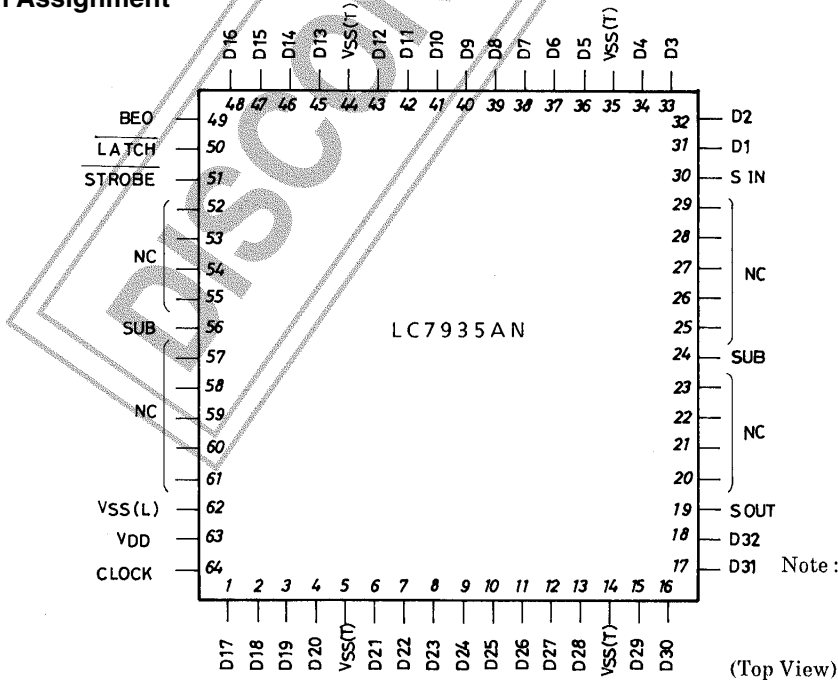
Equivalent Circuit Block Diagram



Output Driver Section Equivalent Circuit



Pin Assignment

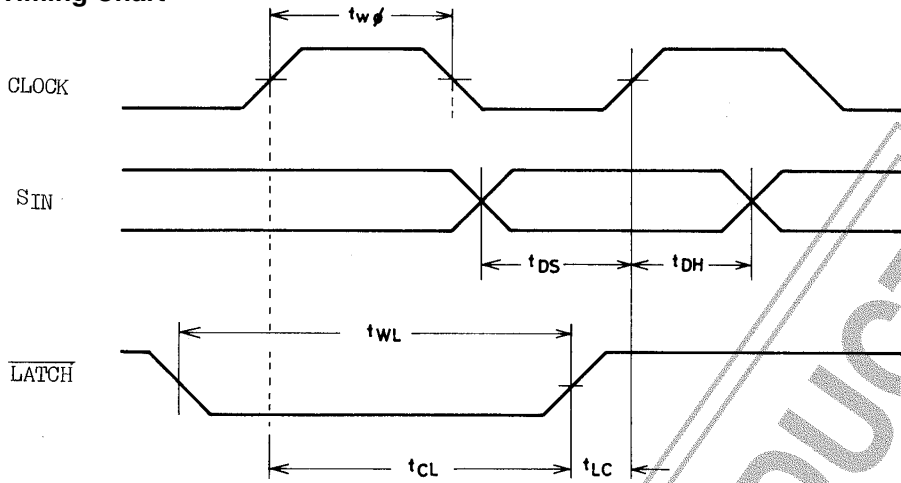


Note: SUB pin and NC pin must be kept open. [SUB pin is connected to the substrate (V_{DD}).]

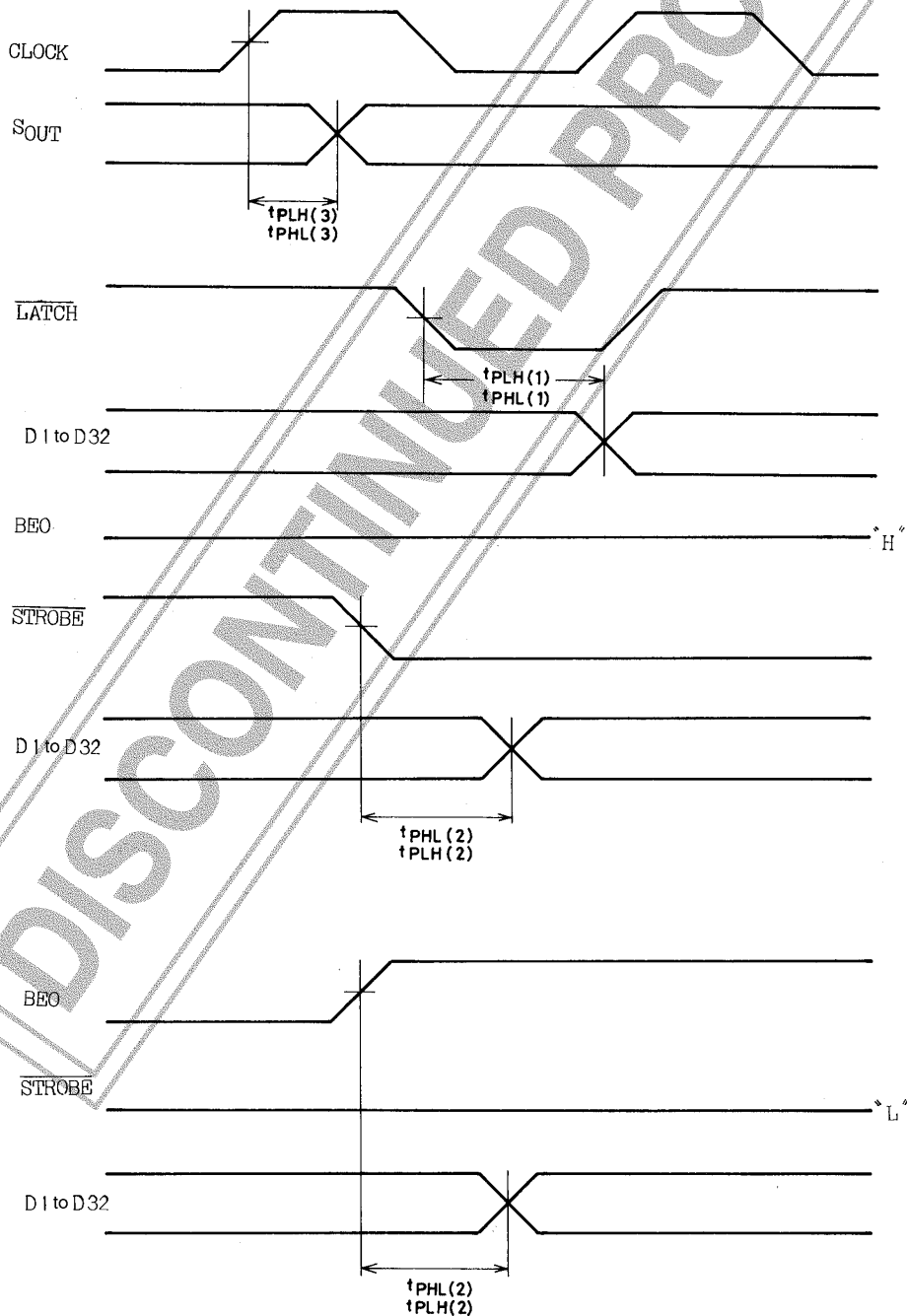
(Top View)

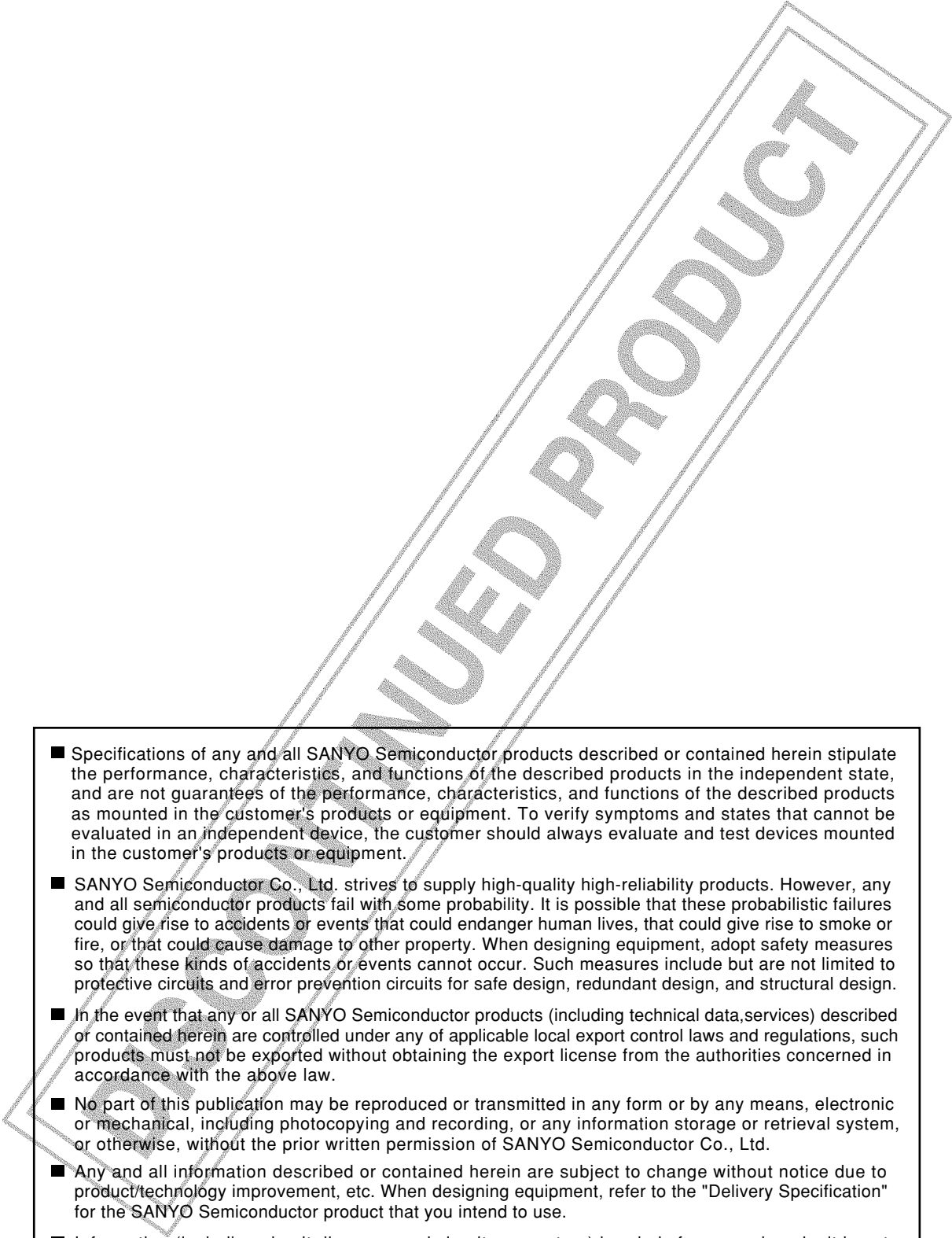
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Input Data Timing Chart



Output Data Timing Chart



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