

## SANYO Semiconductors DATA SHEET

CMOS IC

# LC7935AN — General-Purpose 32-Bit Shift Register **Latch Driver**

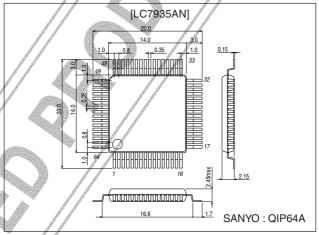
#### **Features**

- High-speed, high-voltage silicon gate CMOS device.
- Contains high-speed shiftable (5MHz max) 32-bit shift register, 32-bit latch, output driver on/off control circuit, 32-bit N-channel open drain output driver.
- Serial shift data is shifted on the positive transition of the clock (CLOCK).
- 32-bit latch data is changed on the negative transition of the LATCH pad and is held on the positive transition.
- The STROBE pad, BEO pad can be used to exercise on/ off control of the output driver.
- Complete separation of logic circuit GND (1 pad) and thermal driver GND (4 pads).
- Maximum ratings of driver output:  $V_O = 28V$ ,  $I_{OL} = 30$ mA.
- Logic unit operating voltage:  $V_{DD} = 4.5$  to 5.5 V.

#### **Package Dimensions**

unit:mm

3057-QIP64A



### **Specifications**

Absolute Maximum Ratings at Ta = 25

	7 - 4	70.0			
Parameter	d	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	- 4	V <sub>DD</sub>		-0.3 to +7.0	V
Input voltage		V <sub>L</sub>		-0.3 to V <sub>DD</sub> +0.3	V
Output voltage		V <sub>O</sub> 1	Sour output	-0.3 to V <sub>DD</sub> +0.3	V
Cutput voltage		V <sub>O</sub> 2	D1/to D32 output, output Tr off	28	V
Output current		lo /	D1 to D32 output, per output	30	mA
Allowable power dissipation	- 4	Pd max	Ta=70°C	450	mW
Operating temperature		Tøpr		-10 to +70	°C
Storage temperature		Tstg		-35 to +125	°C

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#### **LC7935AN**

#### Allowable Operating Conditions at $Ta = -10 \text{ to } +70^{\circ}\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
		Conditions	min	typ	max	Offic
Supply voltage	$V_{DD}$	V <sub>DD</sub>	4.5		5.5	V
H-level input voltage	$v_{IH}$	S <sub>IN</sub> , CLOCK, <u>LATCH</u> , BEO, <u>STROBE</u>	0.8V <sub>DD</sub>	Page 1	$V_{DD}$	V
L-level input voltage	$V_{IL}$	S <sub>IN</sub> , CLOCK, <u>LATCH</u> , BEO, <u>STROBE</u>	V <sub>SS</sub> (L)	Page Town	0.2V <sub>DD</sub>	V
Clock frequency	f <sub>CLK</sub>	CLOCK: Duty: 50%		The state of the s	5.0	MHz
Clock pulse width	tWΦ	CLOCK	75	40.	The state of the s	ns
Clock rise/fall time	t <sub>r,</sub> t <sub>f</sub>	CLOCK	//	1	200	ns
Data setup time	t <sub>DS</sub>	S <sub>IN</sub> , CLOCK	100	100		ns
Data hold time	<sup>t</sup> DH	S <sub>IN</sub> , CLOCK	50			ns
Latch pulse width	tWL	LATCH	100			ns

#### **Electrical Characteristics** at Ta = 25°C

			State 2003	#	A .	
Parameter	Symbol	Conditions		Ratings		Unit
	1		min	typ/	max	
H-level input current	I <sub>IH</sub> 1	S <sub>IN</sub> , CLOCK, LATCH			10	μΑ
	I <sub>IH</sub> 2	BEO	12		72	μΑ
L-level input current	I <sub>IL</sub> 1	S <sub>IN</sub> , CLOCK, LATCH	-10			μA
	I <sub>IL</sub> 2	STROBE	<b>/</b> -72		-12	μA
H-level output voltage	V <sub>OH</sub>	S <sub>OUT</sub> : V <sub>DD</sub> =5V, I <sub>OH</sub> =-0.5mA	/ <sub>DD</sub> -0.5			V
L-level output voltage	V <sub>OL</sub> 1	S <sub>OUT</sub> : V <sub>DD</sub> =5V, I <sub>OL</sub> =0.5mA			0.5	V
	V <sub>OL</sub> 2	D1 to D32: V <sub>DD</sub> =5V, I <sub>QL</sub> =30mA	F		0.5	V
Output OFF-state leakage current	loff	D1 to D32: V <sub>O</sub> =24V			20	μA
Input capacitance	C <sub>IN</sub>	CLOCK		5.0		pF
Operating current drain	I <sub>DD</sub>	V <sub>DD</sub> : V <sub>DD</sub> =5V, f <sub>CLK</sub> =5MHz, All outputs : no load			5	mA

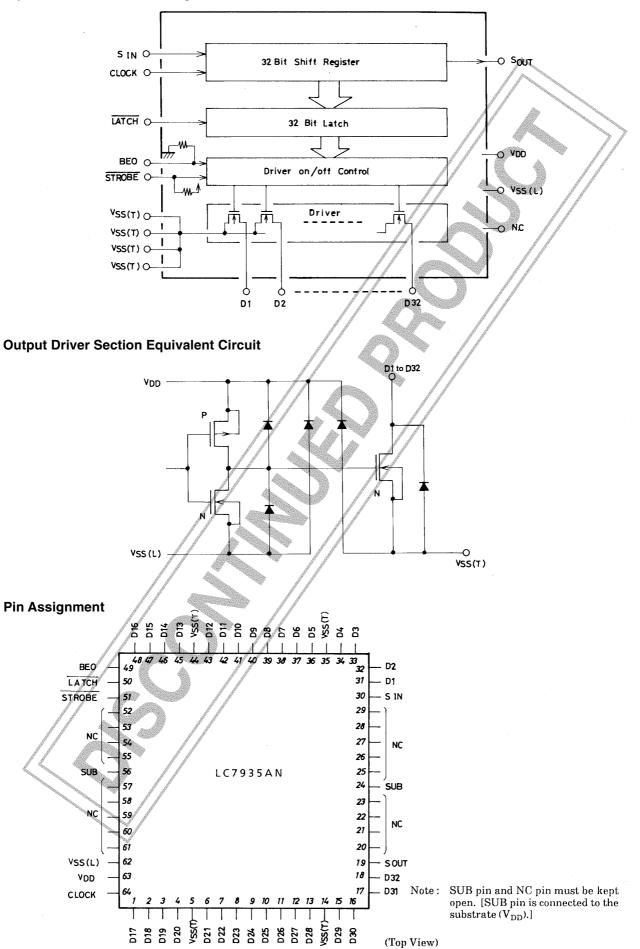
# Switching Characteristics at Ta = 25°C

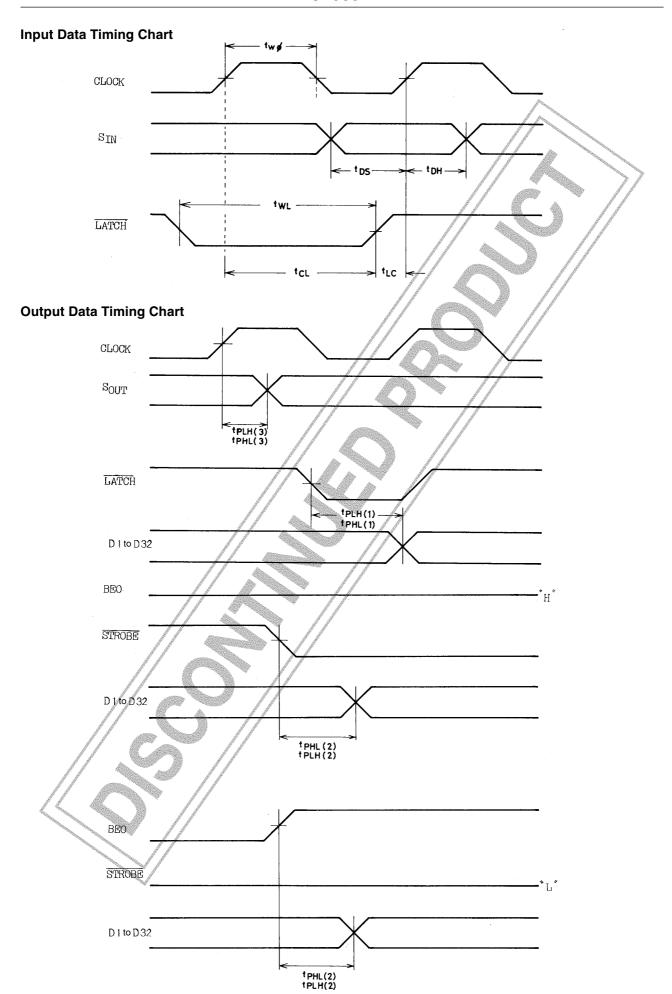
Parameter	Symbol Conditions	Ratings			Unit	
i alametei	Symbol	Conditions	min	typ	max	5,111
Clock latch delay width	//tCL	CLOCK, LATCH: V <sub>DD</sub> =5V	100			ns
Latch clock delay width	/ t <sub>LC</sub>	CLOCK, LATCH: VDD=5V	0			ns
	t <sub>PLH</sub> 1	LATCH, D1 to D32: $V_{DD}$ =5V, Dn: R <sub>L</sub> =1.0k $\Omega$ , C <sub>L</sub> =15pF			400	ns
H-level output propagation delay time	t <sub>PLH</sub> 2	BEQ, STROBE: $V_{DD}$ =5V, Dn: $R_L$ =1.0k $\Omega$ , $C_L$ =15pF			300	ns
	tpLH3	CLOCK, SOUT: VDD=5V, SOUT: CL=15pF			200	ns
	t <sub>PHL</sub> 1	LATCH, D1 to D32: $V_{DD}$ =5V, Dn: $R_L$ =1.0k $\Omega$ , $C_L$ =15pF			200	ns
L-level output propagation delay time	t <sub>PHL</sub> 2	BEO STROBE, D1 to D32: $V_{DD}$ =5V, Dn: $R_L$ =1.0k $\Omega$ , $C_L$ =15pF			100	ns
	t <sub>PHL</sub> 3	CLOCK, S <sub>OUT</sub> : V <sub>DD</sub> =5V, S <sub>OUT</sub> : C <sub>L</sub> =15pF			200	ns

#### Driver ON/OFF Truth Table

Latch Data (Q)	BEO	STROBE	Driver
0//	0	0	OFF
/1/	0 //	0	OFF
0	1//	0	OFF
// 1 //	1/	0	ON Driver on
0	Q	1	OFF
1	0	1	OFF
0	// 1	1	OFF
1	// 1	1	OFF

#### **Equivalent Circuit Block Diagram**







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