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MOSFET - Power, Single N-Channel, LFPAK8 30 V, 0.9 mΩ, 315 A



NTMJS0D9N03CG

Features

- Wide SOA to Improve Inrush Current Management
- Advanced LFPAK Package (5x6mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- These Devices are Pb-Free, Halogen/BFR-Free and are RoHS Compliant

Typical Applications

- Hot Swap Application
- Motor Drive
- Power Load Switch
- Battery Management

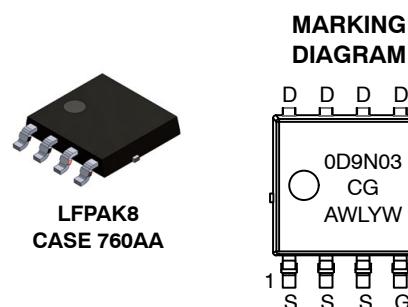
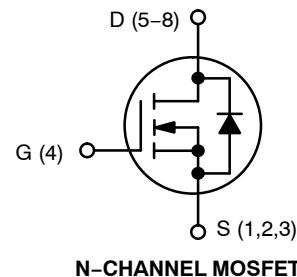
MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	30	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	I_D	315
		$T_C = 100^\circ\text{C}$		223
Power Dissipation $R_{\theta JA}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	P_D	150
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)		$T_A = 25^\circ\text{C}$	I_D	50
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		$T_A = 100^\circ\text{C}$		36
Pulsed Drain Current		$T_A = 25^\circ\text{C}$	P_D	3.9
Operating Junction and Storage Temperature Range		$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM}	900
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 29.2 \text{ A}$)		E_{AS}	556	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using a 1 in², 2 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	0.9 mΩ @ 10 V	315 A



0D9N03CG = Specific Device Code

A = Assembly Location

WL = Wafer Lot

Y = Year

W = Work Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 5 of this data sheet.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	1.0	°C/W
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	39	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250 \mu\text{A}$, ref to 25°C		13		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 30 \text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = 20 \text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 200 \mu\text{A}$	1.3		2.2	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 200 \mu\text{A}$, ref to 25°C		-5.0		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 20 \text{ A}$	0.71	0.9	mΩ
Forward Transconductance	g_{FS}	$V_{DS} = 3 \text{ V}$, $I_D = 20 \text{ A}$		70		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.5		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{iss}	$V_{GS} = 0 \text{ V}$, $V_{DS} = 15 \text{ V}$, $f = 1 \text{ MHz}$		9550		pF
Output Capacitance	C_{oss}			4306		
Reverse Transfer Capacitance	C_{rss}			243		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10 \text{ V}$, $V_{DS} = 15 \text{ V}$; $I_D = 20 \text{ A}$		131.4		nC
Threshold Gate Charge	$Q_{G(TH)}$			14.2		
Gate-to-Drain Charge	Q_{GD}			13.5		
Gate-to-Source Charge	Q_{GS}			24.2		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10 \text{ V}$, $V_{DS} = 15 \text{ V}$, $I_D = 20 \text{ A}$, $R_G = 3 \Omega$		20		ns
Rise Time	t_r			16		
Turn-Off Delay Time	$t_{d(OFF)}$			93		
Fall Time	t_f			24		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0 \text{ V}$, $I_S = 10 \text{ A}$	$T_J = 25^\circ\text{C}$		0.75	1.2	V
			$T_J = 125^\circ\text{C}$		0.60		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0 \text{ V}$, $V_R = 15 \text{ V}$, $I_S = 20 \text{ A}$, $dI_S/dt = 100 \text{ A}/\mu\text{s}$			83		ns
					114		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

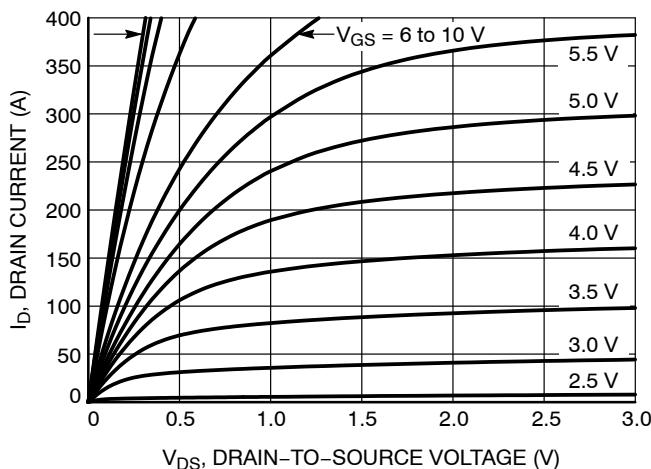


Figure 1. On-Region Characteristics

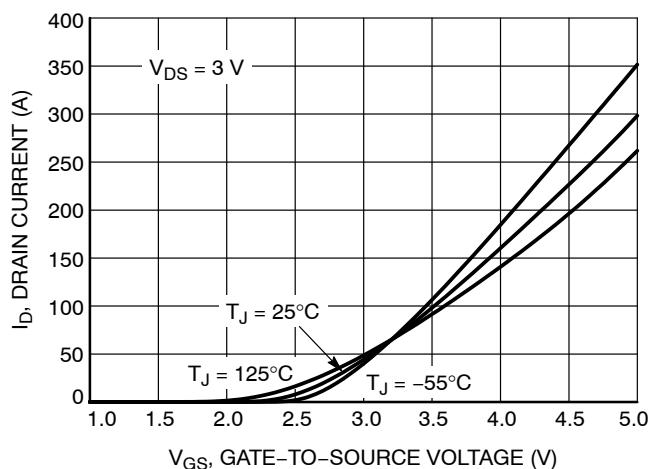


Figure 2. Transfer Characteristics

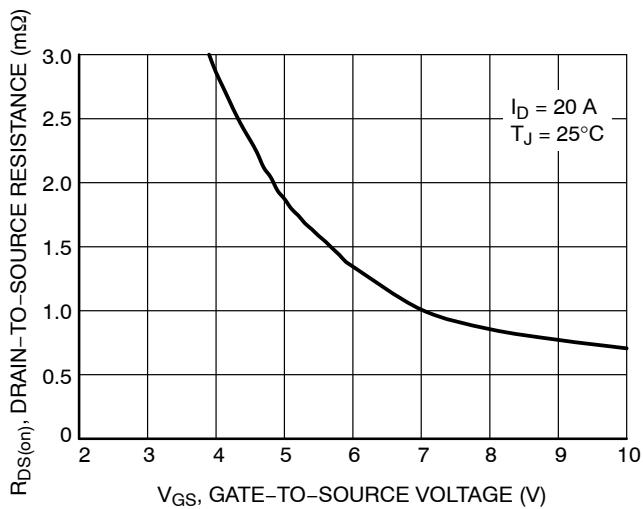


Figure 3. On-Resistance vs. Gate-to-Source Voltage

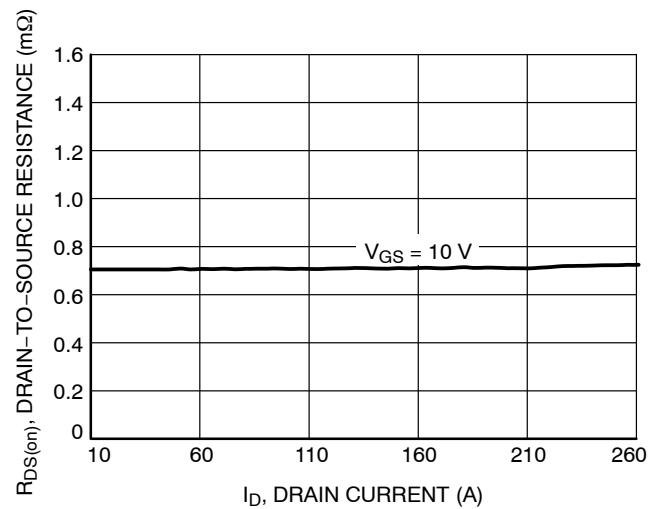


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

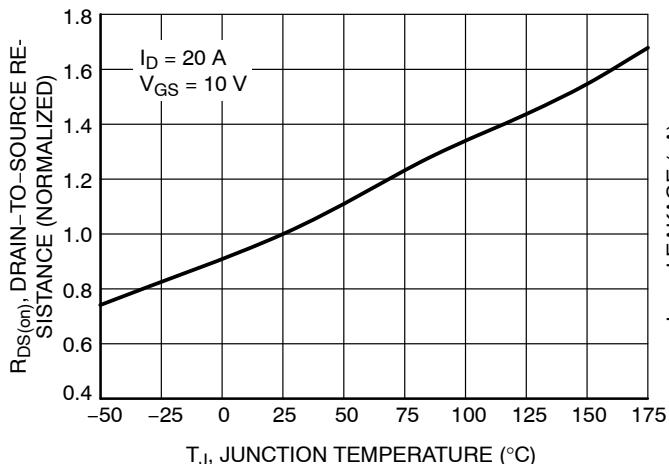


Figure 5. On-Resistance Variation with Temperature

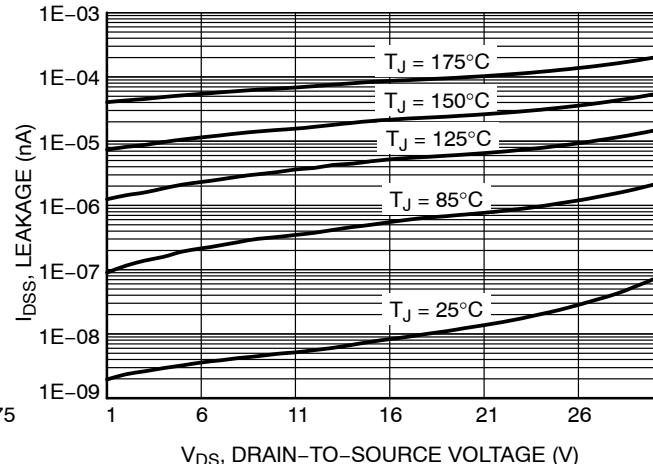


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

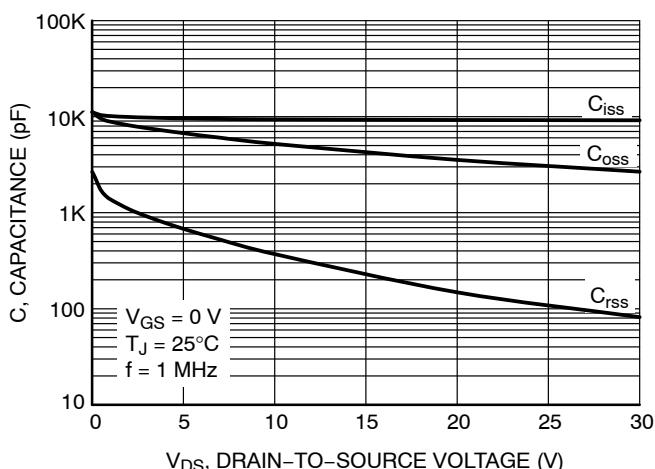


Figure 7. Capacitance Variation

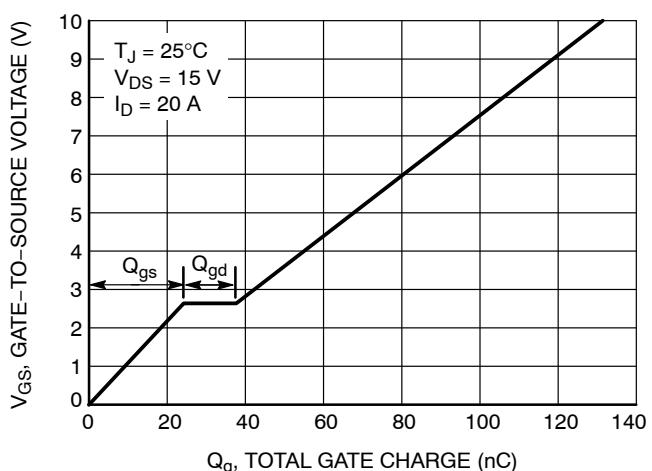


Figure 8. Gate-to-Source vs. Total Charge

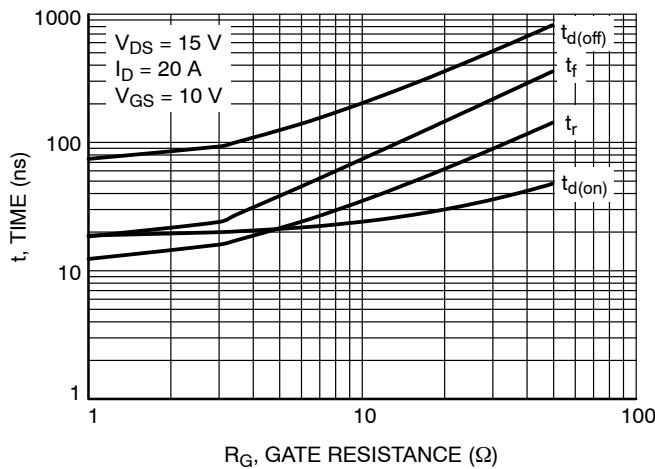


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

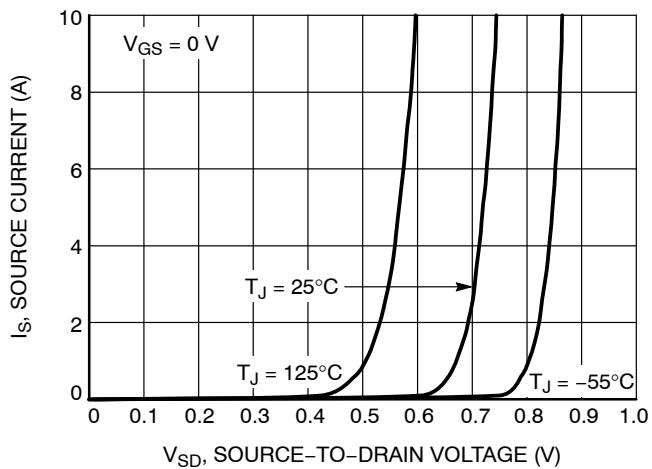


Figure 10. Diode Forward Voltage vs. Current

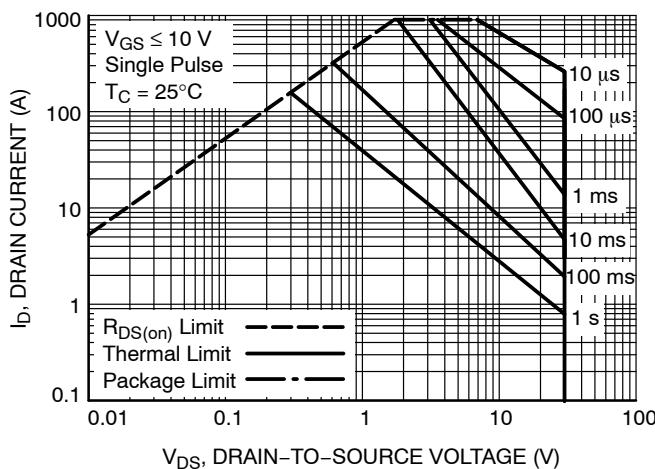


Figure 11. Maximum Rated Forward Biased Safe Operating Area

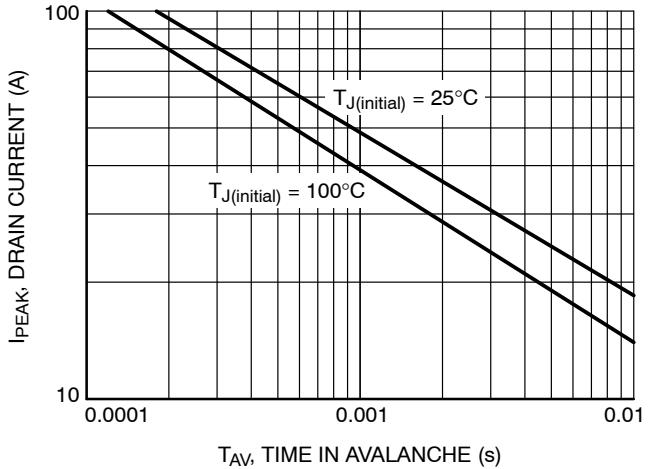


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

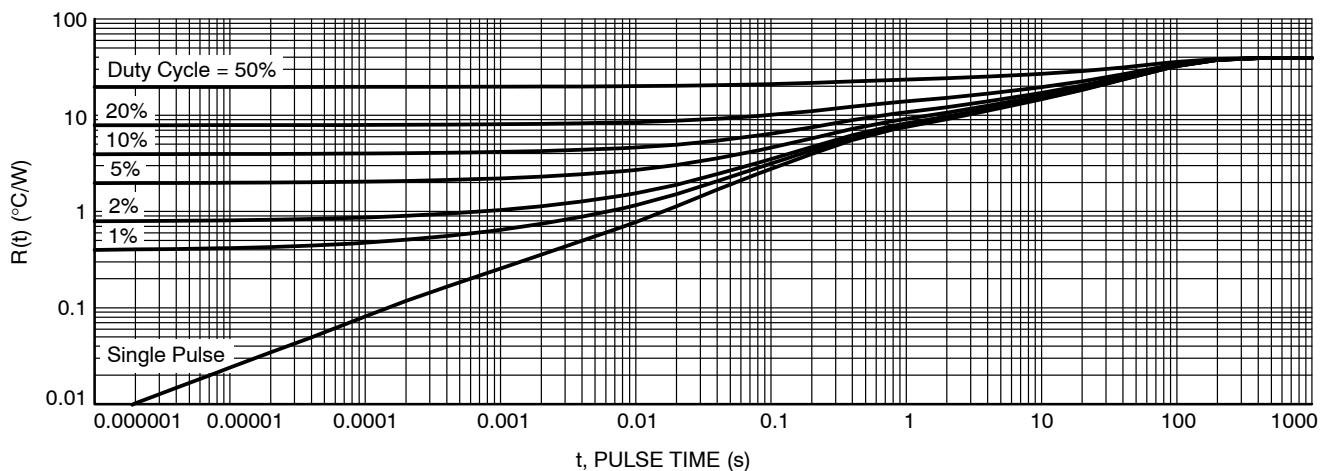


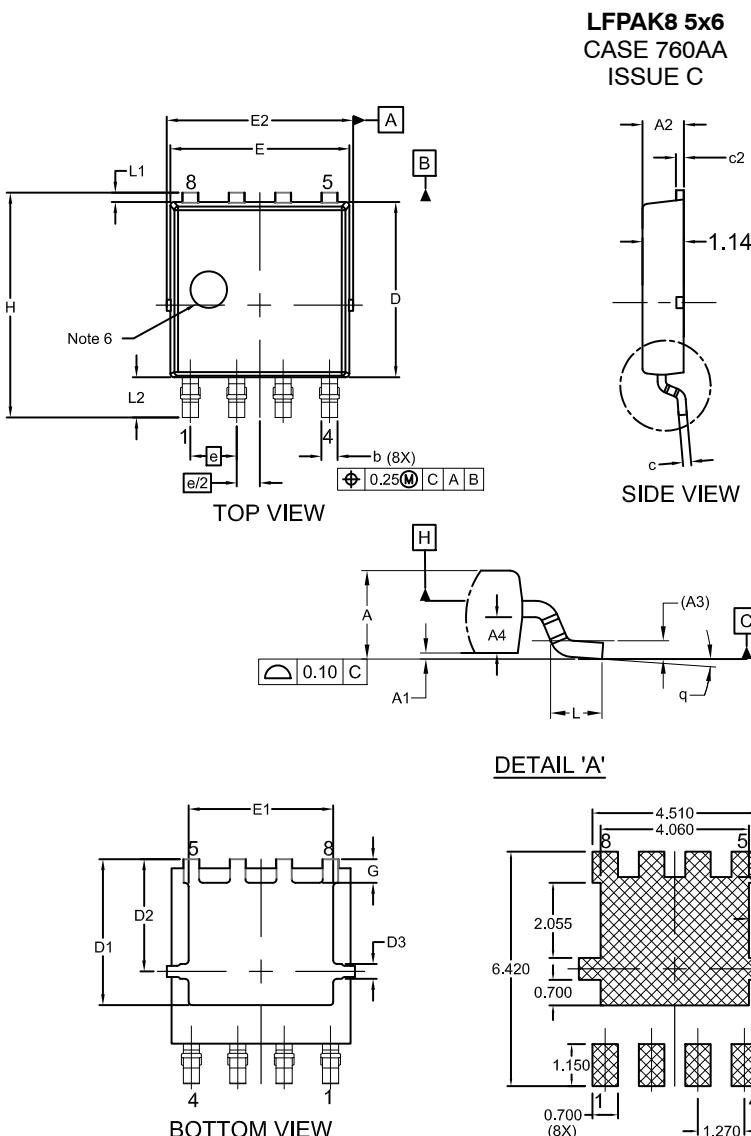
Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NTMJS0D9N03CGTWG	0D9N03 CG	LFPAK8 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS



RECOMMENDED LAND PAD

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
6. OPTIONAL MOLD FEATURE.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25	REF	
A4	0.45	0.50	0.55
b	0.40	0.45	0.50
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	3.00	3.10	3.20
D3	0.30	0.40	0.50
E	4.80	4.90	5.00
E1	3.90	4.00	4.10
E2	5.00	5.15	5.30
e	1.27	BS	C
G	0.55	0.65	0.75
H	6.00	6.15	6.30
L	0.45	0.65	0.85
L1	0.15	0.25	0.35
L2	0.90	1.10	1.30
q	0°	4°	8°

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