To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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# HA16141P/FP, HA16142P/FP

## PFC and PWM Controller

REJ03F0145-0500
(Previous: ADE-204-036D)
Rev.5.00
Jun 15, 2005

## Description

The HA16141P/FP and the HA16142P/FP are power supply controller ICs combining an AC-DC converter switching controllers for power factor correction and off-line power supply switching controllers. PFC (Power factor correction) section employs average current mode PWM and off-line power supply control section employs peak current mode PWM.

The HA16142P/FP is the change version of HA16141P/FP's PWM maximum on duty cycle.

The PFC operation can be turned on and off by external control signal. Use of this on/off function makes it possible to disable PFC operation at a low line voltage, or to perform remote control operation from the transformer secondary side. The PFC power supply boosted output voltage is not only fed to an error amplifier input signal but also fed to as the boost voltage monitor circuit. $\overline{PG}$ signal is put out if the boost voltage is out-of-spec.

The PWM controller, which begins operation at the same time as release of the IC's UVLO (under-voltage lockout) is suitable for auxiliary power supply use in a multi-output power supply system.

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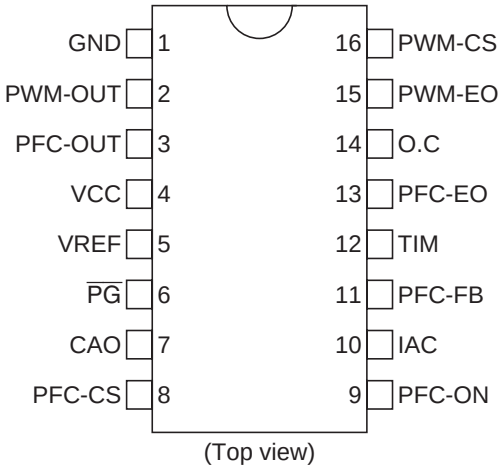
## Features

- Synchronized PFC and PWM timing
- Self oscillation with fixed frequency
  PFC : 100 kHz (±15 %)
  PWM : 200 kHz (±15 %)
- PFC function on/off control
- PFC boosted output voltage monitor
- High-output current gate drivers
  PFC driver peak current : ±1.5 A typ.
  PWM driver peak current : ±1.0 A typ.
- PWM maximum on duty cycle
  72% min (HA16141P/FP)
  49.5% max (HA16142P/FP)

## Pin Arrangement



(Top view)

## Pin Description

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | GND | Ground |
| 2 | PWM-OUT | Power MOS FET driver output (PWM control) |
| 3 | PFC-OUT | Power MOS FET driver output (PFC control) |
| 4 | VCC | Supply voltage |
| 5 | VREF | Reference voltage |
| 6 | $\overline{PG}$ | Power Good signal output (open-drain output) |
| 7 | CAO | Average current control error amp. output |
| 8 | PFC-CS | PFC control current sense signal input |
| 9 | PFC-ON | PFC function on/off signal input |
| 10 | IAC | Multiplier reference current input |
| 11 | PFC-FB | PFC control error amp. input |
| 12 | TIM | Overcurrent timer time setting |
| 13 | PFC-EO | PFC control error amp. output |
| 14 | O.C | Overcurrent detector signal input |
| 15 | PWM-EO | PWM control error amp. output (photocoupler input also possible) (HA16141 only) |
| | | PWM control feedback voltage signal input (HA16142 only) |
| 16 | PWM-CS | PWM control current sense signal input |

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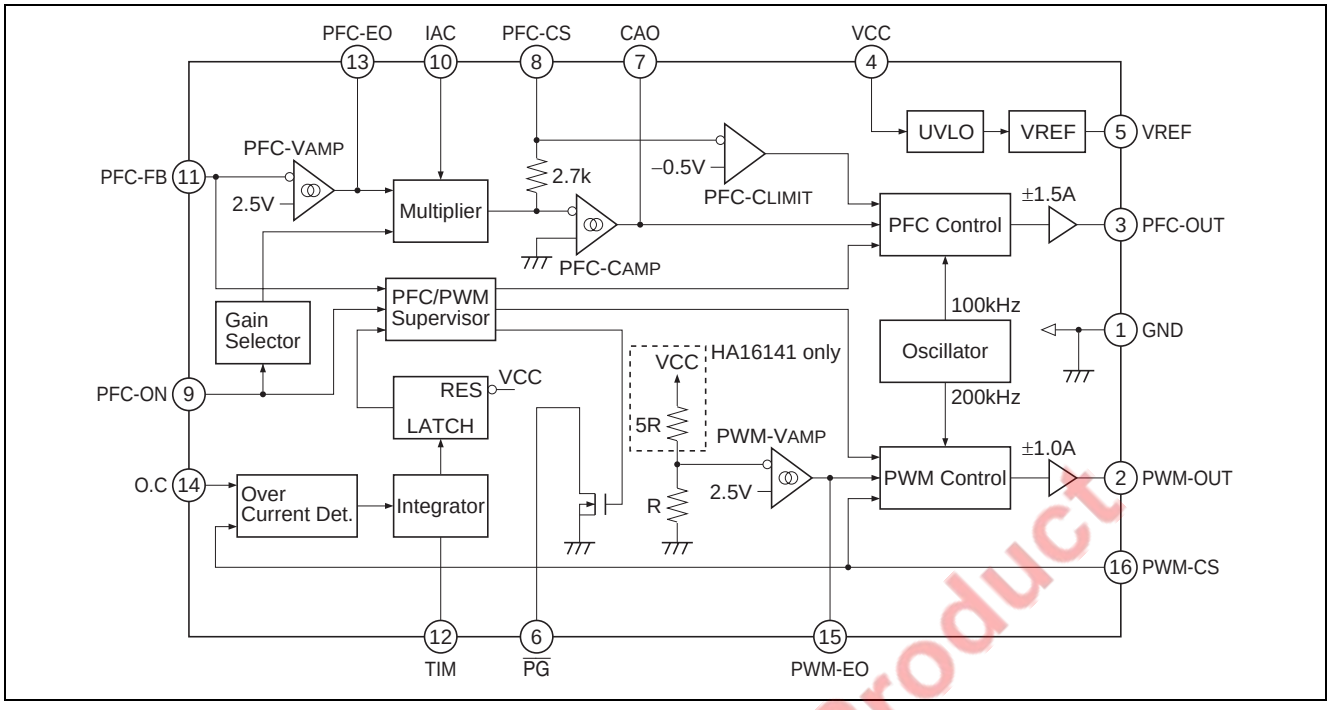
## Block Diagram

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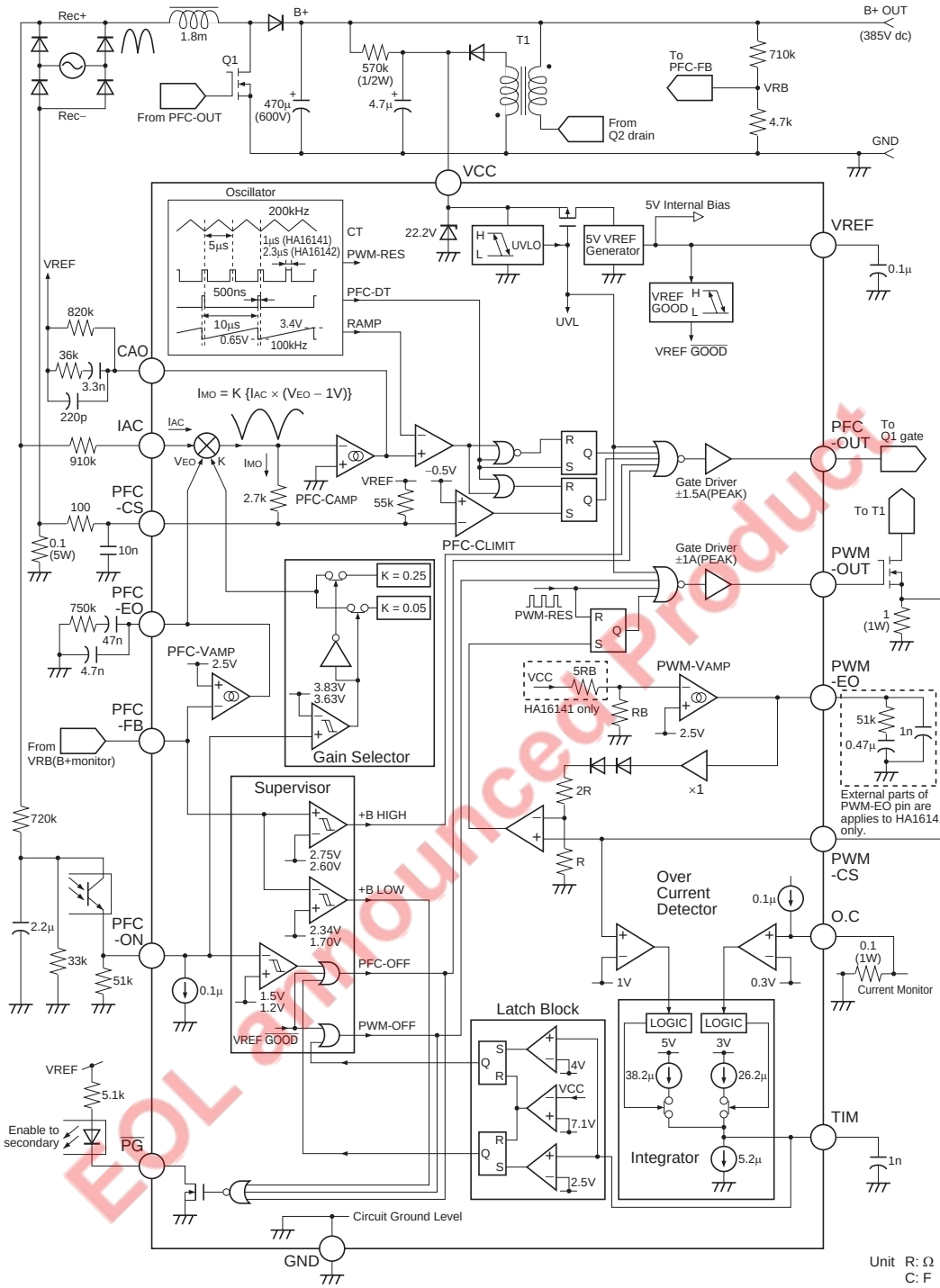
## System Diagram




Note: The constants for the external components are for reference. Please confirm the operation when designing the system.

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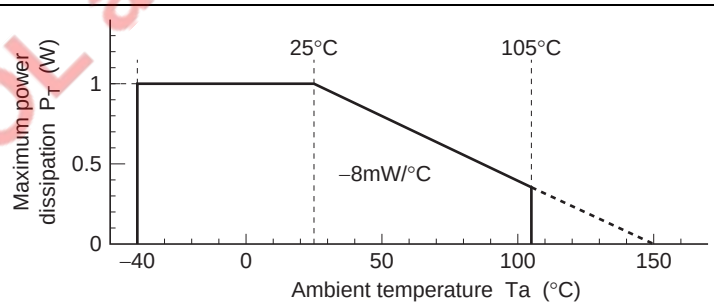
## Absolute Maximum Ratings

(Ta = 25°C)

| Item | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 20 | V | |
| Peak PFC-OUT current | Ipk-pfc | ±1.5 | A | 3 |
| Peak PWM-OUT current | Ipk-pwm | ±1.0 | A | 3 |
| DC PFC-OUT current | Idc-pfc | ±0.15 | A | |
| DC PWM-OUT current | Idc-pwm | ±0.10 | A | |
| Terminal voltage | Vi-group1 | –0.3 to $V_{CC}$ | V | 4 |
| | Vi-group2 | –0.3 to Vref | V | 5 |
| CAO voltage | Vcao | –0.3 to Veoh-ca | V | |
| PFC-EO voltage | Vpfc-eo | –0.3 to Veoh-pfc | V | |
| PWM-EO voltage | Vpwm-eo | –0.3 to Veoh-pwm | V | |
| PFC-ON voltage | Vpfc-on | –0.3 to +7 | V | |
| IAC voltage | Vi-ac | –0.3 to +5 | V | |
| IAC current | Ii-ac | 0.8 | mA | |
| PFC-CS voltage | Vi-cs | –1.5 to +0.3 | V | |
| TIM voltage | Vi-tim | –0.3 to +6 | V | |
| VREF current | Io-ref | –20 | mA | |
| $\overline{PG}$ voltage | Vo-pg | –0.3 to +7 | V | |
| $\overline{PG}$ current | Io-pg | 15 | mA | |
| Power dissipation | $P_T$ | 1 | W | 6 |
| Operating temperature | Topr | –40 to +105 | °C | |
| Storage temperature | Tstg | –55 to +150 | °C | |
| Junction temperature | Tj | 150 | °C | |

Notes:
1. Rated voltages are with reference to the GND pin.
2. For rated currents, inflow to the IC is indicated by (+), and outflow by (–).
3. Shows the transient current when driving a capacitive load.
4. Group1 is the rated voltage for the following pins: PFC-OUT, PWM-OUT
5. Group2 is the rated voltage for the following pins: VREF, PFC-FB, PWM-CS
6. This is the value when the ambient temperature (Ta) is 25°C or below. If Ta exceeds 25°C, the graph below applies. For the SOP package, this value is based on actual measurements on a 10% wiring density glass epoxy circuit board (40 mm × 40 mm × 1.6 mm).

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## Electrical Characteristics

(Ta = 25°C, $V_{CC}$ = 14 V)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Supply | Start threshold | $V_H$ | 12.2 | 13.0 | 13.8 | V | |
| | Shutdown threshold | $V_L$ | 9.4 | 10.0 | 10.6 | V | |
| | UVLO hysteresis | $dV_{UVL}$ | 2.6 | 3.0 | 3.4 | V | |
| | Start-up current | $I_S$ | 150 | 200 | 300 | µA | $V_{CC}$ = 12V |
| | Is temperature stability | $dI_S/dTa$ | – | –0.3 | – | %/°C | *1 |
| | Operating current | $I_{CC}$ | 4 | 7 | 9 | mA | IAC = 100µA, $C_L$ = 0F |
| | Latch current | $I_{LATCH}$ | 230 | 310 | 375 | µA | $V_{CC}$ = 9V |
| | Shunt zener voltage | $V_Z$ | 21.2 | 22.2 | 23.2 | V | $I_{CC}$ = 14mA |
| | Vz temperature stability | $dV_Z/dTa$ | – | +4 | – | mV/°C | $I_{CC}$ = 14mA *1 |
| PFC-OUT | Minimum duty cycle | Dmin-pfc | – | – | 0 | % | CAO = 3.6V |
| | Maximum duty cycle | Dmax-pfc | 90 | 95 | 98 | % | CAO = 0V |
| | Rise time | $t_r$-pfc | – | 30 | 100 | ns | $C_L$ = 1000p |
| | Fall time | $t_f$-pfc | – | 30 | 100 | ns | $C_L$ = 1000p |
| | Peak current | Ipk-pfc | – | 1.5 | – | A | $C_L$ = 0.01µF *1 |
| | Low voltage | Vol1-pfc | – | 0.05 | 0.2 | V | Iout = 20mA |
| | | Vol2-pfc | – | 0.35 | 1.4 | V | Iout = 200mA |
| | | Vol3-pfc | – | 0.03 | 0.7 | V | Iout = 10mA, $V_{CC}$ = 5V |
| | High voltage | Voh1-pfc | 13.5 | 13.9 | – | V | Iout = –20mA |
| | | Voh2-pfc | 12.6 | 13.3 | – | V | Iout = –200mA |
| PWM-OUT | Minimum duty cycle | Dmin-pwm | – | – | 0 | % | PWM-EO = 1.3V<br>PWM-CS = 0V |
| | Maximum duty cycle | Dmax-pwm | 72 | 80 | 88 | % | PWM-EO = 5V<br>PWM-CS = 0V *2 |
| | | | 42.5 | 46 | 49.5 | % | PWM-EO = 5V<br>PWM-CS = 0V *3 |
| | Rise time | $t_r$-pwm | – | 30 | 100 | ns | $C_L$ = 1000p |
| | Fall time | $t_f$-pwm | – | 30 | 100 | ns | $C_L$ = 1000p |
| | Peak current | Ipk-pwm | – | 1.0 | – | A | $C_L$ = 0.01µF *1 |
| | Low voltage | Vol1-pwm | – | 0.05 | 0.2 | V | Iout = 20mA |
| | | Vol2-pwm | – | 0.5 | 2.0 | V | Iout = 200mA |
| | | Vol3-pwm | – | 0.03 | 0.7 | V | Iout = 10mA, $V_{CC}$ = 5V |
| | High voltage | Voh1-pwm | 13.5 | 13.9 | – | V | Iout = –20mA |
| | | Voh2-pwm | 12.0 | 13.0 | – | V | Iout = –200mA |
| VREF | Output voltage | Vref | 4.9 | 5.0 | 5.1 | V | Isource = 1mA |
| | Line regulation | Vref-line | – | 5 | 20 | mV | Isource = 1mA<br>$V_{CC}$ = 12V to 18V |
| | Load regulation | Vref-load | – | 5 | 20 | mV | Isource = 1mA to 20mA |
| | Temperature stability | dVref | – | 80 | – | ppm/°C | Ta = –40 to 105°C *1 |

Notes: 1. Design spec.
2. Apply to HA16141.
3. Apply to HA16142.

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## Electrical Characteristics (cont.)

(Ta = 25°C, $V_{CC}$ = 14 V)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Oscillator | Initial accuracy | fpwm | 170 | 200 | 230 | kHz | Measured pin: PWM-OUT |
| | | fpfc | 85 | 100 | 115 | kHz | Measured pin: PFC-OUT |
| | fpwm temperature stability | dfpwm/dTa | – | ±0.1 | – | %/°C | Ta = –40 to 105°C *1 |
| | fpwm voltage stability | fpwm(line) | –1.5 | +0.5 | +1.5 | % | $V_{CC}$ = 12V to 18V |
| | Ramp peak voltage | Vramp-H | – | 3.4 | 3.6 | V | |
| | Ramp valley volatge | Vramp-L | – | 0.65 | – | V | *1 |
| PFC-ON | PFC on voltage | Von-pfc | 1.3 | 1.5 | 1.7 | V | |
| | PFC off voltage | Voff-pfc | 1.0 | 1.2 | 1.4 | V | |
| | PFC on-off hysteresis | dVon-off | 0.15 | 0.30 | 0.45 | V | |
| | Input current | Ipfc-on | – | 0.1 | 1.0 | µA | PFC-ON = 2V |
| Supervisor/ $\overline{PG}$ | PFC GOOD threshold voltage | Vb-good | 2.29 | 2.34 | 2.39 | V | Input pin: PFC-FB |
| | PFC FAIL threshold voltage | Vb-fail | 1.66 | 1.70 | 1.74 | V | Input pin: PFC-FB |
| | +B High PFC inhibit voltage | Vb-h | 2.69 | 2.75 | 2.81 | V | Input pin: PFC-FB |
| | +B High PFC restart voltage | Vb-res | 2.54 | 2.60 | 2.66 | V | Input pin: PFC-FB |
| | $\overline{PG}$ leak current | Ioff-pg | – | 0.001 | 1.0 | µA | $\overline{PG}$ = 5V |
| | $\overline{PG}$ shunt current | Ion-pg | 5 | 15 | – | mA | $\overline{PG}$ = 3V *2 |
| | Delay to $\overline{PG}$ | tg-pg | – | 0.2 | 1 | µs | Step signal (5 to 0V) to PFC-ON |
| O.C (Over Current Detector) | O.C threshold voltage | $V_{OC}$ | 0.27 | 0.30 | 0.33 | V | |
| | PWM-CS threshold voltage | $V_{CS}$ | 0.9 | 1.0 | 1.1 | V | |
| | O.C input current | $I_{OC}$ | – | –0.1 | –1.0 | µA | O.C = 0V |
| Integrator | Sink current | Isnk-tim | 3.9 | 5.2 | 6.5 | µA | TIM = 2V |
| | Source current O.C trigger | Isrc-tim1 | –16 | –21 | –26 | µA | TIM = 2V, O.C = 0.5V *1 |
| | Source Current PWM-CS trigger | Isrc-tim2 | –25 | –33 | –41 | µA | TIM = 2V, PWM-CS = 2V *1 |
| | Integrated time O.C trigger | t-tim1 | 88 | 110 | 132 | µs | Step signal (0 to 1V) to O.C, Ctim = 1000p, Measured pin: $\overline{PG}$ |
| | Integrated Time PWM-CS trigger | t-tim2 | 53 | 67 | 81 | µs | Step signal (0 to 2V) to PWM-CS, Ctim = 1000p, Measured pin: $\overline{PG}$ |

Notes: 1. Design spec.
2. Maximum rating of PG current is 15 mA. Use series resistor to limit PG current lower than 15 mA.

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## Electrical Characteristics (cont.)

(Ta = 25°C, $V_{CC}$ = 14 V)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| Latch | Threshold voltage for PFC stop | Vlch-pfc | 2.4 | 2.5 | 2.6 | V | Input pin: TIM |
| | Threshold Voltage for PWM stop | Vlch-sys | 3.8 | 4.0 | 4.2 | V | Input pin: TIM |
| | Latch Reset Voltage | Vcc-res | 6.1 | 7.1 | 8.1 | V | |
| PWM-$V_{AMP}$ | Feedback $V_{CC}$ voltage | Vfb-pwm | 14.2 | 14.8 | 15.4 | V | PWM-EO = 2.5V *2 |
| | Open loop gain | Av-pwm | – | 45 | – | dB | *1, *2 |
| | High voltage | Veoh-pwm | 5.1 | 5.7 | 6.3 | V | $V_{CC}$ = 14V, PWM-EO: Open |
| | Low voltage | Veol-pwm | – | 0.1 | 0.3 | V | $V_{CC}$ = 16V, PWM-EO: Open *2 |
| | Source current | Isrc-pwm | – | –77 | – | µA | *1 $V_{CC}$ = 11V |
| | Sink current | Isnk-pwm | – | 77 | – | µA | *1 $V_{CC}$ = 18V *2 |
| | Transconductance respect to $V_{CC}$ | Gm-pwm | 19 | 27 | 35 | µA/V | $V_{CC}$ = 15V, PWM-EO = 2.5V *2 |
| PWM current sense | Delay to output | td-cs | – | 210 | 300 | ns | PWM-EO = 5V, PWM-CS = 0 to 2V |
| PFC current limit | Threshold voltage | $V_{LM}$ | –0.47 | –0.50 | –0.53 | V | |
| | Delay to output | td-$_{LM}$ | – | 280 | 500 | ns | PFC-CS = 0 to –1V |
| PFC-$V_{AMP}$ | Feedback voltage | Vfb-pfc | 2.45 | 2.50 | 2.55 | V | PFC-EO = 2.5V |
| | Input bias current | Ifb-pfc | –0.30 | –0.07 | +0.30 | µA | Measured pin: PFC-FB |
| | Open loop gain | Av-pfc | – | 65 | – | dB | *1 |
| | High voltage | Veoh-pfc | 5.1 | 5.7 | 6.3 | V | PFC-FB = 2.3V, PFC-EO: Open |
| | Low voltage | Veol-pfc | – | 0.1 | 0.3 | V | PFC-FB = 2.7V, PFC-EO: Open |
| | Source current | Isrc-pfc | –62 | –77 | –93 | µA | PFC-FB = 1.0V, PFC-EO = 2.5V |
| | Sink current | Isnk-pfc | 62 | 77 | 93 | µA | PFC-FB = 4.0V, PFC-EO = 2.5V |
| | Transconductance | Gm-pfcv | 120 | 160 | 200 | µA/V | PFC-FB = 2.5V, PFC-EO = 2.5V |

Notes: 1. Design spec.
2. Apply to HA16141.

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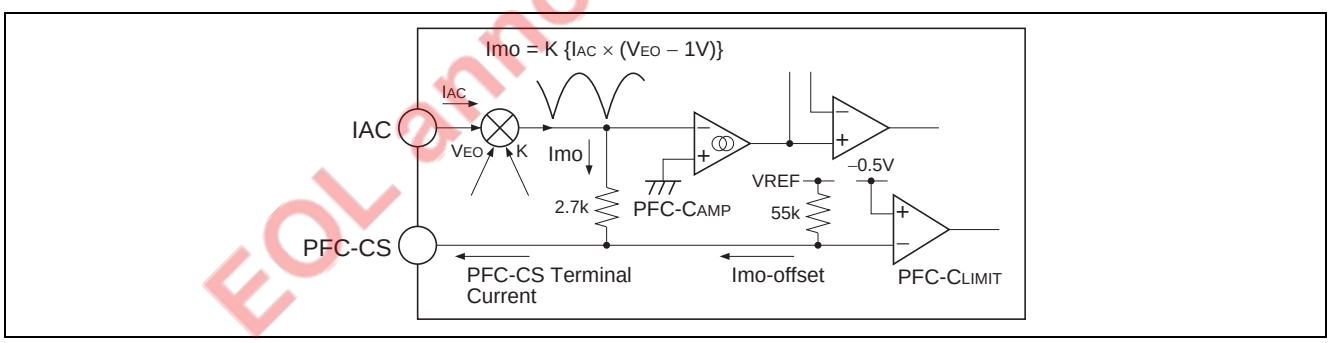
## Electrical Characteristics (cont.)

(Ta = 25°C, $V_{CC}$ = 14 V)

| Item | | Symbol | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| PFC-CAMP | Input offset voltage | Vio-ca | – | ±7 | – | mV | *1 |
| | Open loop gain | Av-ca | – | 65 | – | dB | *1 |
| | High voltage | Veoh-ca | 5.1 | 5.7 | 6.3 | V | |
| | Low voltage | Veol-ca | – | 0.1 | 0.3 | V | |
| | Source current | Isrc-ca | – | –77 | – | µA | CAO = 2.5V *1 |
| | Sink current | Isnk-ca | – | 77 | – | µA | CAO = 2.5V *1 |
| | Transconductance | Gm-pfcc | 120 | 160 | 200 | µA/V | *1 |
| IAC/ Multiplier | IAC PIN voltage | Viac | 0.7 | 1.0 | 1.3 | V | IAC = 100µA |
| | Terminal offset current | Imo-offset | –56 | –75 | –94 | µA | IAC = 0A, PFC-CS = 0V, Measured pin: PFC-CS |
| | Output current (PFC-ON = 3.4V) | Imo1 | – | –25 | – | µA | PFC-EO = 2V, IAC = 100µA *1, *2 |
| | | Imo2 | – | –75 | – | µA | PFC-EO = 4V, IAC = 100µA *1, *2 |
| | Output current (PFC-ON = 3.9V) | Imo3 | – | –5 | – | µA | PFC-EO = 2V, IAC = 100µA *1, *2 |
| | | Imo4 | – | –15 | – | µA | PFC-EO = 4V, IAC = 100µA *1, *2 |
| | PFC-CS resistance | Rmo | – | 2.7 | – | kΩ | *1 |
| Gain selector | Threshold voltage for K = 0.05 | $V_{K-H}$ | 3.71 | 3.83 | 3.95 | V | |
| | Threshold voltage for K = 0.25 | $V_{K-L}$ | 3.51 | 3.63 | 3.75 | V | |
| | $V_K$ hysteresis voltage | $dV_K$ | 0.15 | 0.20 | 0.25 | V | *1 |

Notes: 1. Design spec.
2. Imo1 to Imo4 are defined as,
Imo = (PFC-CS Terminal Current) – (Imo-offset)

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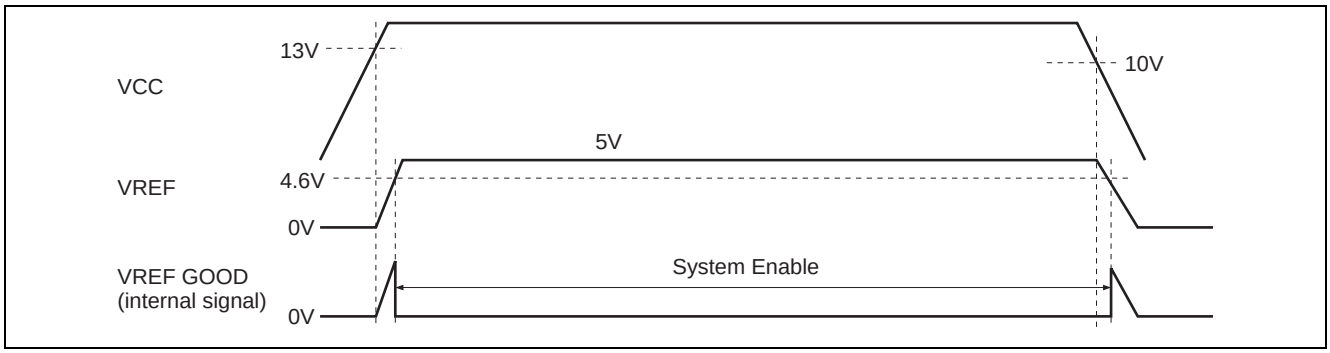
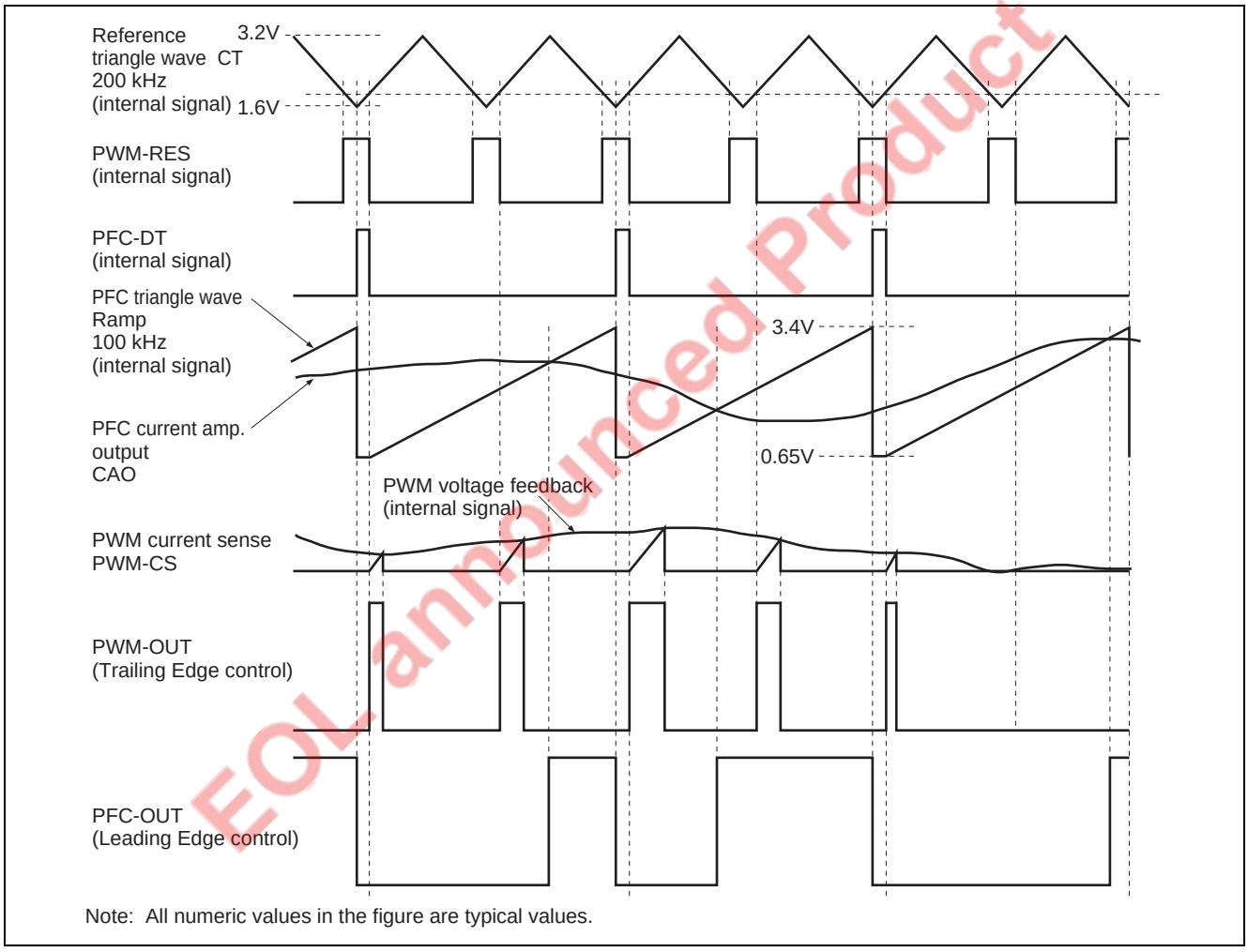
## Internal Timing

1. UVLO




2. Oscillator, Gate driver output




Note: All numeric values in the figure are typical values.

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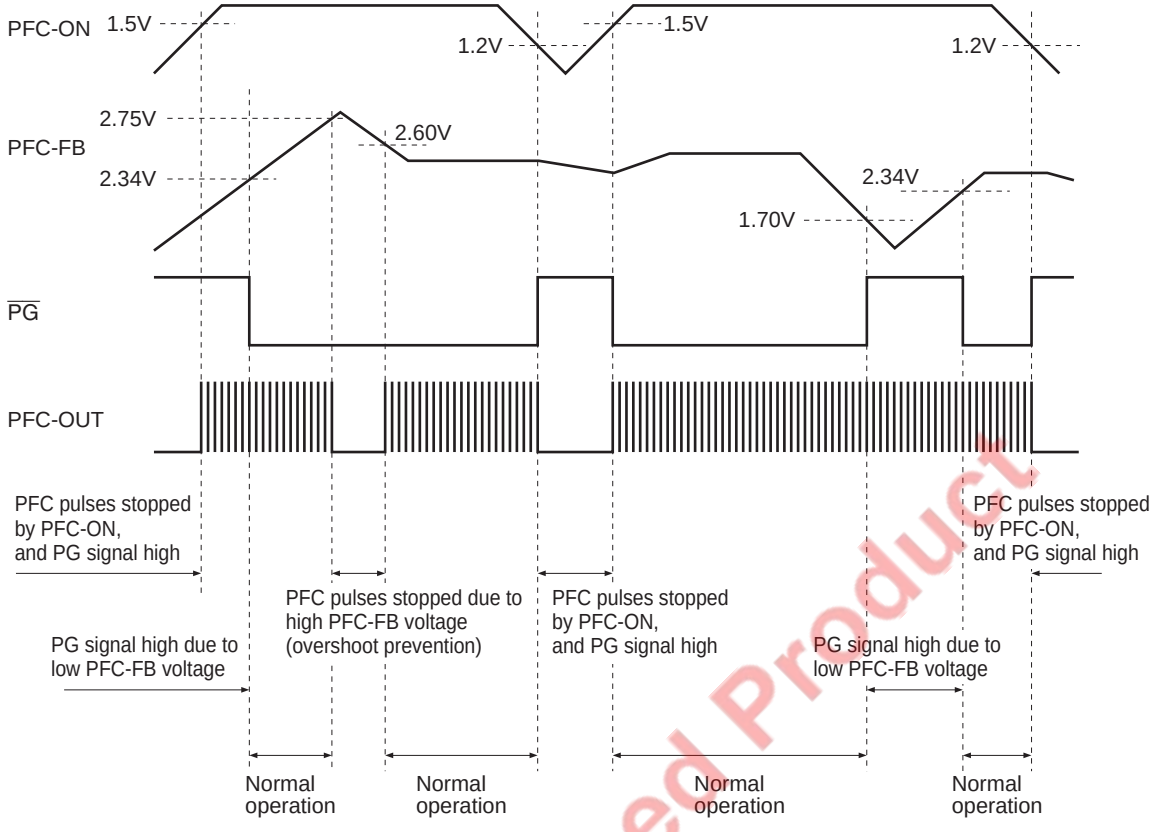
3. PFC controller status

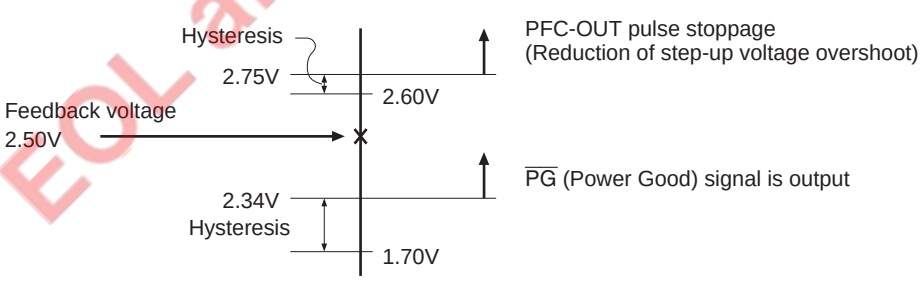
Precondition: VREF GOOD, Non latched.




Notes: 1. All numeric values in the figure are typical values.

2. PFC-ON
The HA16141P/FP can perform on/off control of the PFC function using the PFC-ON pin.
If an AC voltage that has undergone primary rectification and has been divided with an external resistance is input, PFC stoppage is possible in the event of a low input voltage.
On/off control by means of a logic signal is also possible.

3. PFC-FB
The input to this pin is the voltage obtained by dividing the stepped-up PFC output voltage.
The pin voltage is fed back to the PFC control system, and is also used for step-up voltage logic decisions.
This is outlined in the figure below.

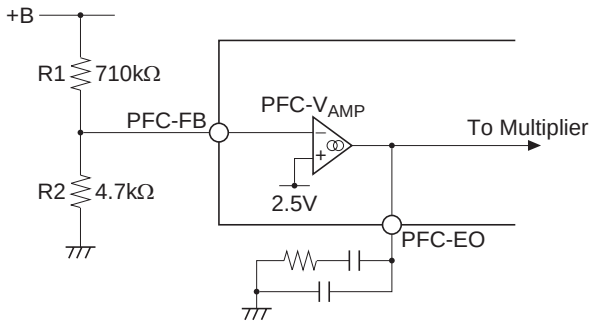



(Note 3 is continued on the next page)

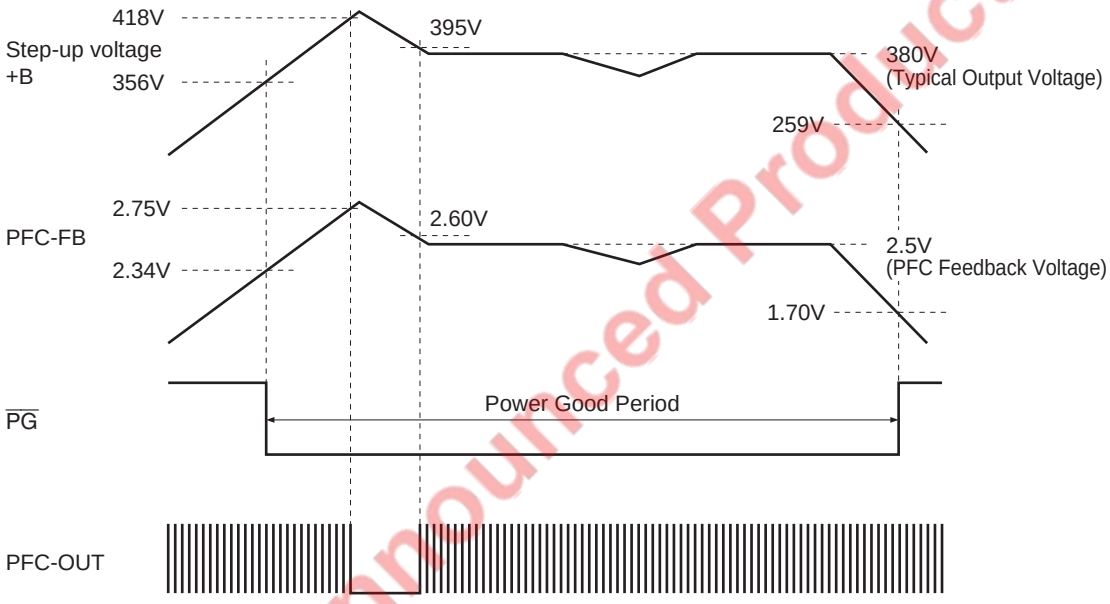
EOL announced Product

3. PFC controller status (cont.)

Notes: 3. PFC-FB (cont.)
The actual input voltage to the PFC-FB pin is the step-up voltage divided with a resistance (see figure below).
If R1 is set as 710 kΩ and R2 as 4.7 kΩ, the decision voltage at the step-up pin (+B) is as shown in the figure below.




Precondition: VREF GOOD, PFC-ON, Non latched.




Notes: 4. All numeric values in the figure are typical values.

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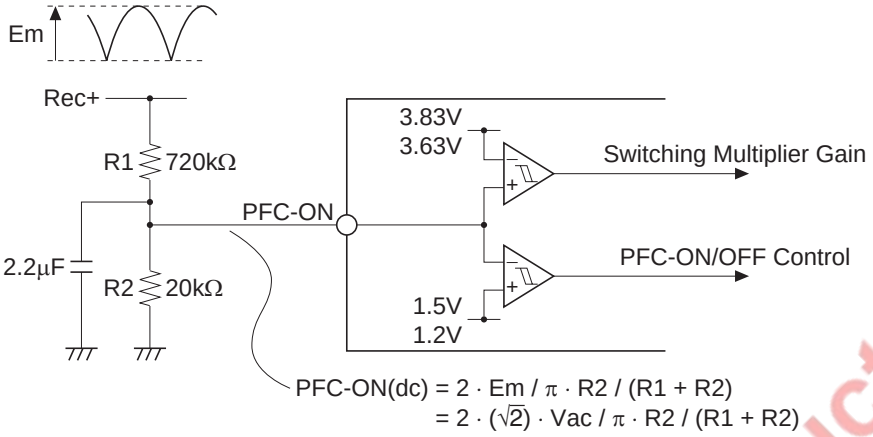
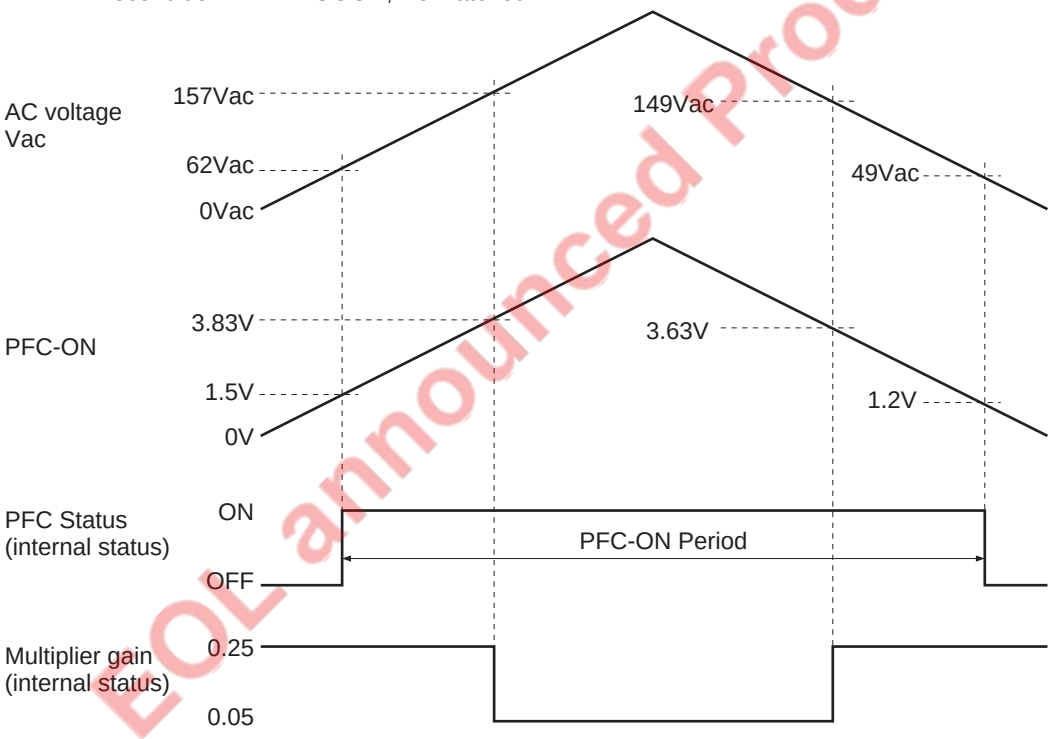
4. PFC-ON pin

The following functions are effected by inputting an AC voltage that has undergone primary rectification and has been divided with an external resistance to the PFC-ON pin (see figure below).
a) Turning PFC operation off when AC voltage is low
b) Switching multiplier gain with AC 100 V system and 200 V system input




PFC-ON(dc) = 2 · Em / π · R2 / (R1 + R2)
= 2 · (√2) · Vac / π · R2 / (R1 + R2)

Precondition: VREF GOOD, Non latched.

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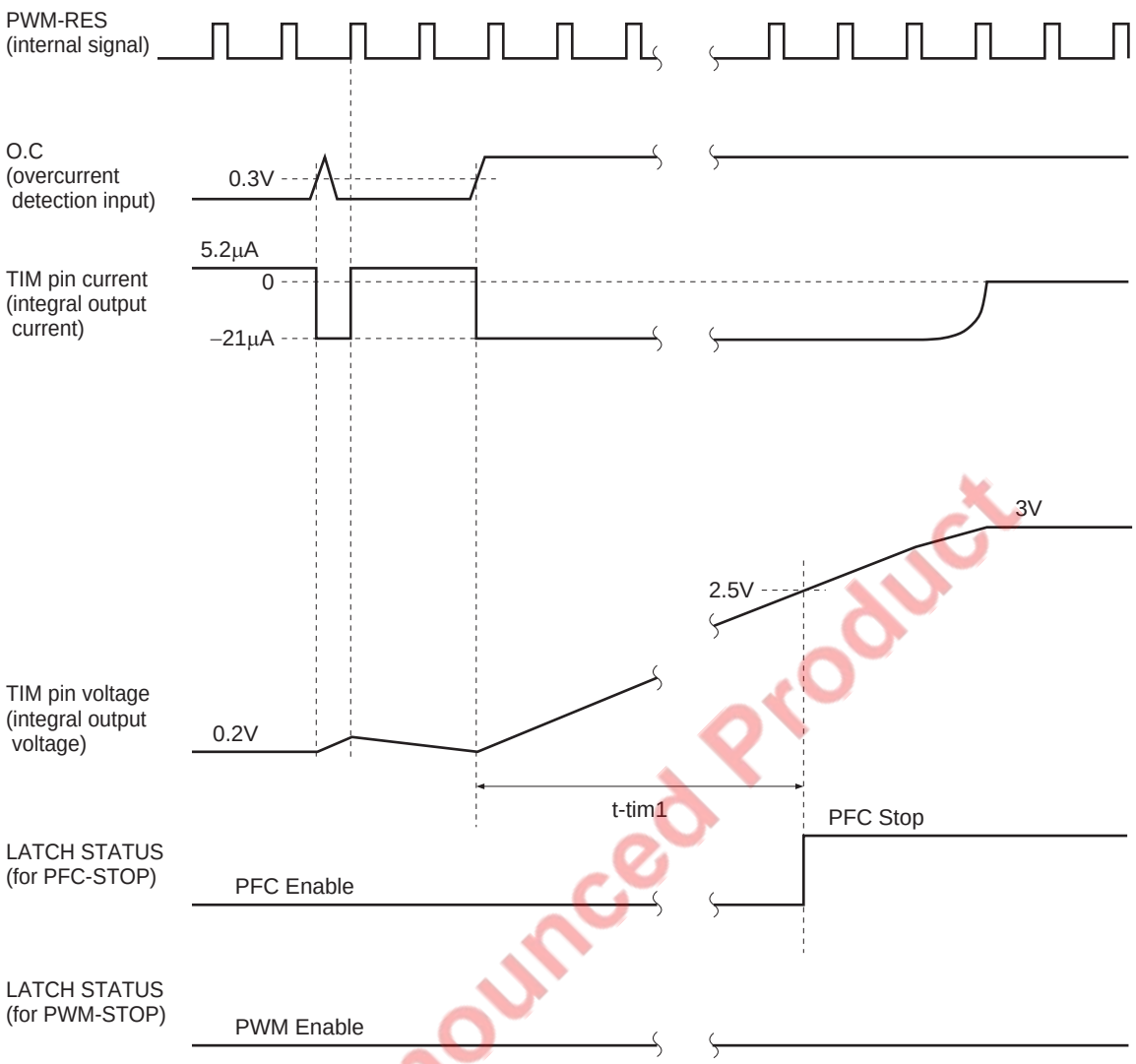
Note: All numeric values in the figure are typical values.

5. Integrator (OC detection operation)



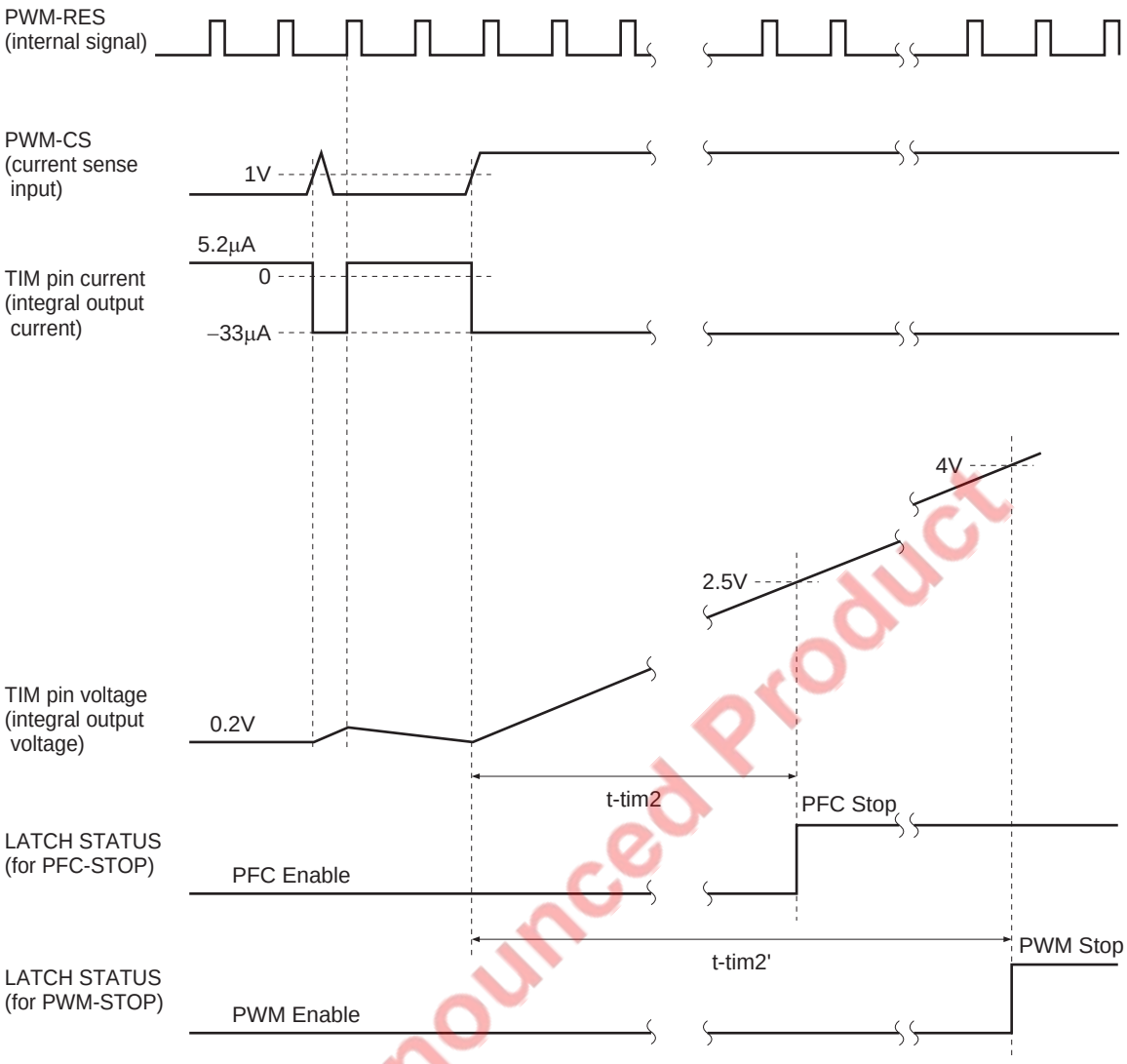

Note: Timer time calculation equation

Timer time t-tim1 is the time until PG pin inversion (from low to high) after the O.C pin trigger. t-tim1 can be set using the following approximate equation.

t-tim1 = –Ctim · (Vlch – pfc – 0.2V) / Isrc – tim1
= –Ctim · (2.5V – 0.2V) / (–21μA) · · · · · Typical calculation

EOL announced Product

6. Integrator (PWM-CS detection operation)




Pre-announced Product

Note: Timer time calculation equation

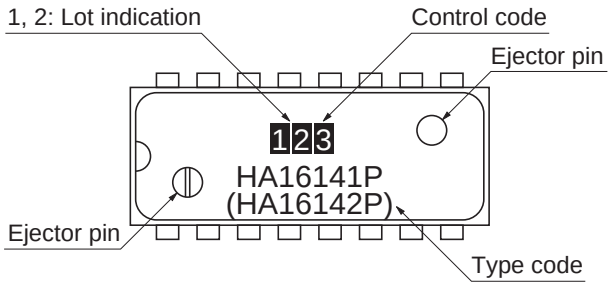
Timer time t-tim2 is the time until PG pin inversion (from low to high) after the PWM-CS pin trigger. t-tim2 can be set using the following approximate equation.

t-tim2 = –Ctim · (Vlch – pfc – 0.2V) / Isrc – tim2
= –Ctim · (2.5V – 0.2V) / (–33μA) · · · · · Typical calculation

The time at which both the PFC and PWM functions are stopped by this timer can be calculated using the following approximate equation.

t-tim2' = 1.65 · t – tim2 · · · · · Typical calculation

## Mark Pattern




Notes: 1. Example of lot indication.

For example, a product manufactured in May 2000 has the markings "0E" in positions 1 2 in the above figure.

| Production | | Indication | |
|---|---|---|---|
| Month | Year | 1 | 2 |
| May | 2000 | 0 | E |

| Month | Jan | Feb | Mar | Apr | May | Jun | Jul | Aug | Sep | Oct | Nov | Dec |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Code | A | B | C | D | E | F | G | H | J | K | L | M |

2. Laser marking is used.

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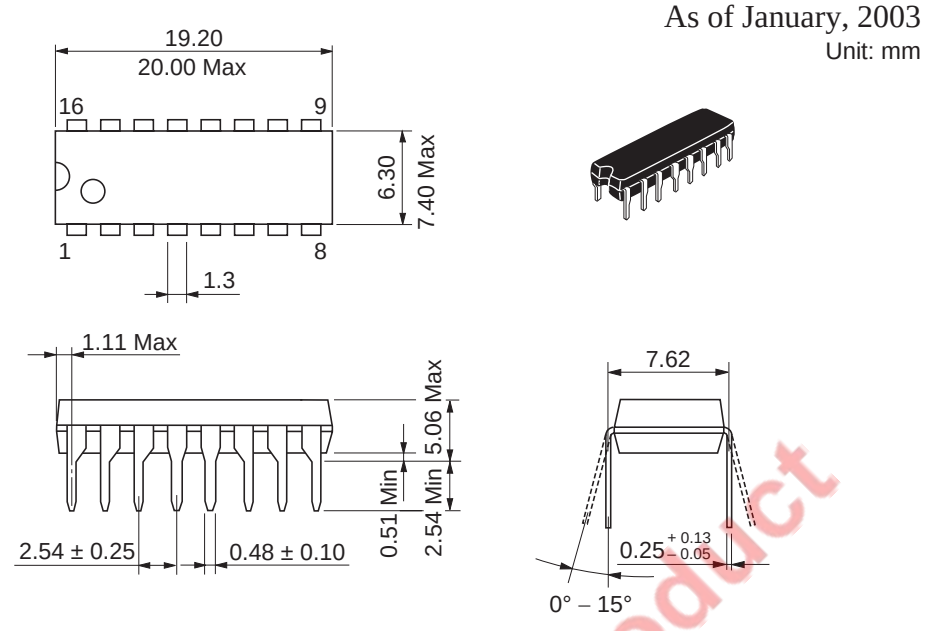
## Package Dimensions

As of January, 2003

Unit: mm




| | |
|---|---|
| Package Code | DP-16 |
| JEDEC | Conforms |
| JEITA | Conforms |
| Mass (reference value) | 1.07 g |

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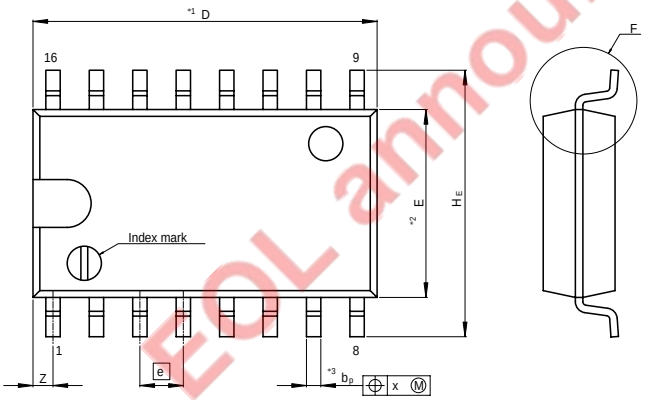
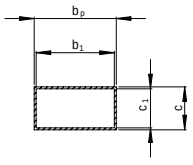
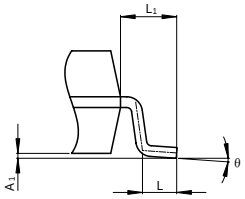
| JEITA Package Code | RENESAS Code | Previous Code | MASS(Typ.) |
|---|---|---|---|
| P-SOP16-5.5x10.06-1.27 | PRSP0016DH-A | FP-16DA | 0.24g |




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.




Terminal cross section




Detail F

| Reference Symbol | Dimension in Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| D | — | 10.06 | 10.5 |
| E | — | 5.5 | — |
| $A_2$ | — | — | — |
| $A_1$ | 0.00 | 0.10 | 0.20 |
| A | — | — | 2.20 |
| $b_p$ | 0.34 | 0.42 | 0.50 |
| $b_1$ | — | 0.40 | — |
| c | 0.17 | 0.22 | 0.27 |
| $c_1$ | — | 0.20 | — |
| θ | 0° | — | 8° |
| $H_E$ | 7.50 | 7.80 | 8.00 |
| e | — | 1.27 | — |
| x | — | — | 0.12 |
| y | — | — | 0.15 |
| Z | — | — | 0.80 |
| L | 0.50 | 0.70 | 0.90 |
| $L_1$ | — | 1.15 | — |

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