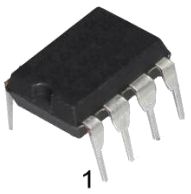
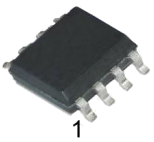
High Performance Current Mode PWM Switch

Features

- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Power-on Soft Start Reducing MOS Stress
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Low V_{DD} startup and operating current
- Frequency jitter to Minimize EMI
- Leading edge blanking on current sense
- Internal Synchronized Slope Compensation
- Low V_{IN}/V_{DD} Startup Current(6.5uA) and Low Operating Current(2.0mA)
- Complete Protection Coverage With Auto Self-Recovery
  - V_{DD} Under Voltage Lockout with Hysteresis (UVLO)
  - Cycle-by-Cycle over current Protection
  - Over load Protection (OLP)
  - Over Temperature Protection (OTP)
  - V_{DD} Over Voltage Protection (OVP)



DIP-8



SOP-8

MSOP-8

Ordering Information

DEVICE	Package Type	MARKING	Packing	Packing Qty
OB2269N	DIP-8	OB2269	TUBE	2000pcs/Box
OB2269M/TR	SOP-8	OB2269	REEL	2500pcs/Reel
OB2269MM/TR	MSOP-8	OB2269	REEL	3000pcs/Reel

Description

OB2269 combines a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective off line flyback converter applications. PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates is extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

V_{DD} low startup current and low operating current contribute to a reliable power on startup and low standby design with OB2269. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery. This greatly helps to reduce the external component count and system cost in application. OB2269 offers complete protection coverage with automatic self recovery feature including Cycle-by-Cycle current limiting(OCP), over load protection(OLP), V_{DD} under voltage lockout

(UVLO), over temperature protection (OTP), and over voltage protection (OVP). The Gate-drive output is clamped at 18V to protect the power MOSFET.

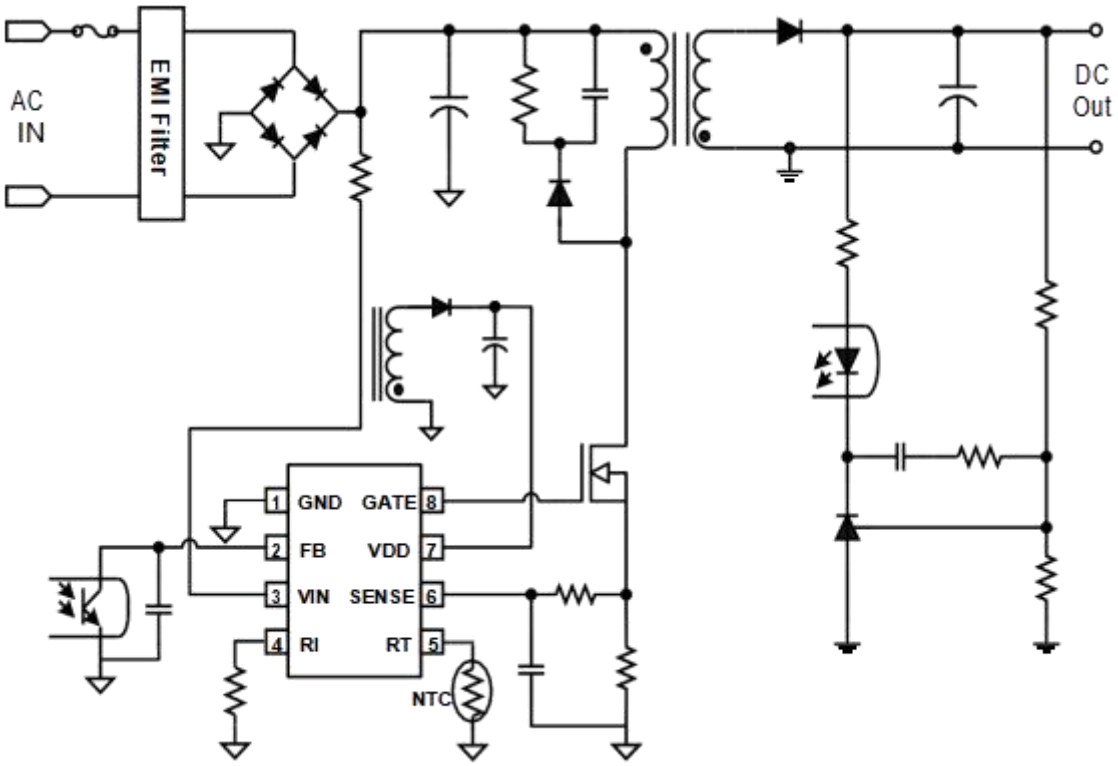
In OB2269, OCP threshold slope is internally optimized to reach constant output power limit over universal AC input range. Excellent EMI performance is achieved with internal frequency jitter technique and soft switching control at the totem pole gate drive output.

The tone energy at below 22KHz is minimized in the design and audio noise is eliminated. OB2269 is offered in both SOP-8 ， MSOP-8 and DIP-8

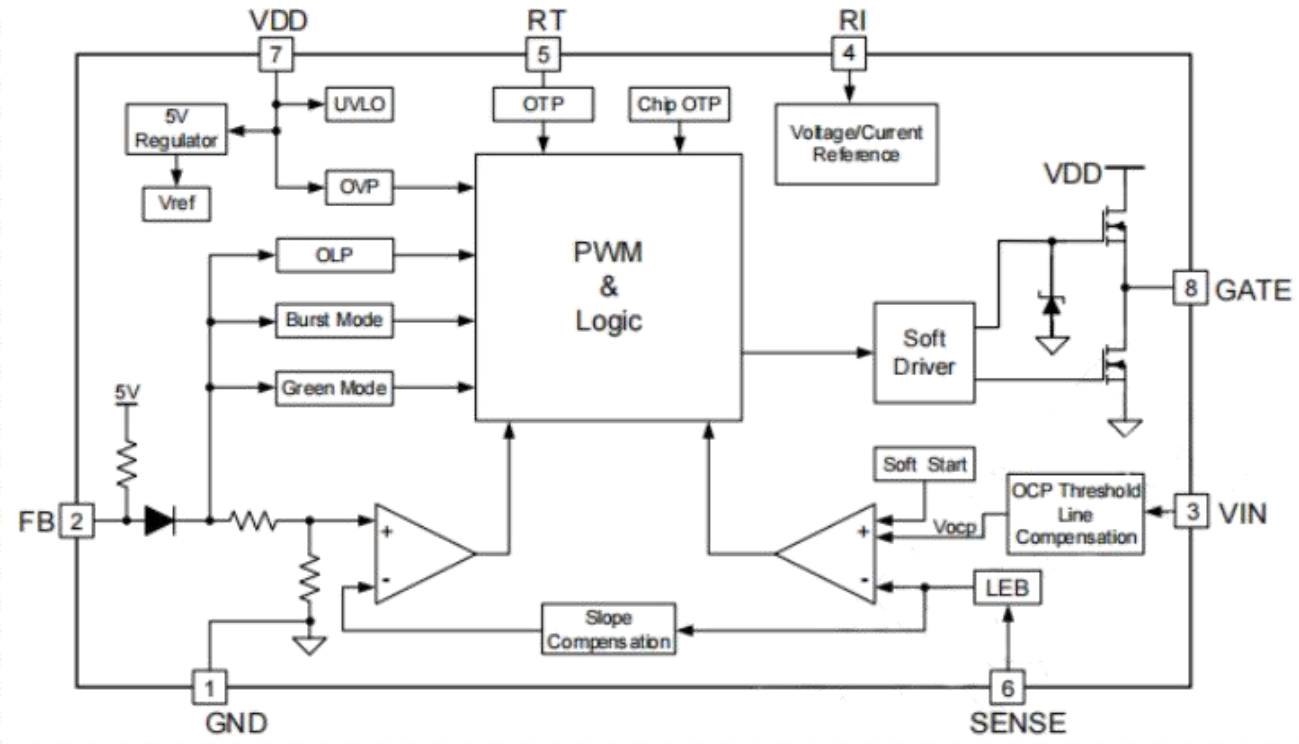
Applications

- Offline AC/DC flyback converter for
- AC/DC Adapter
- Set-Top Box Power Supplies
- Auxiliary Power Supply
- Open-frame SMPS
- Battery Charger

Typical Application

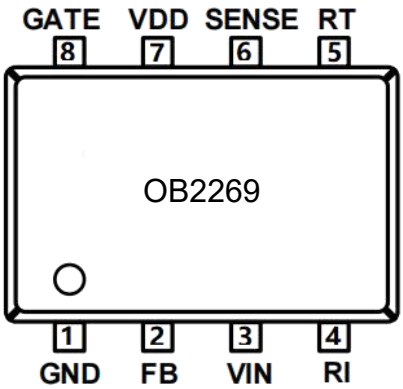


Block Diagram



Pin Configuration

(TOP VIEW)



SOP-8/DIP-8/MSOP-8

Pin Descriptions

Name	Pin	I/O	Description
GND	1	P	Ground
FB	2	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
VIN	3	I	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
RI	4	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
RT	5	I	Temperature sensing input pin. Connected through a NTC resistor to GND.
SENSE	6	I	Current sense input. Connected to MOSFET current sensing resistor node.
VDD	7	P	DC Power Supply pin.
GATE	8	O	Totem-pole gate drive output for power MOSFET.

Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V_{DD}/V_{IN}	DC Supply Voltage		30	V
V_{DD_Clamp}	VDD Clamp Voltage		35	V
I_{DD_Clamp}	VDD Clamp Continuous Current		10	mA
V_{FB}	FB Input Voltage	-0.3V	6.5	V
V_{SENSE}	SENSE Input Voltage	-0.3V	6.5	V
V_{RT}	RT Input Voltage	-0.3V	6.5	V
V_{RI}	RI Input Voltage	-0.3V	6.5	V
R_{JA}	SOP-8 Thermal Resistance (Junction-to-Air)		120	℃/W
T_J	Operating Junction Temperature	-20	125	℃
T_{STG}	Storage Temperature Range	-55	150	℃
T_L	Lead Temperature (Wave Soldering or IR,10Seconds)		245	℃
ESD	Human Body Model,JEDEC:JESD22-A114		2.5	KV
	Machine Model, JEDEC:JESD22- A115		250	V

Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum-rated conditions for extended period may affect device’s reliability

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	DC Supply Voltage	12	23	V
TA	Operating Ambient Temperature	-20	85	℃
RI	RI Resistor Value	24	31	KΩ

Maximum practical continuous power in an open frame design with sufficient drain pattern as a heat sink, at 45℃ ambient.

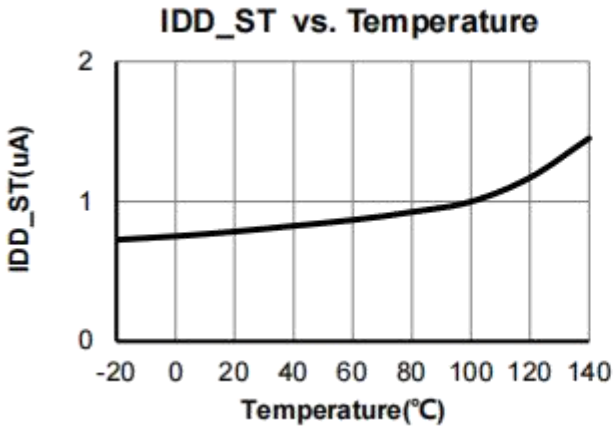
Higher output power is possible with extra added heat sink or air circulation to reduce thermal resistance.

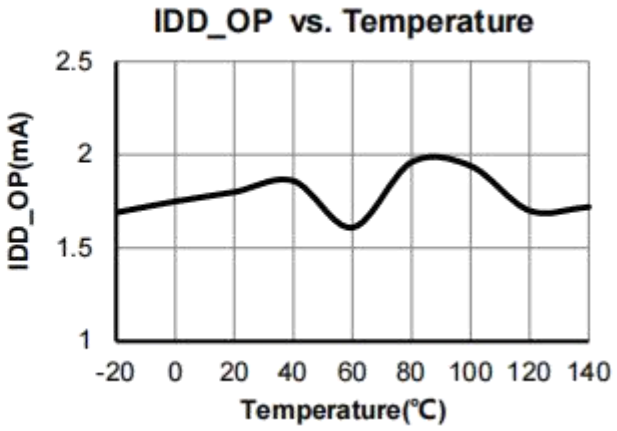
Electrical Characteristics(T_A= 25℃, V_{DD}=16V, RI=24KΩ unless otherwise noted)

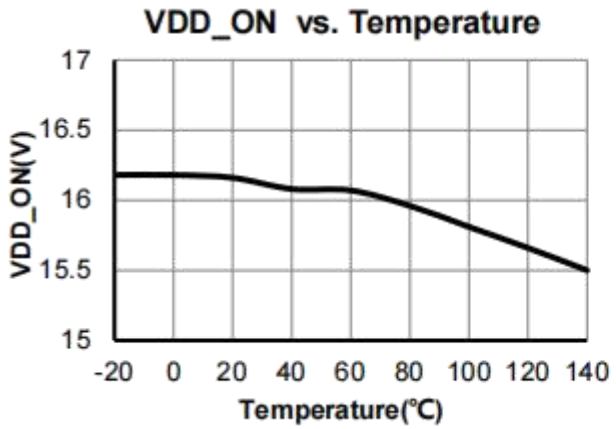
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Supply Voltage (VDD)						
I_{DD_ST}	Startup Current	VDD=15V		6.5	20	uA
I_{DD_OP}	Operation Current	VFB=3V		2.0		mA
V_{DD_ON}	Threshold Voltage to Startup	VDD Rising	14.5	15.5	16.5	V
V_{DD_OFF}	Threshold Voltage to Stop Switching in Normal Mode	VDD Falling	8.5	9.5	10.5	V
$V_{DD\_OVP\_ON}$	VDD Over voltage protection Enter		23.5	25.0	26.5	V
$V_{DD\_OVP\_OFF}$	VDD Over voltage protection Exit (Recovery)		21.5	23.0	24.5	V
$V_{DD\_OVP\_Hys}$	OVP Hysteresis			2.0		V
$T_{D\_VDD\_OVP}$	VDD OVP Debounce time			80		uSec
V_{DD_Clamp}	VDD Zener Clamp voltage	IVDD=5mA		35.0		V
Feedback Input Section(FB Pin)						
V_{FB_Open}	FB Open Loop Voltage			5.1		V
A_V	PWM input gain	$\Delta V_{FB}/\Delta VCS$		2.8		V/V
D_{MAX}	Max duty cycle	VFB=3V,VCS=0.3V	75	80	85	%
V_{Ref_Green}	The threshold enter green mode			2.3		V
$V_{Ref\_Burst\_H}$	The threshold exit Burst mode			1.5		V
$V_{Ref\_Burst\_L}$	The threshold enter Burst mode			1.4		V
I_{FB_Short}	FB pin short circuit current	Short FB pin to GND		0.8		mA
V_{TH_PL}	Power Limiting FB Threshold Voltage			4.4		V
T_{D_PL}	Power limiting Debounce Time			75		mS
Z_{FB_IN}	Input Impedance			6.9		KΩ
Current Sense Input(SENSE Pin)						
T_{SS}	Soft start time			4		ms
T_{LEB}	Leading edge blanking time			250		ns
T_{D_OC}	Over Current Detection and Control Delay			120		ns
$V_{TH\_OC\_0}$	Current Limiting Threshold Voltage at No Compensation	I_{VIN}=0uA	0.85	0.9	0.95	V
$V_{TH\_OC\_1}$	Current Limiting Threshold Voltage at Compensation	I_{VIN}=150uA		0.81		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency	VFB=3V, VCS=0V	60	65	70	KHz
F_{JR}	Frequency jitter range			+/-5		%
F_{Jitter}	jitter frequency			65		Hz
F_{DT}	Frequency Variation vs. Temperature Deviation			5		%
F_{DV}	Frequency Variation vs. V_{DD} Deviation			1		%
RI_range	Operating RI Range		12	24	60	KΩ

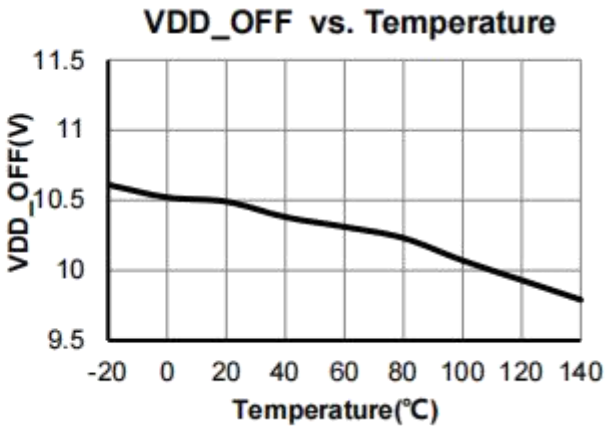
V_{RI_open}	RI open voltage			2.0		V
F_{Burst}	Burst Mode Switch Frequency			22		KHz
Gate Driver Output						
V_{OL}	Output Low Level	IO= -20mA			0.3	V
V_{OH}	Output High Level	IO= +20mA	11			V
V_{GATE_CLAMP}	Output Clamp Voltage Level	VDD=20V		18		V
$T_{\_r}$	Output Rising Time	CL=1nf		120		nSec
$T_{\_f}$	Output Falling Time	CL=1nf		50		nSec
Over Temperature Protection						
I_{RT}	Output Current of RT Pin			70		uA
V_{TH_OTP}	OTP Threshold Voltage		1.00	1.05	1.10	V
$V_{TH\_OTP\_OFF}$	OTP Recovery Threshold Voltage			1.15		V
T_{D_OTP}	OTP Debounce Time			100		uSec
V_{RT_OPEN}	RT Pin Open Voltage			5.5		V

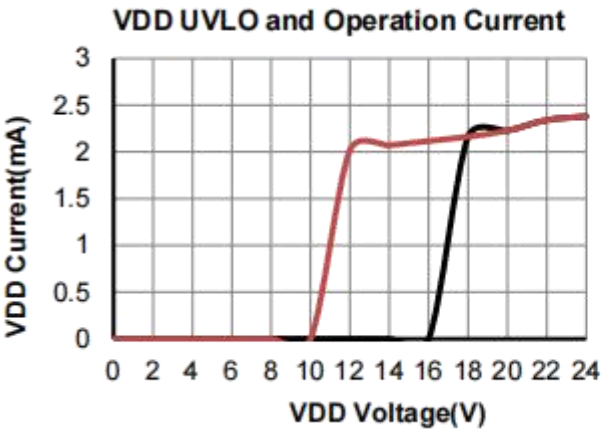
Typical Performance Characteristics (T_A = 25℃, V_{DD}=16V, unless otherwise noted)

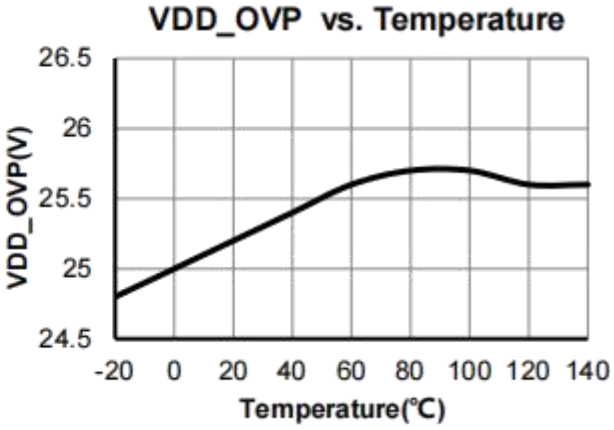


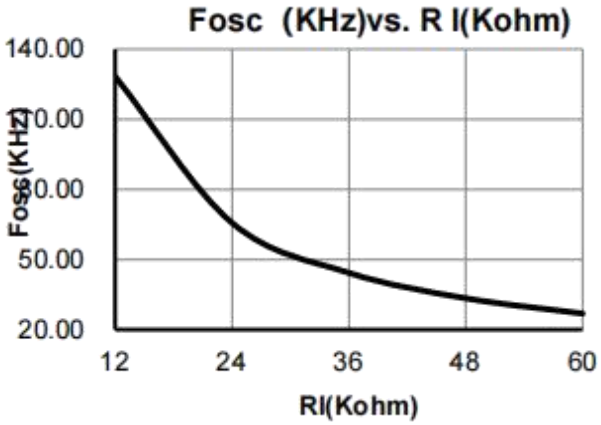


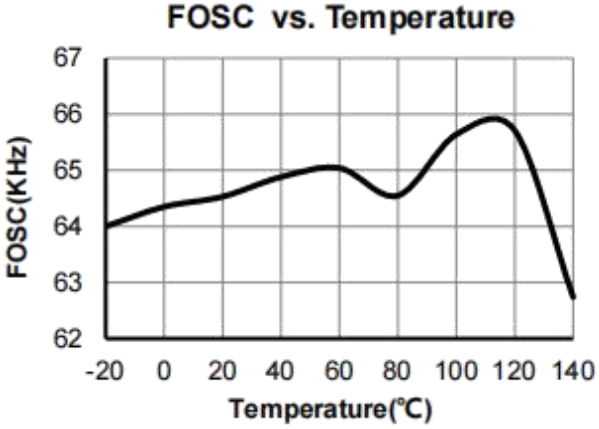


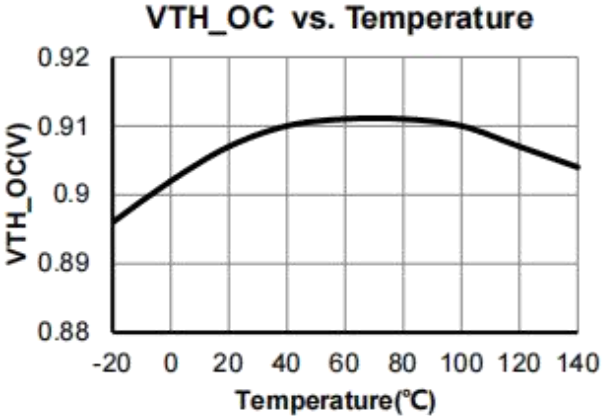


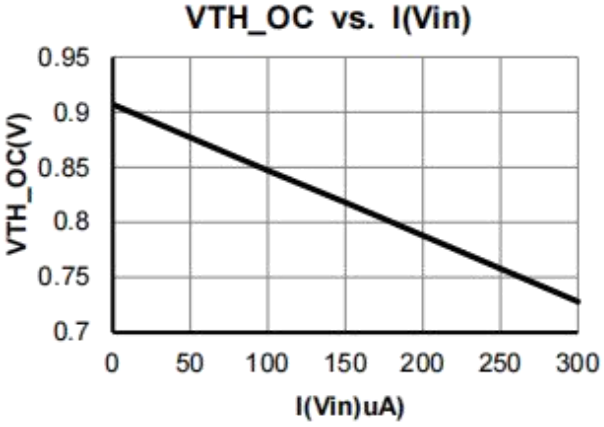

VDD UVLO and Operation Current
VDD Current(mA)
3
2.5
2
1.5
1
0.5
0
0 2 4 6 8 10 12 14 16 18 20 22 24
VDD Voltage(V)

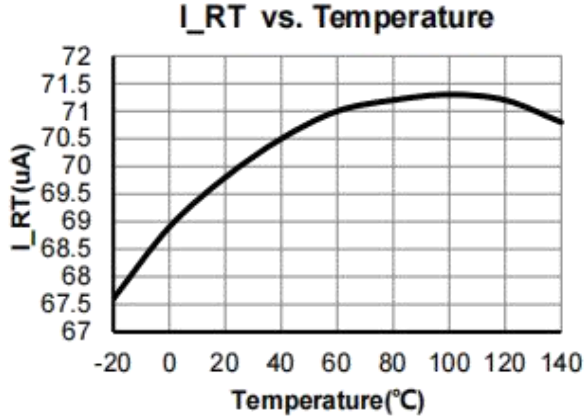

VDD_OVP vs. Temperature
VDD_OVP(V)
26.5
26
25.5
25
24.5
-20 0 20 40 60 80 100 120 140
Temperature(℃)


Fosc (KHz)vs. R I(Kohm)
Fosc(KHz)
140.00
50.00
20.00
12 24 36 48 60
RI(Kohm)


FOSC vs. Temperature
FOSC(KHz)
67
66
65
64
63
62
-20 0 20 40 60 80 100 120 140
Temperature(℃)


VTH_OC vs. Temperature
VTH_OC(V)
0.92
0.91
0.9
0.89
0.88
-20 0 20 40 60 80 100 120 140
Temperature(℃)


VTH_OC vs. I(Vin)
VTH_OC(V)
0.95
0.9
0.85
0.8
0.75
0.7
0 50 100 150 200 250 300
I(Vin)uA)


I_RT vs. Temperature
I_RT(uA)
72
71.5
71
70.5
70
69.5
69
68.5
68
67.5
67
-20 0 20 40 60 80 100 120 140
Temperature(℃)

Functional Description

The OB2269 is a highly integrated PWM controller IC optimized for off-line flyback converter applications. The extended Burst Mode control greatly reduces the standby power consumption and helps the design easily to meet the international power conservation requirements.

Startup Current and Start up Control

Startup current of OB2269 is designed to be very low so that V_{DD} could be charged up above V_{DD_ON} and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet achieve a reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2MΩ, 1/8W startup resistor could be used together with a V_{DD} capacitor to provide a fast startup and yet low power dissipation design solution.

Operating Current

The Operating current of OB2269 is low at 2.0mA (typical). Good efficiency is achieved with OB2269 low operation current together with the extended Burst Mode control features.

Soft Start

OB2269 features an internal 4ms (typical) soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as V_{DD} reaches V_{DD_ON}, the SENSE peak voltage is gradually increased from 0.1V to the maximum level. Every restart up is followed by a soft start.

Frequency jitter for EMI improvement

The frequency jitter is implemented in OB2269. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Oscillator Operation

The switching frequency of OB2269 is externally programmable. A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in KΩ range at nominal loading operational condition.

$$F_{OSC}= \frac{1560}{RI(K\Omega)} \ (Khz)$$

Multi-mode Operation for High Efficiency

OB2269 is a multi-mode controller. The controller changes the mode of operation according to the FB pin voltage. At the normal operating condition, the IC operates in （65KHz, if RI=24KΩ）PWM mode. As the output load current is decreased, the IC enter into green mode smoothly from the PWM mode. In this mode, the switching frequency will start to linearly decrease from 65KHz to 22KHz. So the switching loss is minimized and the high conversion efficiency can be achieved. At light load or no load condition, most of the power dissipation in a switching mode power supply is from switching loss of the MOSFET, the core loss of the transformer and the loss of the snubber circuit. The magnitude of power loss is in proportion to the switching frequency. Lower switching frequency leads to the reduction on the power loss and thus conserves the energy. The switching frequency is internally adjusted at no load or light load condition. The switch frequency reduces at light/no load condition to improve the conversion efficiency.

At light load or no load condition, the FB input drops below $V_{Ref\_Burst\_L}$ and device enters Burst Mode control. The Gate drive output switches when FB input rises back to $V_{Ref\_Burst\_H.}$ Otherwise the gate drive remains at off state to minimize the switching loss and reduces the standby power consumption to the greatest extend.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in OB2269 current mode PWM control. The switch current is detected by a sense resistor into the SENSE pin. An internal leading edge blanking circuit chops off the sensed voltage spike at initial internal power MOSFET on state due to snubber diode reverse recovery and surge gate current of power MOSFET. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

Over Temperature Protection

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperatures rise. With the fixed internal current IRT flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than V_{TH_OTP}.

Gate Drive

OB2269 GATE is connected to the gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.

A good trade-off is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected V_{DD} input.

Protection Controls

Good power supply system reliability is achieved with auto-recovery protection features including Cycle-by-Cycle current limiting (OCP), Under Voltage Lockout on V_{DD} (UVLO), Over Temperature Protection (OTP), V_{DD} Over Voltage Protection (OVP).

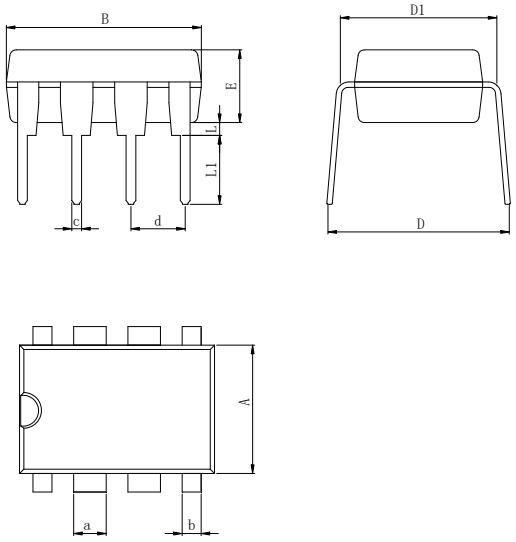
The OCP threshold value is self adjusted lower at higher current into V_{IN} pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on OB2269.

At output overload condition when FB input voltage exceeds power limit threshold value for more than TD_PL, control circuit reacts to shut down the power MOSFET. It restarts when V_{DD} voltage drops below UVLO limit.

Similarly, when an Over Temperature condition is detected, control circuit shutdowns the power MOSFET. OB2269 resumes the operation when temperature drops below the hysteresis value. V_{DD} is supplied with transformer auxiliary winding output. It is clamped when V_{DD} is higher than 35V. MOSFET is shut down when V_{DD} drops below V_{DD_ON} limit and device enters power on startup sequence thereafter.

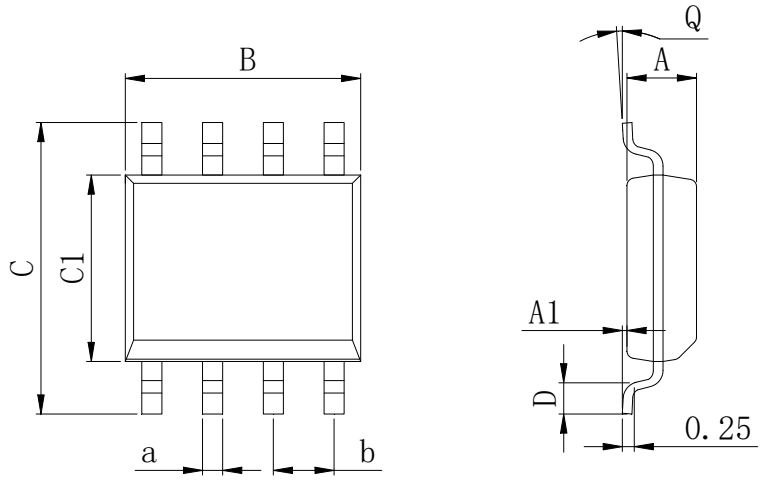
Physical Dimensions

DIP-8



Dimensions In Millimeters(DIP-8)											
Symbol:	A	B	D	D1	E	L	L1	a	b	c	d
Min:	6.10	9.00	8.10	7.42	3.10	0.50	3.00	1.50	0.85	0.40	2.54 BSC
Max:	6.68	9.50	10.9	7.82	3.55	0.70	3.60	1.55	0.90	0.50	

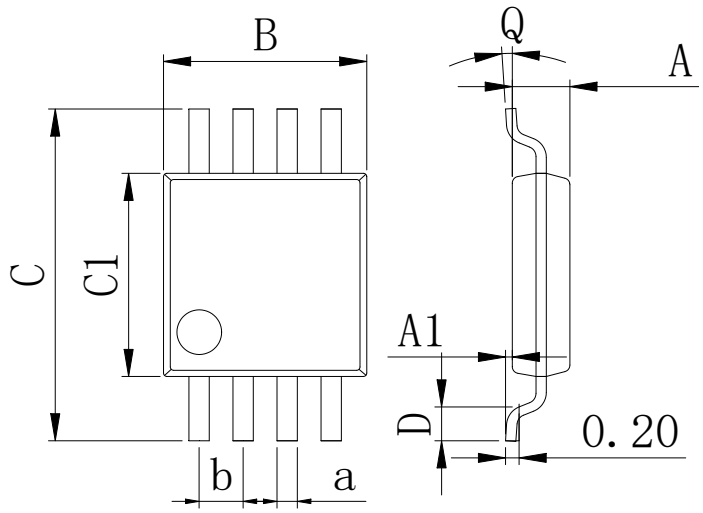
SOP-8 (150mil)



Dimensions In Millimeters(SOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	1.35	0.05	4.90	5.80	3.80	0.40	0°	0.35	1.27 BSC
Max:	1.55	0.20	5.10	6.20	4.00	0.80	8°	0.45	

Physical Dimensions

MSOP-8



Dimensions In Millimeters(MSOP-8)									
Symbol:	A	A1	B	C	C1	D	Q	a	b
Min:	0.80	0.05	2.90	4.75	2.90	0.35	0°	0.25	0.65 BSC
Max:	0.90	0.20	3.10	5.05	3.10	0.75	8°	0.35	

Revision History

DATE	REVISION	PAGE
2012-10-15	New	1-14
2023-8-30	Update encapsulation type、Update Lead Temperature、Updated DIP-8 Physical dimension	1、5、11

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