

To our customers,

---

## Old Company Name in Catalogs and Other Documents

---

On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

Send any inquiries to <http://www.renesas.com/inquiry>.

## Notice

1. All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
2. Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
3. You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
4. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
5. When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
6. Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
7. Renesas Electronics products are classified according to the following three quality grades: “Standard”, “High Quality”, and “Specific”. The recommended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as “Specific” without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as “Specific” or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is “Standard” unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.
  - “Standard”: Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.
  - “High Quality”: Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.
  - “Specific”: Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
8. You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

**μPD44647094A-A, 44647184A-A, 44647364A-A, 44647096A-A, 44647186A-A, 44647366A-A**

## 72M-BIT QDR™ II+ SRAM 2.0 & 2.5 CLOCK CYCLES READ LATENCY 4-WORD BURST OPERATION

### Description

The μPD44647094A-A and μPD44647096A-A are 8,388,608-word by 9-bit, the μPD44647184A-A and μPD44647186A-A are 4,194,304-word by 18-bit and the μPD44647364A-A and μPD44647366A-A are 2,097,152-word by 36-bit synchronous quad data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μPD44647xx4A-A is for 2.0 clock cycles and the μPD44647xx6A-A is for 2.5 clock cycles read latency. The μPD44647094A-A, μPD44647096A-A, μPD44647184A-A, μPD44647186A-A, μPD44647364A-A and μPD44647366A-A integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and K#) are latched on the positive edge of K and K#.

These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

These products are packaged in 165-pin PLASTIC BGA.

### Features

- 1.8 ± 0.1 V power supply
- 165-pin PLASTIC BGA (15 x 17)
- HSTL interface
- DLL/PLL circuitry for wide output data valid window and future frequency scaling
- Separate independent read and write data ports with concurrent transactions
- 100% bus utilization DDR READ and WRITE operation
- Four-tick burst for reduced address frequency
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two Echo clocks (CQ and CQ#)
- Data Valid pin (QVLD) supported
- Read latency : 2.0 & 2.5 clock cycles (Not selectable by user)
- Internally self-timed write control
- Clock-stop capability. Normal operation is restored in 20 μs after clock is resumed.
- User programmable impedance output (35 to 70 Ω)
- Fast clock cycle time : 2.5 ns (400 MHz) for 2.0 clock cycles read latency,  
2.0 ns (500 MHz) for 2.5 clock cycles read latency
- Simple control logic for easy depth expansion
- JTAG 1149.1 compatible test access port
- On-Die Termination (ODT) for better signal quality (Selectable ON/OFF by user)

**The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**

Ordering Information

2.0 Clock Cycles Read Latency

Part number	Cycle Time ns	Clock Frequency MHz	Organization (word x bit)	Core Supply Voltage V	I/O Interface	Package
μPD44647094AF5-E25-FQ1-A <sup>Note</sup>	2.5	400	8M x 9	1.8 ± 0.1	HSTL	165-pin PLASTIC BGA (15 x 17) Lead-free
μPD44647094AF5-E30-FQ1-A	3.0	333				
μPD44647094AF5-E33-FQ1-A	3.3	300				
μPD44647184AF5-E25-FQ1-A <sup>Note</sup>	2.5	400	4M x 18			
μPD44647184AF5-E30-FQ1-A	3.0	333				
μPD44647184AF5-E33-FQ1-A	3.3	300				
μPD44647364AF5-E25-FQ1-A <sup>Note</sup>	2.5	400	2M x 36			
μPD44647364AF5-E30-FQ1-A	3.0	333				
μPD44647364AF5-E33-FQ1-A	3.3	300				

Note Please contact our sales.

2.5 Clock Cycles Read Latency

Part number	Cycle Time ns	Clock Frequency MHz	Organization (word x bit)	Core Supply Voltage V	I/O Interface	Package
μPD44647096AF5-E20-FQ1-A <sup>Note</sup>	2.0	500	8M x 9	1.8 ± 0.1	HSTL	165-pin PLASTIC BGA (15 x 17) Lead-free
μPD44647096AF5-E22-FQ1-A	2.2	450				
μPD44647096AF5-E25-FQ1-A	2.5	400				
μPD44647096AF5-E30-FQ1-A	3.0	333				
μPD44647186AF5-E20-FQ1-A <sup>Note</sup>	2.0	500	4M x 18			
μPD44647186AF5-E22-FQ1-A	2.2	450				
μPD44647186AF5-E25-FQ1-A	2.5	400				
μPD44647186AF5-E30-FQ1-A	3.0	333				
μPD44647366AF5-E20-FQ1-A <sup>Note</sup>	2.0	500	2M x 36			
μPD44647366AF5-E22-FQ1-A	2.2	450				
μPD44647366AF5-E25-FQ1-A	2.5	400				
μPD44647366AF5-E30-FQ1-A	3.0	333				

Note Please contact our sales.

**Feature Differences between QDR II and QDR II+**

Features	QDR II	QDR II+	Note
Frequency (DLL/PLL ON)	200 MHz to 333 MHz	300 MHz to 500 MHz	
Organization	x9 / x18 / x36	x9 / x18 / x36	
V <sub>DD</sub>	1.8 ± 0.1 V	1.8 ± 0.1 V	
V <sub>DDQ</sub>	1.8 ± 0.1 V or 1.5 ± 0.1 V	1.8 ± 0.1 V or 1.5 ± 0.1 V	
Read Latency	1.5 clock cycles	2.0 & 2.5 clock cycles	1
Write Latency	1.0 clock cycle	1.0 clock cycle	2
Input Clocks (K, K#)	Single Ended (K, K#)	Single Ended (K, K#)	
Output Clocks (C, C#)	Yes	No	
Echo Clock Number (CQ, CQ#)	1 Pair	1 Pair	3
Package	165-pin PLASTIC BGA (15 x 17)	165-pin PLASTIC BGA (15 x 17)	
Individual Byte Write (BWx#)	Yes	Yes	
QVLD	No	Yes	4
ODT	No	Yes	5

- Notes**
1. QDR II+ read latency is not user selectable. Offered as two different devices. 2.5 clock cycle is consortium standard, and 2.0 clock cycle is vendor option.
  2. QDR II+ write latency is 1.0 clock cycle regardless of read latency.
  3. Echo Clocks are single-ended outputs.
  4. Edge aligned with Echo Clocks
  5. ODT ON/OFF is user selectable.

Pin Configurations

165-pin PLASTIC BGA (15 x 17)

(Top View)

[μPD44647094A-A], [μPD44647096A-A]

8M x 9

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	A	A	W#	NC	K#	NC/144M	R#	A	A	CQ
B	NC	NC	NC	A	NC/288M	K	BW0#	A	NC	NC	Q4
C	NC	NC	NC	V <sub>SS</sub>	A	NC	A	V <sub>SS</sub>	NC	NC	D4
D	NC	D5	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	NC
E	NC	NC	Q5	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D3	Q3
F	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
G	NC	D6	Q6	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
H	DLL#	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q2	D2
K	NC	NC	NC	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	NC
L	NC	Q7	D7	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q1
M	NC	NC	NC	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D1
N	NC	D8	NC	V <sub>SS</sub>	A	A	A	V <sub>SS</sub>	NC	NC	NC
P	NC	NC	Q8	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

- |          |                             |                  |                              |
|----------|-----------------------------|------------------|------------------------------|
| A        | : Address inputs            | TMS              | : IEEE 1149.1 Test input     |
| D0 to D8 | : Data inputs               | TDI              | : IEEE 1149.1 Test input     |
| Q0 to Q8 | : Data outputs              | TCK              | : IEEE 1149.1 Clock input    |
| R#       | : Read input                | TDO              | : IEEE 1149.1 Test output    |
| W#       | : Write input               | V <sub>REF</sub> | : HSTL input reference input |
| BW0#     | : Byte Write data select    | V <sub>DD</sub>  | : Power Supply               |
| K, K#    | : Input clock               | V <sub>DDQ</sub> | : Power Supply               |
| CQ, CQ#  | : Echo clock                | V <sub>SS</sub>  | : Ground                     |
| ZQ       | : Output impedance matching | NC               | : No connection              |
| DLL#     | : DLL/PLL disable           | NC/xxM           | : Expansion address for xxMb |
| QVLD     | : Q Valid output            |                  |                              |
| ODT      | : ODT Control Input         |                  |                              |

- Remarks**
1. xxx# indicates active LOW signal.
  2. Refer to **Package Drawing** for the index mark.
  3. 7A and 5B are expansion addresses: 7A for 144Mb  
: 7A and 5B for 288Mb

165-pin PLASTIC BGA (15 x 17)

(Top View)

[μPD44647184A-A], [μPD44647186A-A]

4M x 18

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/144M	A	W#	BW1#	K#	NC/288M	R#	A	A	CQ
B	NC	Q9	D9	A	NC	K	BW0#	A	NC	NC	Q8
C	NC	NC	D10	V <sub>SS</sub>	A	NC	A	V <sub>SS</sub>	NC	Q7	D8
D	NC	D11	Q10	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	NC	D7
E	NC	NC	Q11	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	D6	Q6
F	NC	Q12	D12	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	Q5
G	NC	D13	Q13	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	NC	D5
H	DLL#	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	NC	NC	D14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	Q4	D4
K	NC	NC	Q14	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	NC	D3	Q3
L	NC	Q15	D15	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	NC	NC	Q2
M	NC	NC	D16	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	NC	Q1	D2
N	NC	D17	Q16	V <sub>SS</sub>	A	A	A	V <sub>SS</sub>	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

- A : Address inputs
- D0 to D17 : Data inputs
- Q0 to Q17 : Data outputs
- R# : Read input
- W# : Write input
- BW0#, BW1# : Byte Write data select
- K, K# : Input clock
- CQ, CQ# : Echo clock
- ZQ : Output impedance matching
- DLL# : DLL/PLL disable
- QVLD : Q Valid output
- ODT : ODT Control Input
- TMS : IEEE 1149.1 Test input
- TDI : IEEE 1149.1 Test input
- TCK : IEEE 1149.1 Clock input
- TDO : IEEE 1149.1 Test output
- V<sub>REF</sub> : HSTL input reference input
- V<sub>DD</sub> : Power Supply
- V<sub>DDQ</sub> : Power Supply
- V<sub>SS</sub> : Ground
- NC : No connection
- NC/xxM : Expansion address for xxMb

- Remarks**
1. xxx# indicates active LOW signal.
  2. Refer to **Package Drawing** for the index mark.
  3. 2A and 7A are expansion addresses: 2A for 144Mb  
 : 2A and 7A for 288Mb

165-pin PLASTIC BGA (15 x 17)

(Top View)

[μPD44647364A-A], [μPD44647366A-A]

2M x 36

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	NC/288M	A	W#	BW2#	K#	BW1#	R#	A	NC/144M	CQ
B	Q27	Q18	D18	A	BW3#	K	BW0#	A	D17	Q17	Q8
C	D27	Q28	D19	V <sub>SS</sub>	A	NC	A	V <sub>SS</sub>	D16	Q7	D8
D	D28	D20	Q19	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	Q16	D15	D7
E	Q29	D29	Q20	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	Q15	D6	Q6
F	Q30	Q21	D21	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	D14	Q14	Q5
G	D30	D22	Q22	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	Q13	D13	D5
H	DLL#	V <sub>REF</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	V <sub>DDQ</sub>	V <sub>REF</sub>	ZQ
J	D31	Q31	D23	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	D12	Q4	D4
K	Q32	D32	Q23	V <sub>DDQ</sub>	V <sub>DD</sub>	V <sub>SS</sub>	V <sub>DD</sub>	V <sub>DDQ</sub>	Q12	D3	Q3
L	Q33	Q24	D24	V <sub>DDQ</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>DDQ</sub>	D11	Q11	Q2
M	D33	Q34	D25	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	V <sub>SS</sub>	D10	Q1	D2
N	D34	D26	Q25	V <sub>SS</sub>	A	A	A	V <sub>SS</sub>	Q10	D9	D1
P	Q35	D35	Q26	A	A	QVLD	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	ODT	A	A	A	TMS	TDI

- |              |                             |                  |                              |
|--------------|-----------------------------|------------------|------------------------------|
| A            | : Address inputs            | TMS              | : IEEE 1149.1 Test input     |
| D0 to D35    | : Data inputs               | TDI              | : IEEE 1149.1 Test input     |
| Q0 to Q35    | : Data outputs              | TCK              | : IEEE 1149.1 Clock input    |
| R#           | : Read input                | TDO              | : IEEE 1149.1 Test output    |
| W#           | : Write input               | V <sub>REF</sub> | : HSTL input reference input |
| BW0# to BW3# | : Byte Write data select    | V <sub>DD</sub>  | : Power Supply               |
| K, K#        | : Input clock               | V <sub>DDQ</sub> | : Power Supply               |
| CQ, CQ#      | : Echo clock                | V <sub>SS</sub>  | : Ground                     |
| ZQ           | : Output impedance matching | NC               | : No connection              |
| DLL#         | : DLL/PLL disable           | NC/xxM           | : Expansion address for xxMb |
| QVLD         | : Q Valid output            |                  |                              |
| ODT          | : ODT Control Input         |                  |                              |

**Remarks** 1. xxx# indicates active LOW signal.

2. Refer to **Package Drawing** for the index mark.

3. 2A and 10A are expansion addresses: 10A for 144Mb

10A and 2A for 288Mb

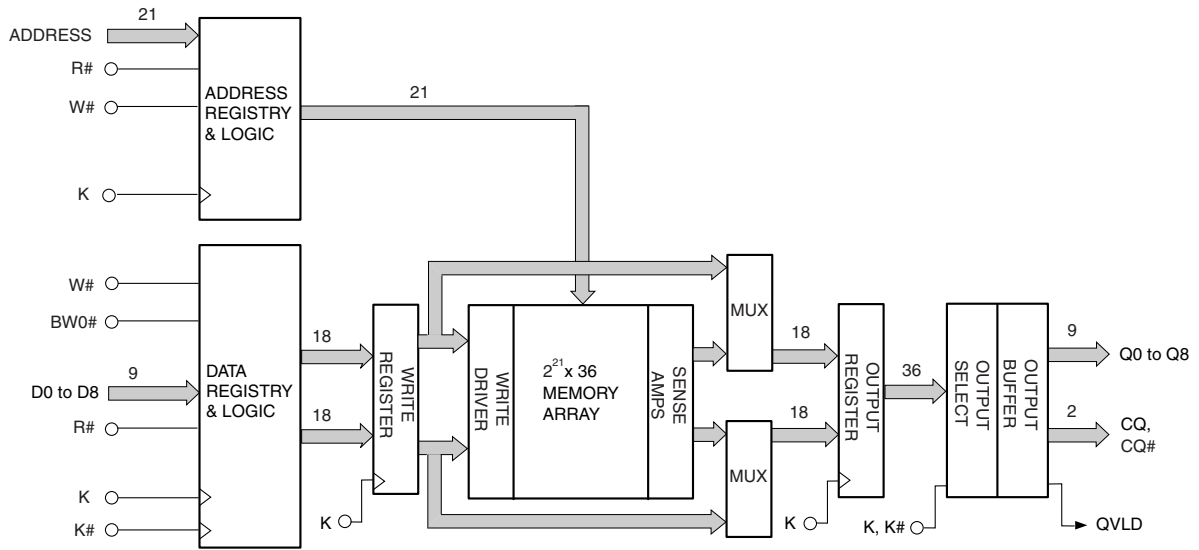


Pin Identification

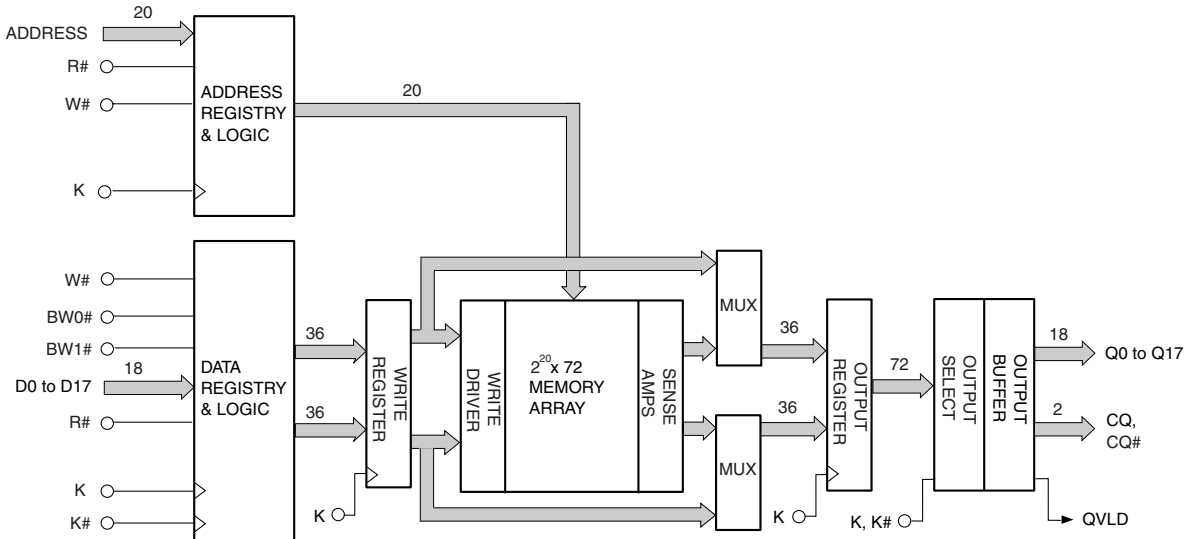
Symbol	Type	Description
A	Input	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst of four words (two clock periods of bus activity). These inputs are ignored when device is deselected, i.e., NOP (R# = W# = HIGH).
D0 to Dxx	Input	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See <b>Pin Configurations</b> for ball site location of individual signals. x9 device uses D0 to D8. x18 device uses D0 to D17. x36 device uses D0 to D35.
Q0 to Qxx	Output	Synchronous Data Outputs: Output data is synchronized to the respective K and K# rising edges. Data is output in synchronization with K and K#, depending on the R# command. See <b>Pin Configurations</b> for ball site location of individual signals. x9 device uses Q0 to Q8. x18 device uses Q0 to Q17. x36 device uses Q0 to Q35.
R#	Input	Synchronous Read: When LOW this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K. If a READ command (R# = LOW) is input, an input of R# on the subsequent rising edge of K is ignored.
W#	Input	Synchronous Write: When LOW this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K. If a WRITE command (W# = LOW) is input, an input of W# on the subsequent rising edge of K is ignored.
BWx#	Input	Synchronous Byte Writes: When LOW these inputs cause their respective byte to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and K# for each of the two rising edges comprising the WRITE cycle. See <b>Pin Configurations</b> for signal to data relationships. x9 device uses BW0#. x18 device uses BW0#, BW1#. x36 device uses BW0# to BW3#. See <b>Byte Write Operation</b> for relation between BWx# and Dxx.
K, K#	Input	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
CQ, CQ#	Output	Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tristates. If K and K# are stopped, CQ and CQ# will also stop.
ZQ	Input	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. Q, CQ, CQ# and QVLD output impedance are set to $0.2 \times RQ$ , where RQ is a resistor from this bump to ground. The output impedance can be minimized by directly connect ZQ to $V_{DDQ}$ . This pin cannot be connected directly to GND or left unconnected. The output impedance is adjusted every 20 μs upon power-up to account for drifts in supply voltage and temperature. After replacement for a resistor, the new output impedance is reset by implementing power-on sequence.
DLL#	Input	DLL/PLL Disable: When DLL# is LOW, the operation can be performed at a clock frequency slower than TKHKH (MAX.) without the DLL/PLL circuit being used. The AC/DC characteristics cannot be guaranteed. For normal operation, DLL# must be HIGH and it can be connected to $V_{DDQ}$ through a 10 kΩ or less resistor.
QVLD	Output	Q valid Output: The Q Valid indicates valid output data. QVLD is edge aligned with CQ and CQ#.
ODT	Input	ODT Control Input: When the ODT control pin is HIGH, the ODT function is turned on at Dxx and BWx# pins. The ODT resistors are set to $0.6 \times RQ$ , where RQ is a resistor from ZQ pin bump to ground. When the ODT Control pin is LOW or No Connect, the ODT function is turned off. The ODT ON/OFF is set at power-on sequence. The ODT can not change the state after power-on. To enable ODT function, ODT pin must be HIGH and it can be connected to $V_{DDQ}$ through a 10 kΩ or less resistor.
TMS TDI	Input	IEEE 1149.1 Test Inputs: 1.8 V I/O level. These balls may be left Not Connected if the JTAG function is not used in the circuit.
TCK	Input	IEEE 1149.1 Clock Input: 1.8 V I/O level. This pin must be tied to $V_{SS}$ if the JTAG function is not used in the circuit.
TDO	Output	IEEE 1149.1 Test Output: 1.8 V I/O level. When providing any external voltage to TDO signal, it is recommended to pull up to $V_{DD}$ .
VREF	–	HSTL Input Reference Voltage: Nominally $V_{DDQ}/2$ . Provides a reference voltage for the input buffers.
VDD	Supply	Power Supply: 1.8 V nominal. See <b>Recommended DC Operating Conditions</b> and <b>DC Characteristics</b> for range.
VDDQ	Supply	Power Supply: Isolated Output Buffer Supply. Nominally 1.5 V. 1.8 V is also permissible. See <b>Recommended DC Operating Conditions</b> and <b>DC Characteristics</b> for range.
VSS	Supply	Power Supply: Ground
NC	–	No Connect: These signals are not connected internally.

Block Diagram

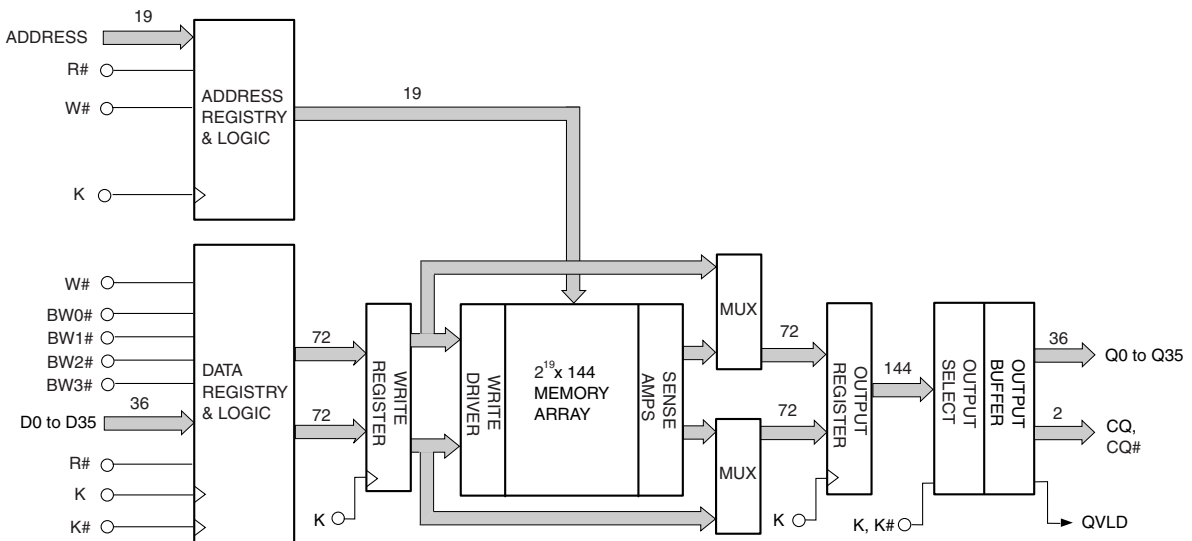
[μPD44647094A-A], [μPD44647096A-A]



[μPD44647184A-A], [μPD44647186A-A]



[μPD44647364A-A], [μPD44647366A-A]



**Power-On Sequence in QDR II+ SRAM**

QDR II+ SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations. The following timing charts show the recommended power-on sequence.

The following power-up supply voltage application is recommended:  $V_{SS}$ ,  $V_{DD}$ ,  $V_{DDQ}$ ,  $V_{REF}$ , then  $V_{IN}$ .  $V_{DD}$  and  $V_{DDQ}$  can be applied simultaneously, as long as  $V_{DDQ}$  does not exceed  $V_{DD}$  by more than 0.5 V during power-up. The following power-down supply voltage removal sequence is recommended:  $V_{IN}$ ,  $V_{REF}$ ,  $V_{DDQ}$ ,  $V_{DD}$ ,  $V_{SS}$ .  $V_{DD}$  and  $V_{DDQ}$  can be removed simultaneously, as long as  $V_{DDQ}$  does not exceed  $V_{DD}$  by more than 0.5 V during power-down.

**Power-On Sequence**

- Apply power and tie DLL# to HIGH.
- Apply  $V_{DD}$  before  $V_{DDQ}$ .
- Apply  $V_{DDQ}$  before  $V_{REF}$  or at the same time as  $V_{REF}$ .
- Select ODT ON/OFF.
- Provide stable clock for more than 20  $\mu s$  to lock the DLL/PLL.

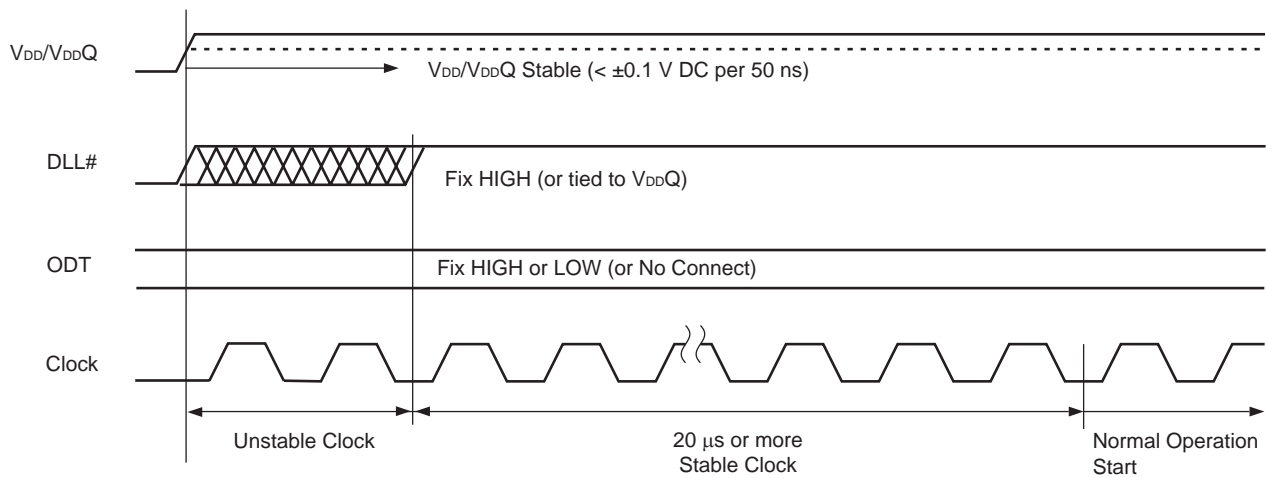
**DLL/PLL Constraints**

The DLL/PLL uses K clock as its synchronizing input and the input should have low phase jitter which is specified as TKC var. The DLL/PLL can cover 190 MHz as the lowest frequency. If the input clock is unstable and the DLL/PLL is enabled, then the DLL/PLL may lock onto an undesired clock frequency.

**ODT initialization**

The ODT ON/OFF is set at power-on sequence. When the ODT Control pin is HIGH before applying stable clock, the ODT function is turn on. When the ODT Control pin is LOW or No Connect, the ODT function is off. The ODT can not change the state after power-on.

**Power-On Waveforms**



**On-Die Termination (ODT)**

On-Die Termination (ODT) is enabled by setting ODT control pin to HIGH at power-on sequence. The ODT resistors ( $R_{TT}$ ) are set to  $0.6 \times R_Q$ , where  $R_Q$  is a resistor from ZQ pin bump to ground. With ODT on, all the Ds and BW#s are terminated to  $V_{DDQ}$  and  $V_{SS}$  with a resistance  $R_{TT} \times 2$ . The command, address, and clock signals are not terminated. Figure below shows the equivalent circuit of a Dxx and BWx# receiver with ODT. ODT at the Ds and BW#s are always on.

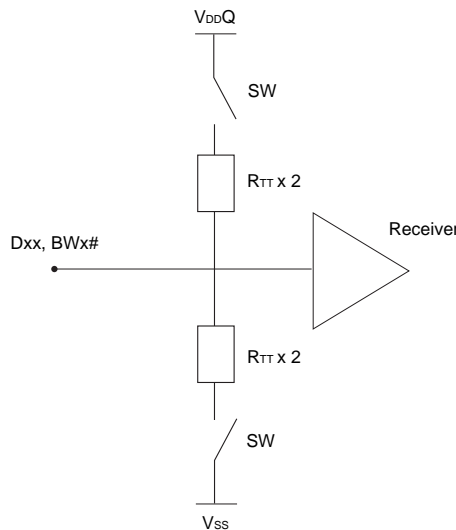
When the ODT control pin is LOW or No Connect at power-on sequence, the ODT function is always off.  
 When the ODT be changed the state after power-on, the AC/DC characteristics cannot be guaranteed.

**On-Die Termination DC Parameters**

Description	Symbol	MIN.	TYP.	MAX.	Units
On-Die termination	$R_{TT}$	105	150	210	$\Omega$
External matching resistor	$R_Q$	175	250	350	$\Omega$

**Remark** The allowable range of  $R_Q$  to guarantee impedance matching a tolerance of  $\pm 20\%$  is between  $175\ \Omega$  and  $350\ \Omega$ .

**On-Die Termination-Equivalent Circuit**



QDR Consortium specification for ODT is defined when 6R is HIGH and vendor specification when 6R is LOW or Floating. NEC specification is "Disabled" with 6R LOW or Floating as follows.

**ODT-option clarification**

6R input	ODT function		Termination value	
	Consortium specification	NEC specification	Consortium specification	NEC specification
HIGH	Active	Active	$R_{TT} = 0.6 \times R_Q$	$R_{TT} = 0.6 \times R_Q$
LOW	Vendor specification	Disabled	Vendor specification	–
Floating	Vendor specification	Disabled	Vendor specification	–

**Note** In case of nominal value ( $R_Q = 250\ \Omega$ ),  $R_{TT} = 150\ \Omega$ .

Truth Table

2.0 Clock Cycles Read Latency

[μPD44647094A-A], [μPD44647184A-A], [μPD44647364A-A]

Operation	CLK	R#	W#	D or Q				
WRITE cycle Load address, input write data on two consecutive K and K# rising edge	L → H	H	L	Data in				
				Input data	D <sub>A</sub> (A+0)	D <sub>A</sub> (A+1)	D <sub>A</sub> (A+2)	D <sub>A</sub> (A+3)
				Input clock	K(t+1) ↑	K#(t+1) ↑	K(t+2) ↑	K#(t+2) ↑
READ cycle Load address, read data on two consecutive K and K# rising edge	L → H	L	X	Data out				
				Output data	Q <sub>A</sub> (A+0)	Q <sub>A</sub> (A+1)	Q <sub>A</sub> (A+2)	Q <sub>A</sub> (A+3)
				Output clock	K(t+2) ↑	K#(t+2) ↑	K(t+3) ↑	K#(t+3) ↑
NOP (No operation)	L → H	H	H	D = X, Q = High-Z				
Clock stop	Stopped	X	X	Previous state				

2.5 Clock Cycles Read Latency

[μPD44647096A-A], [μPD44647186A-A], [μPD44647366A-A]

Operation	CLK	R#	W#	D or Q				
WRITE cycle Load address, input write data on two consecutive K and K# rising edge	L → H	H	L	Data in				
				Input data	D <sub>A</sub> (A+0)	D <sub>A</sub> (A+1)	D <sub>A</sub> (A+2)	D <sub>A</sub> (A+3)
				Input clock	K(t+1) ↑	K#(t+1) ↑	K(t+2) ↑	K#(t+2) ↑
READ cycle Load address, read data on two consecutive K and K# rising edge	L → H	L	X	Data out				
				Output data	Q <sub>A</sub> (A+0)	Q <sub>A</sub> (A+1)	Q <sub>A</sub> (A+2)	Q <sub>A</sub> (A+3)
				Output clock	K#(t+2) ↑	K(t+3) ↑	K#(t+3) ↑	K(t+4) ↑
NOP (No operation)	L → H	H	H	D = X, Q = High-Z				
Clock stop	Stopped	X	X	Previous state				

**Remarks** Remarks listed below are for both products with 2.0 and 2.5 Clock Cycles Read Latency.

1. H : HIGH, L : LOW, × : don't care, ↑ : rising edge.
2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at K and K# rising edges.
3. All control inputs in the truth table must meet setup/hold times around the rising edge (LOW to HIGH) of K. All control inputs are registered during the rising edge of K.
4. This device contains circuitry that ensure the outputs to be in high impedance during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. It is recommended that K = K# when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.
7. If R# was LOW to initiate the previous cycle, this signal becomes a don't care for this WRITE operation however it is strongly recommended that this signal is brought HIGH as shown in the truth table.
8. W# during write cycle and R# during read cycle were HIGH on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.

Byte Write Operation

[μPD44647094A-A], [μPD44647096A-A]

Operation	K	K#	BW0#
Write D0 to D8	L → H	-	0
	-	L → H	0
Write nothing	L → H	-	1
	-	L → H	1

- Remarks**
1. H : HIGH, L : LOW, → : rising edge.
  2. Assumes a WRITE cycle was initiated. BW0# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

[μPD44647184A-A], [μPD44647186A-A]

Operation	K	K#	BW0#	BW1#
Write D0 to D17	L → H	-	0	0
	-	L → H	0	0
Write D0 to D8	L → H	-	0	1
	-	L → H	0	1
Write D9 to D17	L → H	-	1	0
	-	L → H	1	0
Write nothing	L → H	-	1	1
	-	L → H	1	1

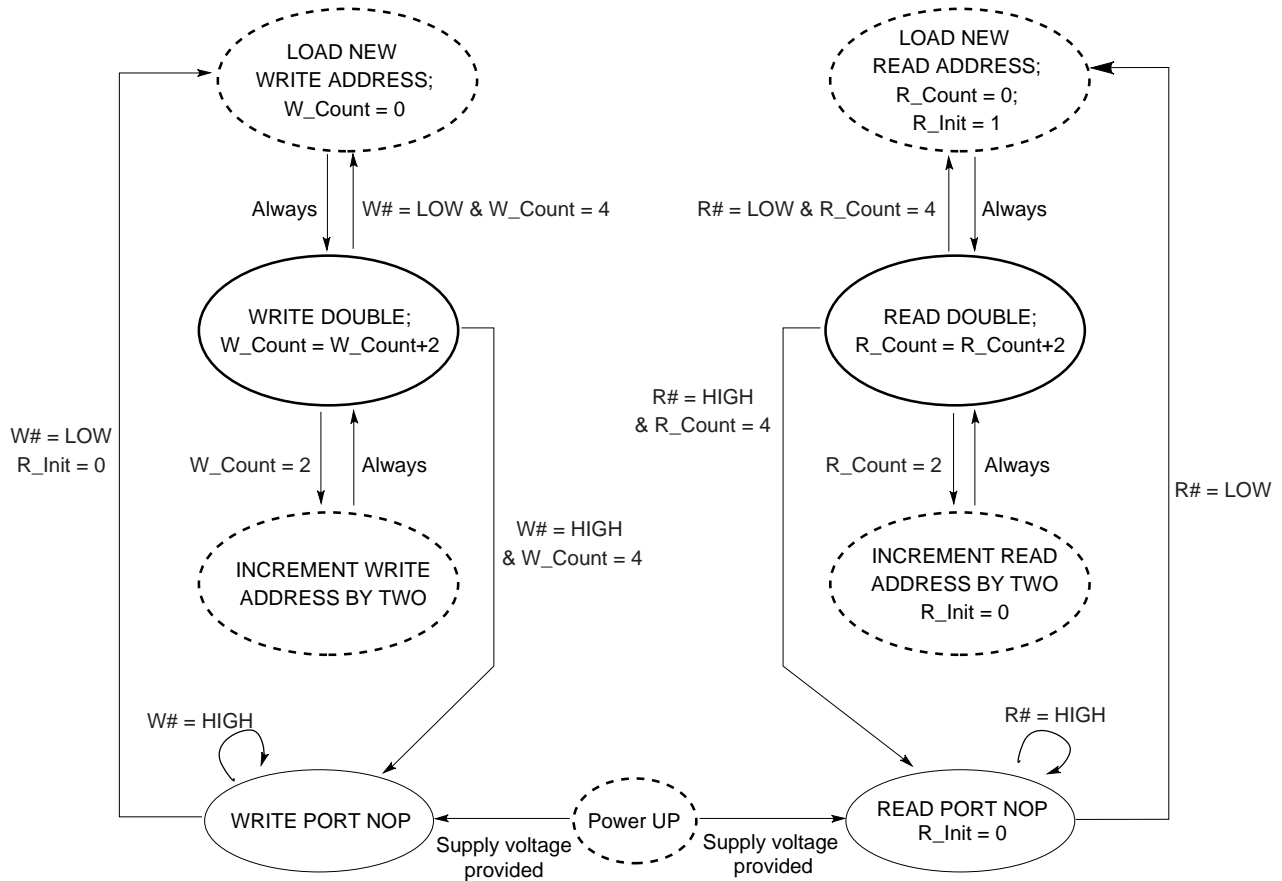
- Remarks**
1. H : HIGH, L : LOW, → : rising edge.
  2. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

[μPD44647364A-A], [μPD44647366A-A]

Operation	K	K#	BW0#	BW1#	BW2#	BW3#
Write D0 to D35	L → H	-	0	0	0	0
	-	L → H	0	0	0	0
Write D0 to D8	L → H	-	0	1	1	1
	-	L → H	0	1	1	1
Write D9 to D17	L → H	-	1	0	1	1
	-	L → H	1	0	1	1
Write D18 to D26	L → H	-	1	1	0	1
	-	L → H	1	1	0	1
Write D27 to D35	L → H	-	1	1	1	0
	-	L → H	1	1	1	0
Write nothing	L → H	-	1	1	1	1
	-	L → H	1	1	1	1

- Remarks**
1. H : HIGH, L : LOW, → : rising edge.
  2. Assumes a WRITE cycle was initiated. BW0# to BW3# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



- Remarks**
1. The address is concatenated with two additional internal LSBs to facilitate burst operation. The address order is always fixed as: xxx...xxx+0, xxx...xxx+1, xxx...xxx+2, xxx...xxx+3. Bus cycle is terminated at the end of this sequence (burst count = 4).
  2. Read and write state machines can be active simultaneously. Read and write cannot be simultaneously initiated. Read takes precedence.
  3. State machine control timing is controlled by K.

**Electrical Specifications**

**Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage	V <sub>DD</sub>		-0.5 to +2.5	V
Output supply voltage	V <sub>DDQ</sub>		-0.5 to V <sub>DD</sub>	V
Input voltage	V <sub>IN</sub>		-0.5 to V <sub>DD</sub> + 0.5 (2.5 V MAX.)	V
Input / Output voltage	V <sub>I/O</sub>		-0.5 to V <sub>DDQ</sub> + 0.5 (2.5 V MAX.)	V
Operating ambient temperature	T <sub>A</sub>		0 to 70	°C
Storage temperature	T <sub>stg</sub>		-55 to +125	°C

**Caution** Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**Recommended DC Operating Conditions (T<sub>A</sub> = 0 to 70°C)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V <sub>DD</sub>		1.7	1.8	1.9	V	
Output supply voltage	V <sub>DDQ</sub>		1.4		V <sub>DD</sub>	V	1
Input HIGH voltage	V <sub>IH</sub> (DC)		V <sub>REF</sub> + 0.1		V <sub>DDQ</sub> + 0.3	V	1, 2
Input LOW voltage	V <sub>IL</sub> (DC)		-0.3		V <sub>REF</sub> - 0.1	V	1, 2
Clock input voltage	V <sub>IN</sub>		-0.3		V <sub>DDQ</sub> + 0.3	V	1, 2
Reference voltage	V <sub>REF</sub>		0.68		0.95	V	

- Notes**
1. During normal operation, V<sub>DDQ</sub> must not exceed V<sub>DD</sub>.
  2. Power-up: V<sub>IH</sub> ≤ V<sub>DDQ</sub> + 0.3 V and V<sub>DD</sub> ≤ 1.7 V and V<sub>DDQ</sub> ≤ 1.4 V for t ≤ 200 ms

**Recommended AC Operating Conditions (T<sub>A</sub> = 0 to 70°C)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit	Note
Input HIGH voltage	V <sub>IH</sub> (AC)		V <sub>REF</sub> + 0.2		V	1
Input LOW voltage	V <sub>IL</sub> (AC)			V <sub>REF</sub> - 0.2	V	1

- Note**
1. Overshoot: V<sub>IH</sub> (AC) ≤ V<sub>DD</sub> + 0.7 V (2.5 V MAX.) for t ≤ TKHKH/2  
 Undershoot: V<sub>IL</sub> (AC) ≥ -0.5 V for t ≤ TKHKH/2  
 Control input signals may not have pulse widths less than TKHKL (MIN.) or operate at cycle rates less than TKHKH (MIN.).



DC Characteristics (T<sub>A</sub> = 0 to 70°C, V<sub>DD</sub> = 1.8 ± 0.1 V)

Parameter	Symbol	Test condition	MIN.	MAX.			Unit	Note
				x9	x18	x36		
Input leakage current	I <sub>LI</sub>		-2	+2			μA	4, 5
I/O leakage current	I <sub>LO</sub>		-2	+2			μA	4
Operating supply current (Read cycle / Write cycle)	I <sub>DD</sub>	V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> I <sub>I/O</sub> = 0 mA Cycle = MAX.	-E20 <sup>Note1</sup>	780	850	1000	mA	
			-E22 <sup>Note1</sup>	730	795	925		
			-E25	690	740	850		
			-E30	580	650	720		
			-E33	520	590	650		
Standby supply current (NOP)	I <sub>SB1</sub>	V <sub>IN</sub> ≤ V <sub>IL</sub> or V <sub>IN</sub> ≥ V <sub>IH</sub> I <sub>I/O</sub> = 0 mA Cycle = MAX. Inputs static	-E20 <sup>Note1</sup>	460	480	530	mA	
			-E22 <sup>Note1</sup>	440	455	500		
			-E25	410	430	470		
			-E30	380	400	440		
			-E33	370	390	430		
Output HIGH voltage	V <sub>OH(Low)</sub>	I <sub>OH</sub>   ≤ 0.1 mA	V <sub>DDQ</sub> - 0.2	V <sub>DDQ</sub>			V	6, 7
	V <sub>OH</sub>	<b>Note2</b>	V <sub>DDQ</sub> /2-0.12	V <sub>DDQ</sub> /2+0.12				6, 7
Output LOW voltage	V <sub>OL(Low)</sub>	I <sub>OL</sub> ≤ 0.1 mA	V <sub>SS</sub>	0.2			V	6, 7
	V <sub>OL</sub>	<b>Note3</b>	V <sub>DDQ</sub> /2-0.12	V <sub>DDQ</sub> /2+0.12				6, 7

- Notes**
- E20 and -E22 are valid for 2.5 Clock Cycles Read Latency products.
  - Outputs are impedance-controlled. |I<sub>OH</sub>| = (V<sub>DDQ</sub>/2)/(R<sub>Q</sub>/5) ±15% for values of 175 Ω ≤ R<sub>Q</sub> ≤ 350 Ω.
  - Outputs are impedance-controlled. I<sub>OL</sub> = (V<sub>DDQ</sub>/2)/(R<sub>Q</sub>/5) ±15% for values of 175 Ω ≤ R<sub>Q</sub> ≤ 350 Ω.
  - Measured with ODT off.
  - ODT pin is internally tied to V<sub>SS</sub>, so input leakage current value is ±5 μA.
  - AC load current is higher than the shown DC values.
  - HSTL outputs meet JEDEC HSTL Class I standards.

Capacitance (T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	MAX.	Unit
Input capacitance (Address, Control)	C <sub>IN</sub>	V <sub>IN</sub> = 0 V		4	pF
Input / Output capacitance (D, Q, CQ, CQ#, QVLD)	C <sub>I/O</sub>	V <sub>I/O</sub> = 0 V		5	pF
Clock Input capacitance	C <sub>clk</sub>	V <sub>clk</sub> = 0 V		4	pF

**Remark** These parameters are periodically sampled and not 100% tested.

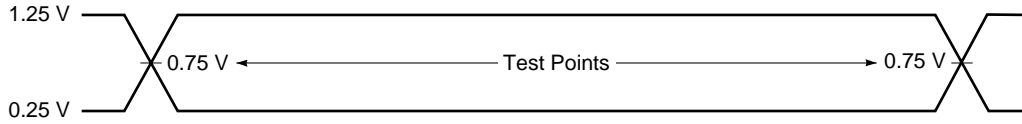
**Thermal Characteristics**

Parameter	Symbol	Substrate	Airflow	TYP.	Unit
Thermal resistance from junction to ambient air	$\theta_{ja}$	4-layer	0 m/s	19.5	°C/W
			1 m/s	12.0	°C/W
		8-layer	0 m/s	18.1	°C/W
			1 m/s	11.3	°C/W
Thermal characterization parameter from junction to the top center of the package surface	$\Psi_{jt}$	4-layer	0 m/s	0.01	°C/W
			1 m/s	0.05	°C/W
		8-layer	0 m/s	0.01	°C/W
			1 m/s	0.04	°C/W
Thermal resistance from junction to case	$\theta_{jc}$			2.14	°C/W

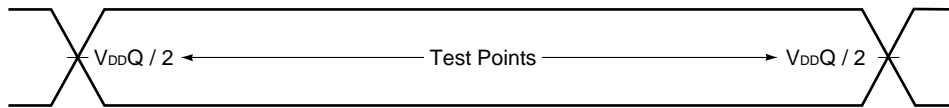
AC Characteristics ( $T_A = 0$  to  $70^\circ\text{C}$ ,  $V_{DD} = 1.8 \pm 0.1$  V)

AC Test Conditions ( $V_{DD} = 1.8 \pm 0.1$  V,  $V_{DDQ} = 1.4$  to  $V_{DD}$ )

Input waveform (Rise / Fall time  $\leq 0.3$  ns)

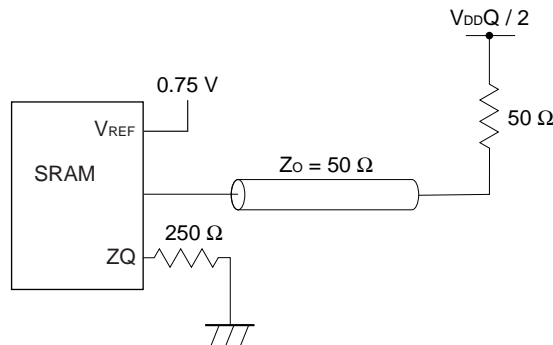


Output waveform



Output load condition

Figure 1. External load at test



Read and Write Cycle

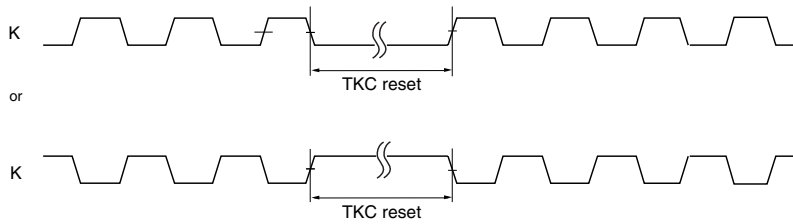
Parameter	Symbol	-E20 <sup>Note1</sup> (500 MHz)		-E22 <sup>Note1</sup> (450 MHz)		-E25 (400 MHz)		-E30 (333 MHz)		-E33 (300 MHz)		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
		<b>Clock</b>											
Average Clock cycle time (K, K#)	TKHKH	2.0	5.25	2.2	5.25	2.5	5.25	3.0	5.25	3.3	5.25	ns	2
Clock phase jitter (K, K#)	TKC var		0.15		0.15		0.20		0.20		0.20	ns	3
Clock HIGH time (K, K#)	TKHKL	0.4		0.4		0.4		0.4		0.4		TKHKH	
Clock LOW time (K, K#)	TKLKH	0.4		0.4		0.4		0.4		0.4		TKHKH	
Clock HIGH to Clock# HIGH (K → K#)	TKHK#H	0.85		0.95		1.06		1.28		1.40		ns	
Clock# HIGH to Clock HIGH (K# → K)	TK#HKH	0.85		0.95		1.06		1.28		1.40		ns	
DLL/PLL lock time (K)	TKC lock	20		20		20		20		20		μs	4
K static to DLL/PLL reset	TKC reset	30		30		30		30		30		ns	5
<b>Output Times</b>													
CQ HIGH to CQ# HIGH (CQ → CQ#)	TCQHCO#H	0.6		0.7		0.81		1.03		1.15		ns	6
CQ# HIGH to CQ HIGH (CQ# → CQ)	TCQ#HCQH	0.6		0.7		0.81		1.03		1.15		ns	6
K, K# HIGH to output valid	TKHQV		0.45		0.45		0.45		0.45		0.45	ns	
K, K# HIGH to output hold	TKHQX	-0.45		-0.45		-0.45		-0.45		-0.45		ns	
K, K# HIGH to echo clock valid	TKHCQV		0.45		0.45		0.45		0.45		0.45	ns	
K, K# HIGH to echo clock hold	TKHCQX	-0.45		-0.45		-0.45		-0.45		-0.45		ns	
CQ, CQ# HIGH to output valid	TCQHCV		0.15		0.15		0.20		0.20		0.20	ns	7
CQ, CQ# HIGH to output hold	TCQHCV	-0.15		-0.15		-0.20		-0.20		-0.20		ns	7
K HIGH to output High-Z	TKHQZ		0.45		0.45		0.45		0.45		0.45	ns	
K HIGH to output Low-Z	TKHQX1	-0.45		-0.45		-0.45		-0.45		-0.45		ns	
CQ, CQ# HIGH to QVLD valid	TCQHCVLD	-0.15	0.15	-0.15	0.15	-0.20	0.20	-0.20	0.20	-0.20	0.20	ns	
<b>Setup Times</b>													
Address valid to K rising edge	TAVKH	0.33		0.4		0.4		0.4		0.4		ns	8
Control inputs (R#, W#) valid to K rising edge	TIVKH	0.33		0.4		0.4		0.4		0.4		ns	8
Data inputs and write data select inputs (BWx#) valid to K, K# rising edge	TDVKH	0.25		0.28		0.28		0.28		0.28		ns	8
<b>Hold Times</b>													
K rising edge to address hold	TKHAX	0.33		0.4		0.4		0.4		0.4		ns	8
K rising edge to control inputs (R#, W#) hold	TKHIX	0.33		0.4		0.4		0.4		0.4		ns	8
K, K# rising edge to data inputs and write data select inputs (BWx#) hold	TKHDX	0.25		0.28		0.28		0.28		0.28		ns	8

**Notes** 1. -E20 and -E22 are valid for 2.5 Clock Cycles Read Latency products.

2. When debugging the system or board, these products can operate at a clock frequency slower than TKHKH (MAX.) without the DLL/PLL circuit being used, if DLL# = LOW. Read latency (RL) is changed to 1.0 clock cycle regardless of RL = 2.0 and 2.5 clock cycles products in this operation. The AC/DC characteristics cannot be guaranteed, however.

3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge. TKC var (MAX.) indicates a peak-to-peak value.

- 4. V<sub>DD</sub> slew rate must be less than 0.1 V DC per 50 ns for DLL/PLL lock retention.  
 DLL/PLL lock time begins once V<sub>DD</sub> and input clock are stable.  
 It is recommended that the device is kept NOP (R# = W# = HIGH) during these cycles.
- 5. K input is monitored for this operation. See below for the timing.



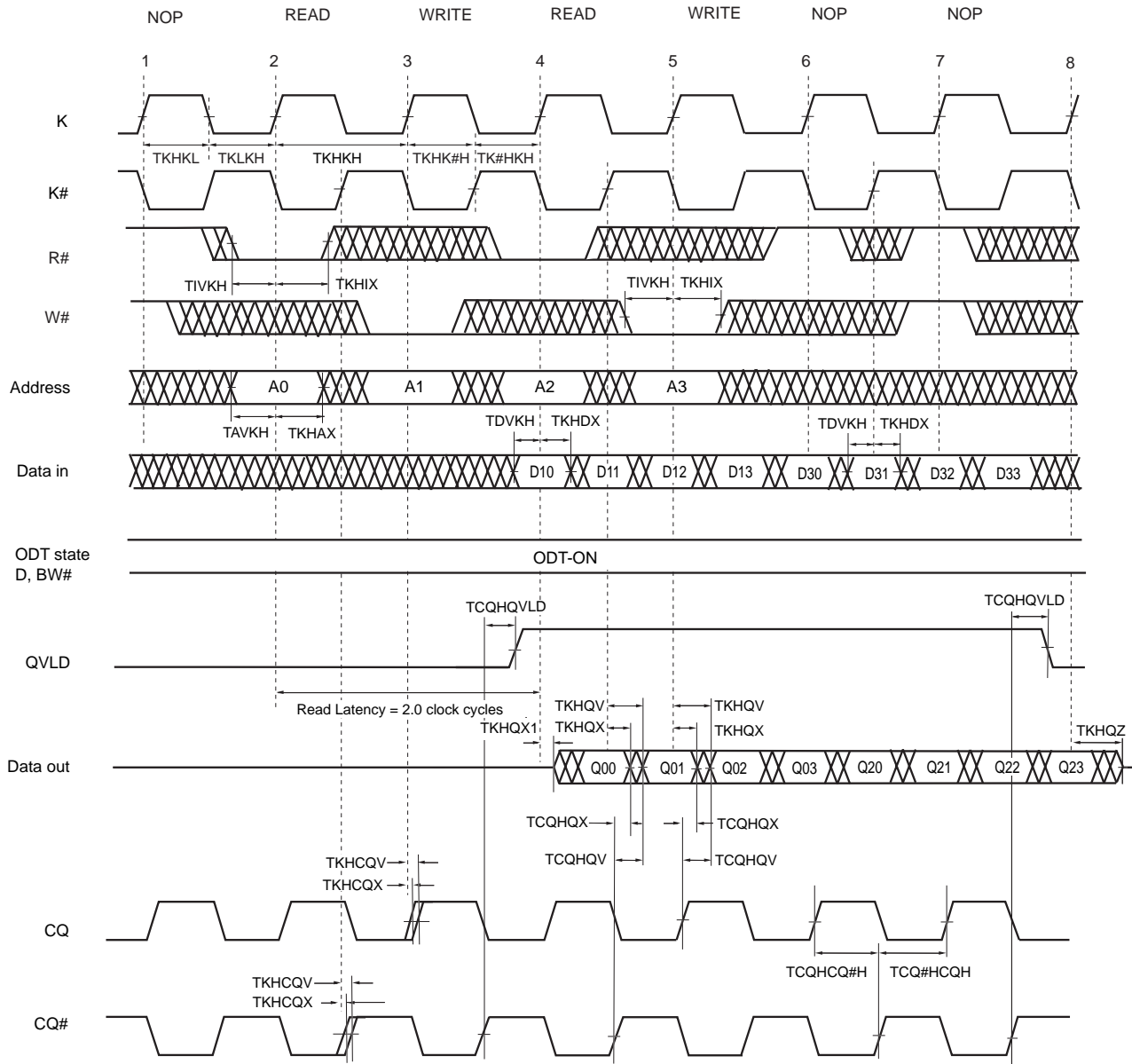
- 6. Guaranteed by design.
- 7. Echo clock is very tightly controlled to data valid / data hold. By design, there is a  $\pm 0.1$  ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.
- 8. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

- Remarks**
- 1. This parameter is sampled.
  - 2. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
  - 3. Control input signals may not be operated with pulse widths less than TKHKL (MIN.).
  - 4. V<sub>DDQ</sub> is 1.5 V DC.

Read and Write Timing

2.0 Clock Cycles Read Latency

[μPD44647094A-A], [μPD44647184A-A], [μPD44647364A-A]



**Remarks 1.** Q00 refers to output from address A0+0.

Q01 refers to output from the next internal burst address following A0, i.e., A0+1.

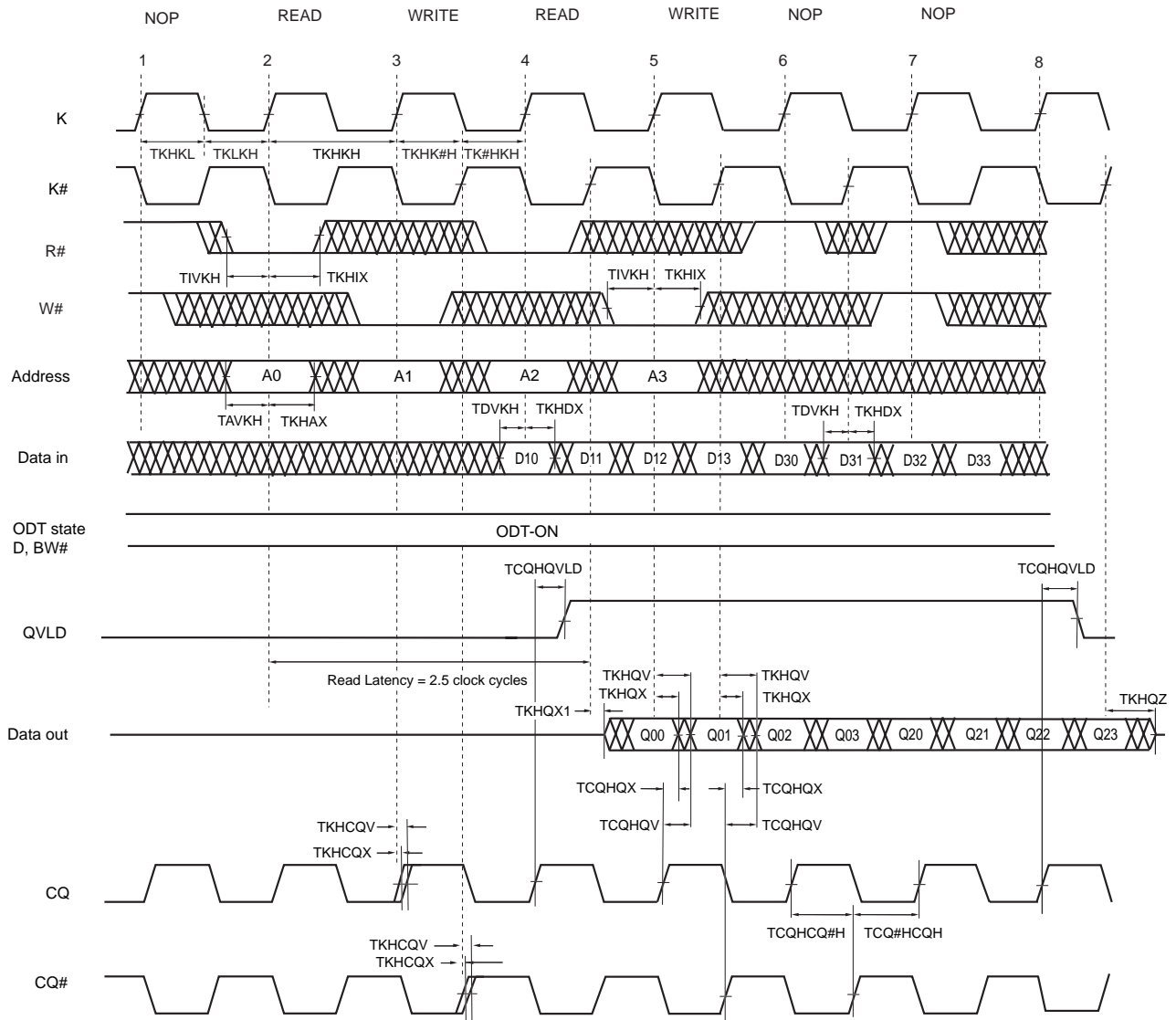
**2.** Outputs are disabled (high impedance) 4.0 clock cycles after the last READ (R# = LOW) is input in the sequences of [READ]-[NOP]-[NOP], [READ]-[WRITE]-[NOP] and [READ]-[NOP]-[WRITE].

**3.** In this example, if address A2 = A1, data Q20 = D10, Q21 = D11, Q22 = D12 and Q23 = D13. Write data is forwarded immediately as read results. This remark applies to whole diagram.

**4.** When the ODT control pin is LOW or No Connect, the ODT function is always off.

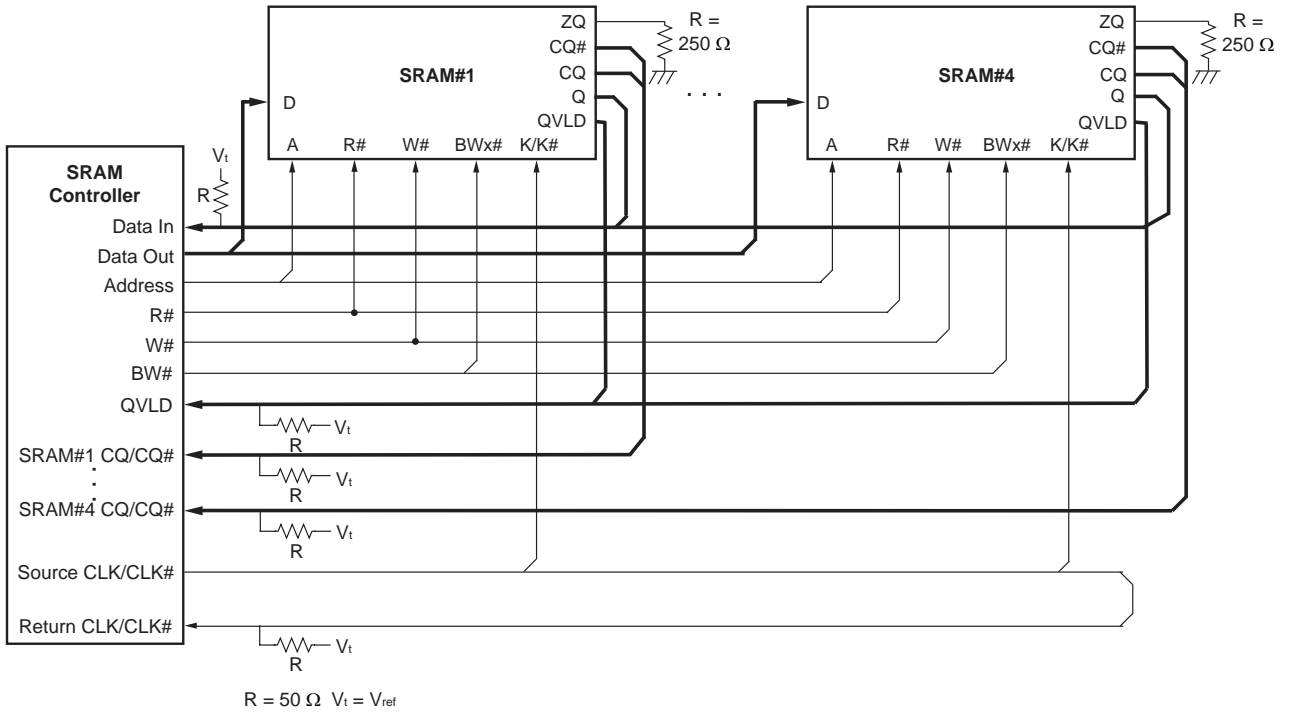
2.5 Clock Cycles Read Latency

[μPD44647096A-A], [μPD44647186A-A], [μPD44647366A-A]



- Remarks**
1. Q00 refers to output from address A0+0.  
Q01 refers to output from the next internal burst address following A0, i.e., A0+1.
  2. Outputs are disabled (high impedance) 4.5 clock cycles after the last READ (R# = LOW) is input in the sequences of [READ]-[NOP]-[NOP], [READ]-[WRITE]-[NOP] and [READ]-[NOP]-[WRITE].
  3. In this example, if address A2 = A1, data Q20 = D10, Q21 = D11, Q22 = D12 and Q23 = D13.  
Write data is forwarded immediately as read results. This remark applies to the whole diagram.
  4. When the ODT control pin is LOW or No Connect, the ODT function is always off.

Application Example



**Remark** AC specifications are defined at the condition of SRAM outputs, CQ, CQ#, QVLD and Q with termination. Ds and BW#s have ODT.



**JTAG Specification**

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

**Test Access Port (TAP) Pins**

Pin name	Pin assignments	Description
TCK	2R	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	11R	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.

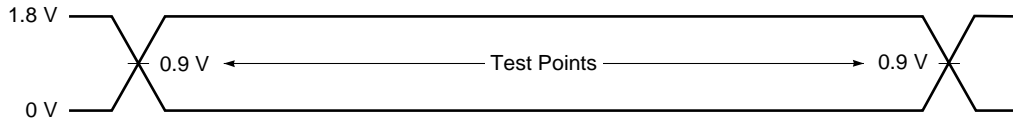
**Remark** The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

**JTAG DC Characteristics (T<sub>A</sub> = 0 to 70°C, V<sub>DD</sub> = 1.8 ± 0.1 V, unless otherwise noted)**

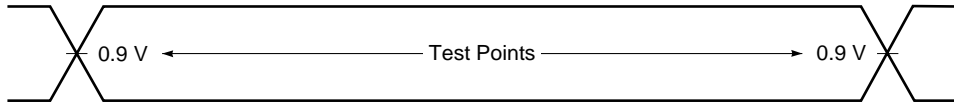
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
JTAG Input leakage current	I <sub>LI</sub>	0 V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub>	-5.0	+5.0	μA
JTAG I/O leakage current	I <sub>LO</sub>	0 V ≤ V <sub>IN</sub> ≤ V <sub>DDQ</sub> , Outputs disabled	-5.0	+5.0	μA
JTAG input HIGH voltage	V <sub>IH</sub>		1.3	V <sub>DD</sub> +0.3	V
JTAG input LOW voltage	V <sub>IL</sub>		-0.3	+0.5	V
JTAG output HIGH voltage	V <sub>OH1</sub>	I <sub>OHC</sub>   = 100 μA	1.6		V
	V <sub>OH2</sub>	I <sub>OHT</sub>   = 2 mA	1.4		V
JTAG output LOW voltage	V <sub>OL1</sub>	I <sub>OLC</sub> = 100 μA		0.2	V
	V <sub>OL2</sub>	I <sub>OLT</sub> = 2 mA		0.4	V

JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 1 ns)

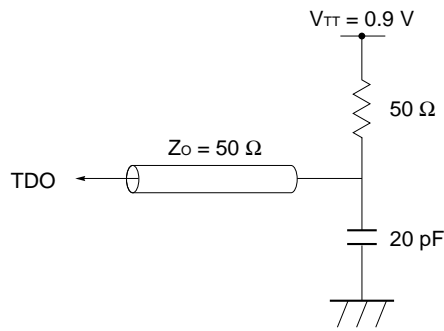


Output waveform



Output load

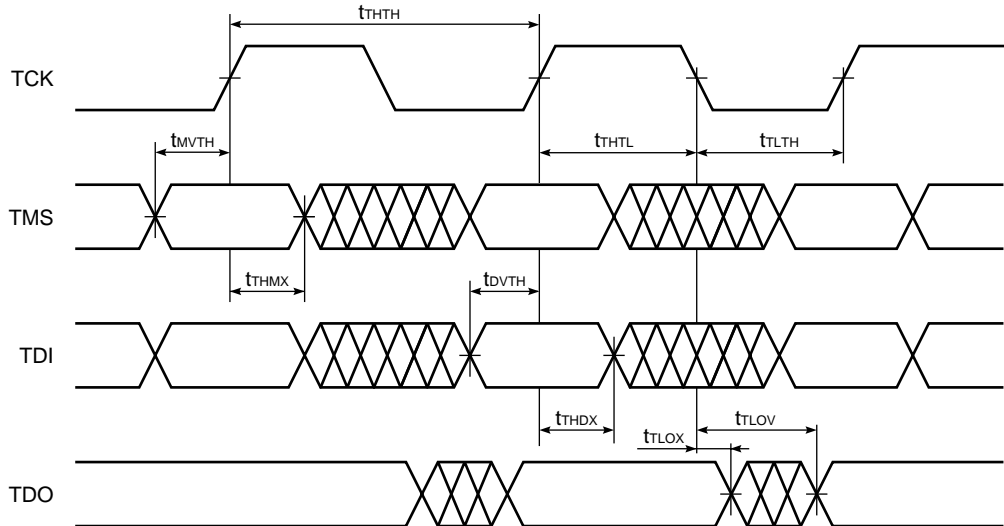
Figure 2. External load at test



JTAG AC Characteristics (T<sub>A</sub> = 0 to 70°C)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
<b>Clock</b>					
Clock cycle time	t <sub>THTH</sub>		50		ns
Clock frequency	f <sub>TF</sub>			20	MHz
Clock HIGH time	t <sub>HTL</sub>		20		ns
Clock LOW time	t <sub>TLH</sub>		20		ns
<b>Output time</b>					
TCK LOW to TDO unknown	t <sub>TLOX</sub>		0		ns
TCK LOW to TDO valid	t <sub>TLOV</sub>			10	ns
<b>Setup time</b>					
TMS setup time	t <sub>MVTH</sub>		5		ns
TDI valid to TCK HIGH	t <sub>DVTH</sub>		5		ns
Capture setup time	t <sub>CS</sub>		5		ns
<b>Hold time</b>					
TMS hold time	t <sub>THMX</sub>		5		ns
TCK HIGH to TDI invalid	t <sub>THDX</sub>		5		ns
Capture hold time	t <sub>CH</sub>		5		ns

JTAG Timing Diagram



**Scan Register Definition (1)**

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register.  The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

**Scan Register Definition (2)**

Register name	Bit size	Unit
Instruction register	3	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	109	bit

**ID Register Definition**

**2.0 Clock Cycles Read Latency**

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44647094A-A	8M x 9	XXXX	0000 0000 1001 0101	00000010000	1
μPD44647184A-A	4M x 18	XXXX	0000 0000 1001 0110	00000010000	1
μPD44647364A-A	2M x 36	XXXX	0000 0000 1001 0111	00000010000	1

**2.5 Clock Cycles Read Latency**

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44647096A-A	8M x 9	XXXX	0000 0000 1010 0001	00000010000	1
μPD44647186A-A	4M x 18	XXXX	0000 0000 1010 0010	00000010000	1
μPD44647366A-A	2M x 36	XXXX	0000 0000 1010 0011	00000010000	1

SCAN Exit Order

Bit no.	Signal name			Bump ID
	x9	x18	x36	
1	ODT			6R
2	QVLD			6P
3	A			6N
4	A			7P
5	A			7N
6	A			7R
7	A			8R
8	A			8P
9	A			9R
10	Q0			11P
11	D0			10P
12	NC	NC	D9	10N
13	NC	NC	Q9	9P
14	NC	Q1	Q1	10M
15	NC	D1	D1	11N
16	NC	NC	D10	9M
17	NC	NC	Q10	9N
18	Q1	Q2	Q2	11L
19	D1	D2	D2	11M
20	NC	NC	D11	9L
21	NC	NC	Q11	10L
22	NC	Q3	Q3	11K
23	NC	D3	D3	10K
24	NC	NC	D12	9J
25	NC	NC	Q12	9K
26	Q2	Q4	Q4	10J
27	D2	D4	D4	11J
28	ZQ			11H
29	NC	NC	D13	10G
30	NC	NC	Q13	9G
31	NC	Q5	Q5	11F
32	NC	D5	D5	11G
33	NC	NC	D14	9F
34	NC	NC	Q14	10F
35	Q3	Q6	Q6	11E
36	D3	D6	D6	10E

Bit no.	Signal name			Bump ID
	x9	x18	x36	
37	NC	NC	D15	10D
38	NC	NC	Q15	9E
39	NC	Q7	Q7	10C
40	NC	D7	D7	11D
41	NC	NC	D16	9C
42	NC	NC	Q16	9D
43	Q4	Q8	Q8	11B
44	D4	D8	D8	11C
45	NC	NC	D17	9B
46	NC	NC	Q17	10B
47	CQ			11A
48	A	A	NC	10A
49	A			9A
50	A			8B
51	A			7C
52	NC			6C
53	R#			8A
54	NC	NC	BW1#	7A
55	BW0#			7B
56	K			6B
57	K#			6A
58	NC	NC	BW3#	5B
59	NC	BW1#	BW2#	5A
60	W#			4A
61	A			5C
62	A			4B
63	A			3A
64	A	NC	NC	2A
65	CQ#			1A
66	NC	Q9	Q18	2B
67	NC	D9	D18	3B
68	NC	NC	D27	1C
69	NC	NC	Q27	1B
70	NC	Q10	Q19	3D
71	NC	D10	D19	3C
72	NC	NC	D28	1D

Bit no.	Signal name			Bump ID
	x9	x18	x36	
73	NC	NC	Q28	2C
74	Q5	Q11	Q20	3E
75	D5	D11	D20	2D
76	NC	NC	D29	2E
77	NC	NC	Q29	1E
78	NC	Q12	Q21	2F
79	NC	D12	D21	3F
80	NC	NC	D30	1G
81	NC	NC	Q30	1F
82	Q6	Q13	Q22	3G
83	D6	D13	D22	2G
84	DLL#			1H
85	NC	NC	D31	1J
86	NC	NC	Q31	2J
87	NC	Q14	Q23	3K
88	NC	D14	D23	3J
89	NC	NC	D32	2K
90	NC	NC	Q32	1K
91	Q7	Q15	Q24	2L
92	D7	D15	D24	3L
93	NC	NC	D33	1M
94	NC	NC	Q33	1L
95	NC	Q16	Q25	3N
96	NC	D16	D25	3M
97	NC	NC	D34	1N
98	NC	NC	Q34	2M
99	Q8	Q17	Q26	3P
100	D8	D17	D26	2N
101	NC	NC	D35	2P
102	NC	NC	Q35	1P
103	A			3R
104	A			4R
105	A			4P
106	A			5P
107	A			5N
108	A			5R
109	-			Internal

**JTAG Instructions**

Instructions	Description
EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE / PRELOAD	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and Q pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time ( $t_{cs}$ plus $t_{ch}$ ). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM Q pins are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

**JTAG Instruction Coding**

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	RESERVED	2
1	0	0	SAMPLE / PRELOAD	
1	0	1	RESERVED	2
1	1	0	RESERVED	2
1	1	1	BYPASS	

- Notes**
1. TRISTATE all Q pins and CAPTURE the pad values into a SERIAL SCAN LATCH.
  2. Do not use this instruction code because the vendor uses it to evaluate this product.

Output Pin States of CQ, CQ#, QVLD and Q

Instructions	Control-Register Status	Output Pin Status	
		CQ, CQ#, QVLD	Q
EXTEST	0	Update	High-Z
	1	Update	Update
IDCODE	0	SRAM	SRAM
	1	SRAM	SRAM
SAMPLE-Z	0	High-Z	High-Z
	1	High-Z	High-Z
SAMPLE	0	SRAM	SRAM
	1	SRAM	SRAM
BYPASS	0	SRAM	SRAM
	1	SRAM	SRAM

**Remark** The output pin statuses during each instruction vary according to the Control-Register status (value of Boundary Scan Register, bit no. 109).

There are three statuses:

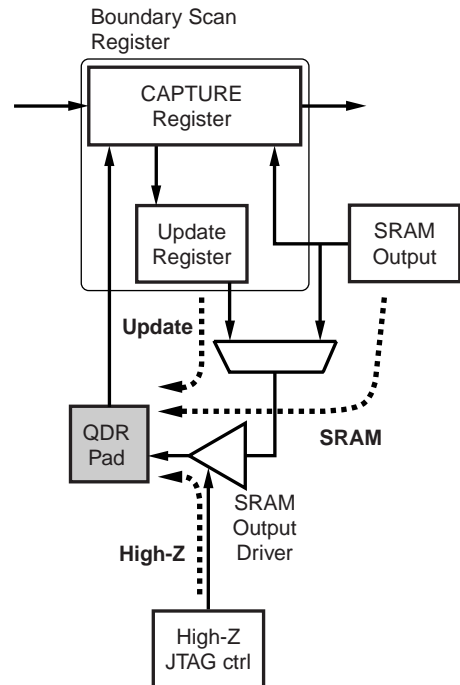
**Update** : Contents of the "Update Register" are output to the output pin (QDR Pad).

**SRAM** : Contents of the SRAM internal output "SRAM Output" are output to the output pin (QDR Pad).

**High-Z** : The output pin (QDR Pad) becomes high impedance by controlling of the "High-Z JTAG ctrl".

The Control-Register status is set during Update-DR at the EXTEST or SAMPLE instruction.

In case checking the QVLD output status in EXTEST mode, please make sure stay DLL# pin HIGH.



Boundary Scan Register Status of Output Pins CQ, CQ#, QVLD and Q

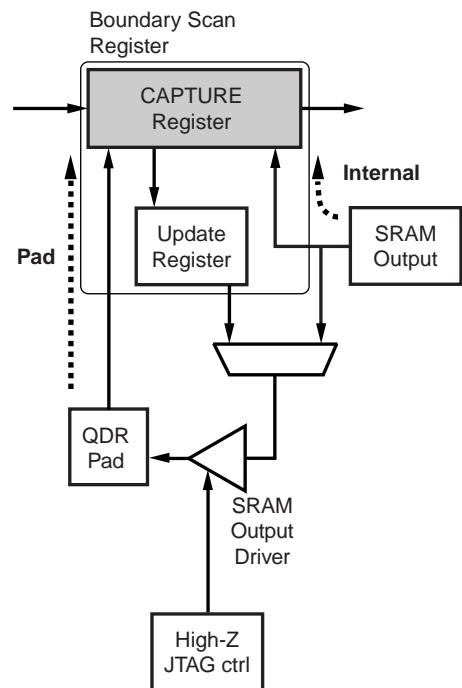
Instructions	SRAM Status	Boundary Scan Register Status		Note
		CQ, CQ#, QVLD	Q	
EXTEST	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
IDCODE	READ (Low-Z)	-	-	No definition
	NOP (High-Z)	-	-	
SAMPLE-Z	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
SAMPLE	READ (Low-Z)	Internal	Internal	
	NOP (High-Z)	Internal	Pad	
BYPASS	READ (Low-Z)	-	-	No definition
	NOP (High-Z)	-	-	

**Remark** The Boundary Scan Register statuses during execution each instruction vary according to the instruction code and SRAM operation mode.

There are two statuses:

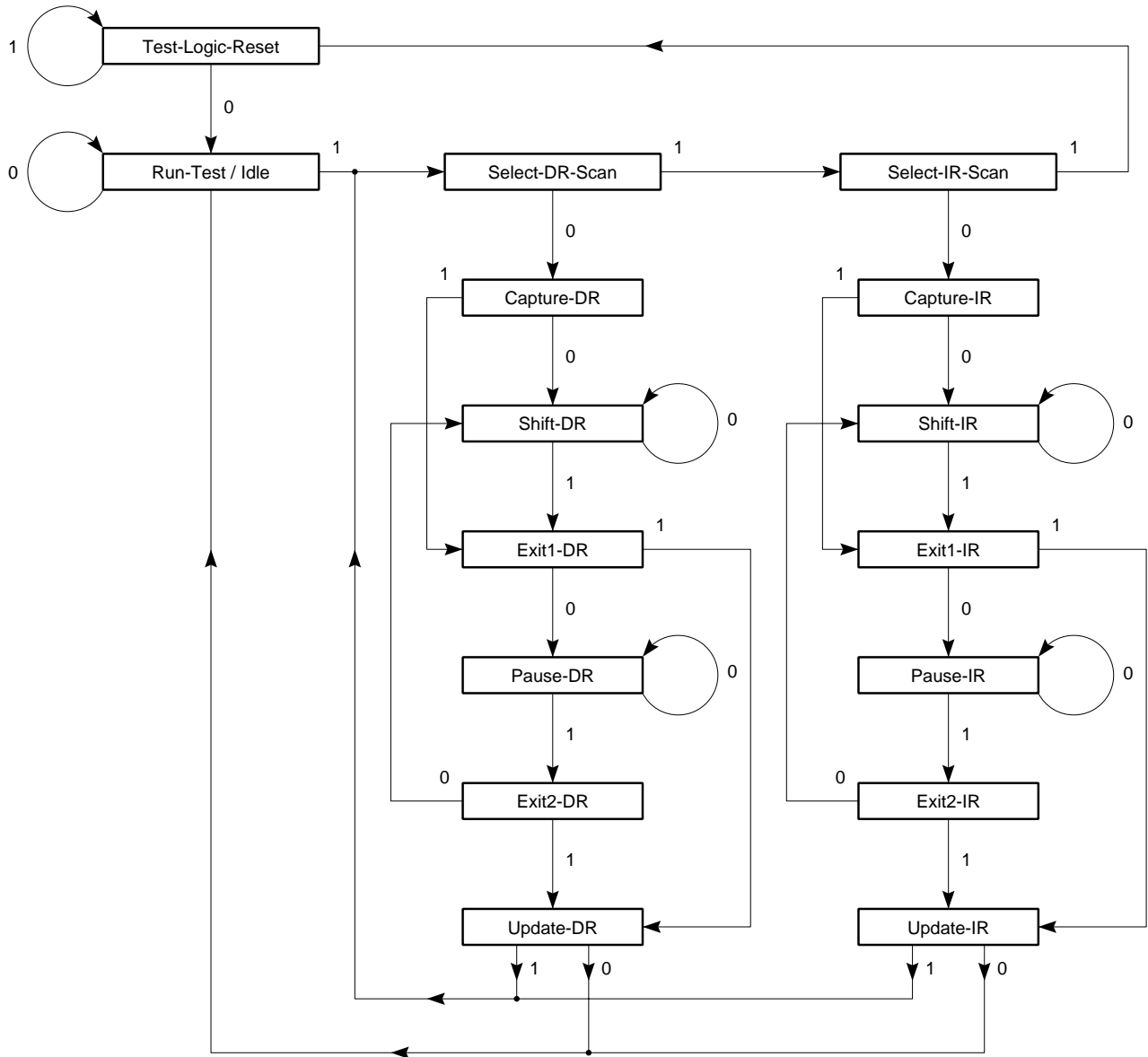
**Pad** : Contents of the output pin (QDR Pad) are captured in the "CAPTURE Register" in the Boundary Scan Register.

**Internal** : Contents of the SRAM internal output "SRAM Output" are captured in the "CAPTURE Register" in the Boundary Scan Register.





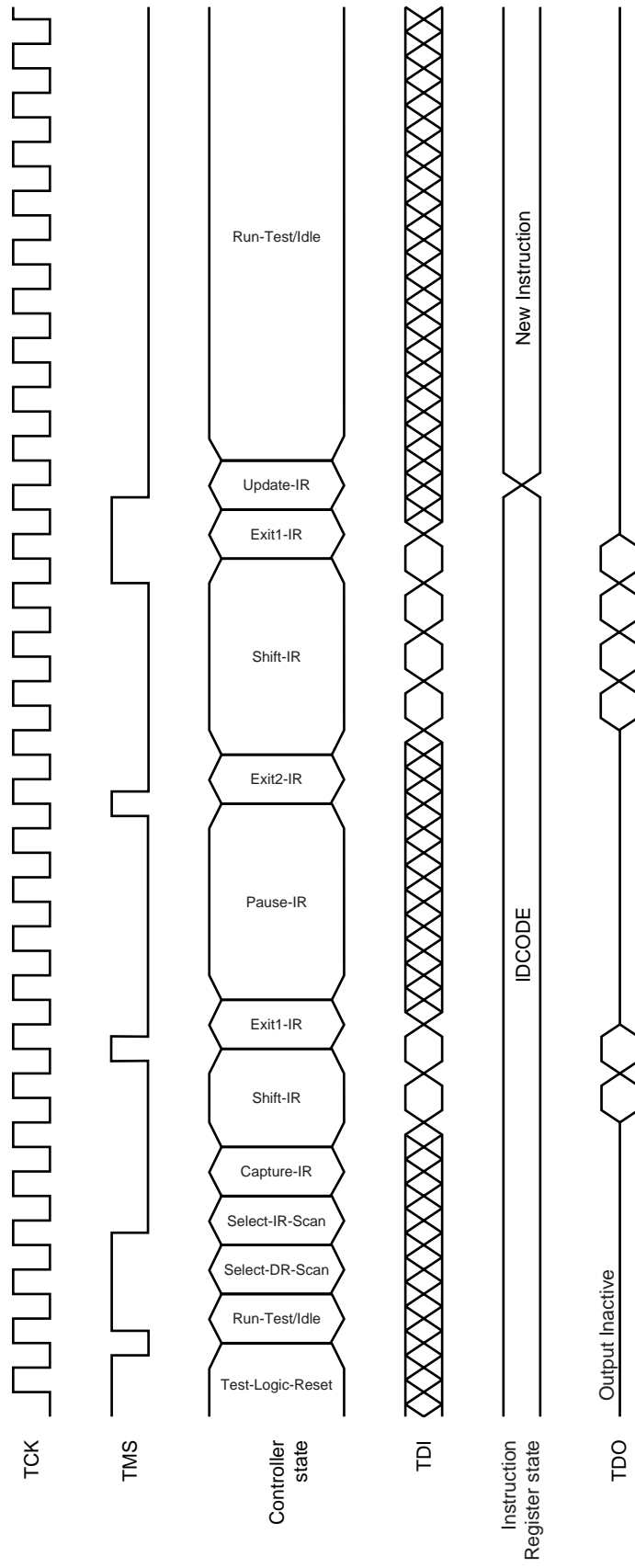
TAP Controller State Diagram



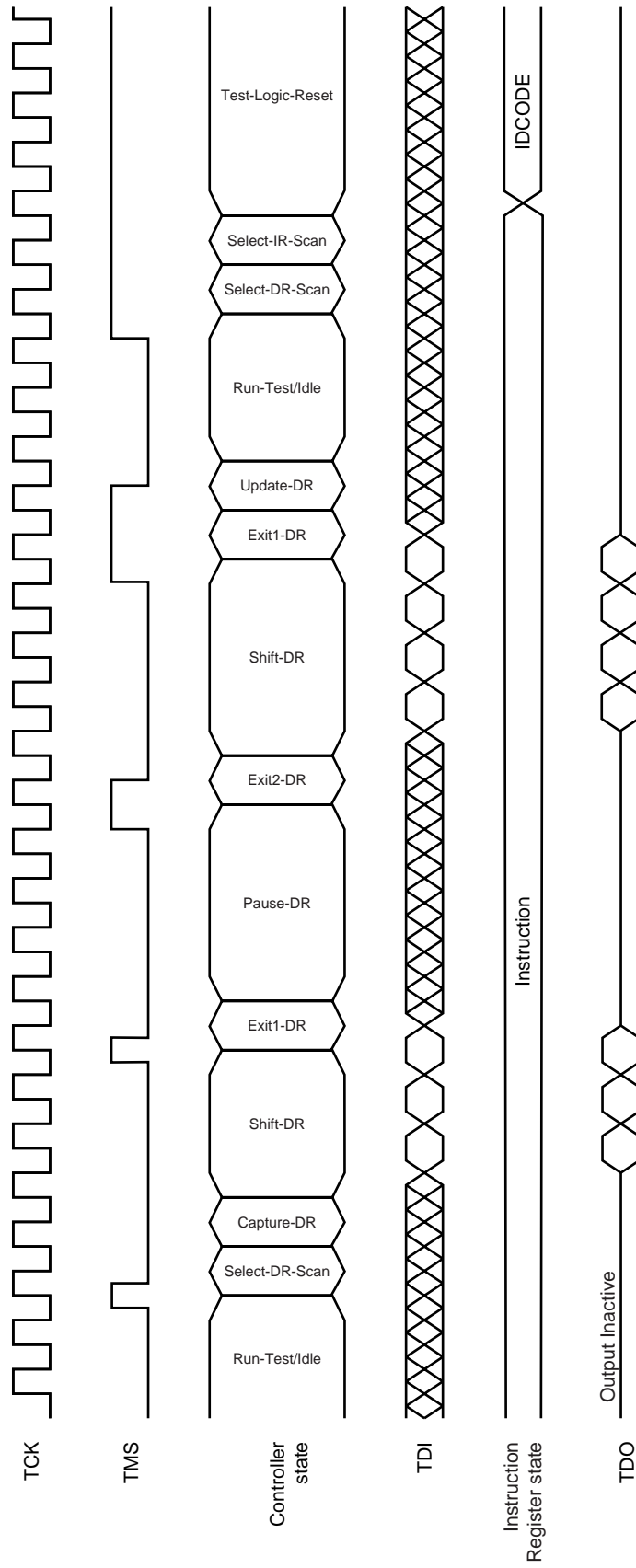
Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to Vss to preclude mid level inputs. TDI and TMS may be left open but fix them to VDD via a resistor of about 1 kΩ when the TAP controller is not used. TDO should be left unconnected also when the TAP controller is not used.

Test Logic Operation (Instruction Scan)

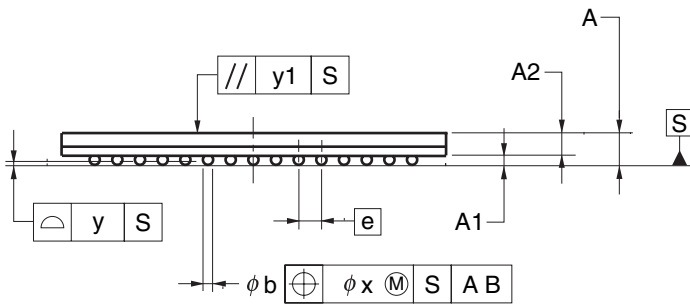
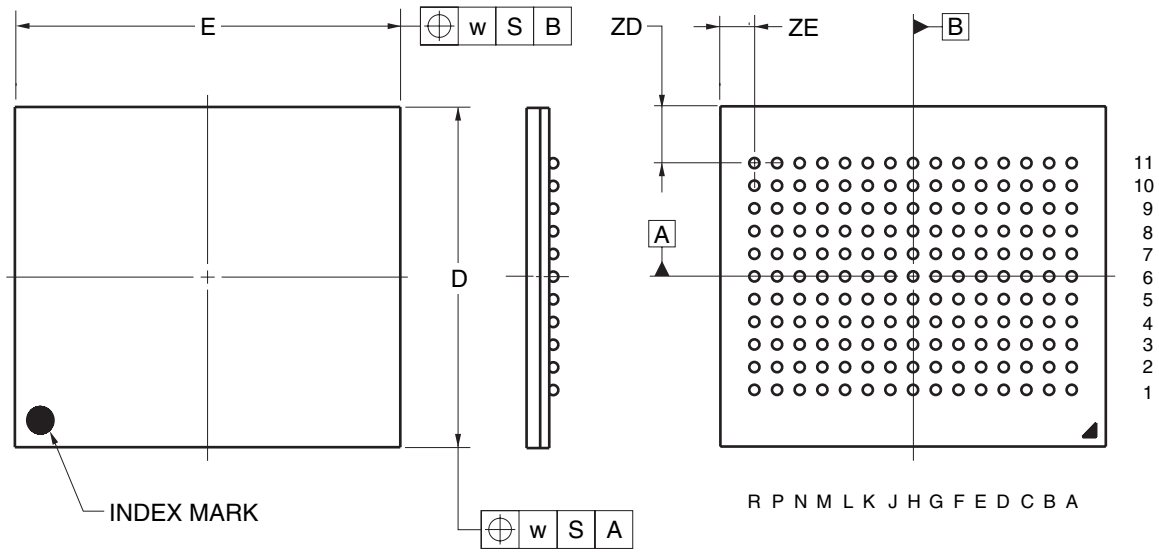


Test Logic (Data Scan)



Package Drawing

165-PIN PLASTIC BGA(15x17)



(UNIT:mm)

ITEM	DIMENSIONS
D	15.00±0.10
E	17.00±0.10
w	0.30
A	1.35±0.11
A1	0.37±0.05
A2	0.98
e	1.00
b	0.50 <sup>+0.10</sup> <sub>-0.05</sub>
x	0.10
y	0.15
y1	0.25
ZD	2.50
ZE	1.50

P165F5-100-FQ1-1

© NEC Electronics Corporation 2009

**Recommended Soldering Condition**

Please consult with our sales offices for soldering conditions of these products.

**Types of Surface Mount Devices**

- μPD44647094AF5-FQ1-A : 165-pin PLASTIC BGA (15 x 17), Lead free
- μPD44647184AF5-FQ1-A : 165-pin PLASTIC BGA (15 x 17), Lead free
- μPD44647364AF5-FQ1-A : 165-pin PLASTIC BGA (15 x 17), Lead free
- μPD44647096AF5-FQ1-A : 165-pin PLASTIC BGA (15 x 17), Lead free
- μPD44647186AF5-FQ1-A : 165-pin PLASTIC BGA (15 x 17), Lead free
- μPD44647366AF5-FQ1-A : 165-pin PLASTIC BGA (15 x 17), Lead free

**Related Document**

Document Name	Document Number
μPD44647094A, 44647184A, 44647364A, 44647096A, 44647186A, 44647366A Data Sheet (Leaded products)	M19063

**Quality Grade**

- A quality grade of the products is "Standard".
- Anti-radioactive design is not implemented in the products.
- Semiconductor devices have the possibility of unexpected defects by affection of cosmic ray that reach to the ground and so forth.

**Revision History**

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
2nd edition/ Mar. 2010	Throughout	Throughout	Modification		Preliminary Data Sheet    Data Sheet

[MEMO]

[MEMO]



## NOTES FOR CMOS DEVICES

**① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (MAX) and  $V_{IH}$  (MIN).

**② HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

**③ PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

**④ STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

**⑤ POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

**⑥ INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

QDR RAMs and Quad Data Rate RAMs comprise a new series of products developed by Cypress Semiconductor, Renesas, IDT, NEC Electronics, and Samsung.

- **The information in this document is current as of March, 2010. The information is subject to change without notice. For actual design-in, refer to the latest publications of NEC Electronics data sheets, etc., for the most up-to-date specifications of NEC Electronics products. Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.**

- No part of this document may be copied or reproduced in any form or by any means without the prior written consent of NEC Electronics. NEC Electronics assumes no responsibility for any errors that may appear in this document.
- NEC Electronics does not assume any liability for infringement of patents, copyrights or other intellectual property rights of third parties by or arising from the use of NEC Electronics products listed in this document or any other liability arising from the use of such products. No license, express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of NEC Electronics or others.
- Descriptions of circuits, software and other related information in this document are provided for illustrative purposes in semiconductor product operation and application examples. The incorporation of these circuits, software and information in the design of a customer's equipment shall be done under the full responsibility of the customer. NEC Electronics assumes no responsibility for any losses incurred by customers or third parties arising from the use of these circuits, software and information.
- While NEC Electronics endeavors to enhance the quality and safety of NEC Electronics products, customers agree and acknowledge that the possibility of defects thereof cannot be eliminated entirely. In addition, NEC Electronics products are not taken measures to prevent radioactive rays in the product design. When customers use NEC Electronics products with their products, customers shall, on their own responsibility, incorporate sufficient safety measures such as redundancy, fire-containment and anti-failure features to their products in order to avoid risks of the damages to property (including public or social property) or injury (including death) to persons, as the result of defects of NEC Electronics products.
- NEC Electronics products are classified into the following three quality grades: "Standard", "Special" and "Specific".

The "Specific" quality grade applies only to NEC Electronics products developed based on a customer-designated "quality assurance program" for a specific application. The recommended applications of an NEC Electronics product depend on its quality grade, as indicated below. Customers must check the quality grade of each NEC Electronics product before using it in a particular application.

"Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots.

"Special": Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support).

"Specific": Aircraft, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems and medical equipment for life support, etc.

The quality grade of NEC Electronics products is "Standard" unless otherwise expressly specified in NEC Electronics data sheets or data books, etc. If customers wish to use NEC Electronics products in applications not intended by NEC Electronics, they must contact an NEC Electronics sales representative in advance to determine NEC Electronics' willingness to support a given application.

(Note)

(1) "NEC Electronics" as used in this statement means NEC Electronics Corporation and also includes its majority-owned subsidiaries.

(2) "NEC Electronics products" means any product developed or manufactured by or for NEC Electronics (as defined above).