R8A66165SP / R8A66166SP / R8A66167SP / R8A66168SP

n-BIT HIGH VOLTAGE OUTPUT LED DRIVER WITH SHIFT REGISTER AND LATCH

REJ03F0281-0101
Rev. 1.01
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DESCRIPTION

R8A66165～R8A66168 are high voltage LED array driver having n-bit serial input and parallel output shift register function with direct coupled reset input and output latch function.
These products guarantees the output current of 24mA which is sufficient for anode common LED drive, capable of following n-bits continuously at the same time. Parallel output is 24V high voltage open drain output.
In addition, as this product has been designed in complete CMOS, power consumption can be greatly reduced when compared with conventional BIPOLAR or Bi-CMOS products.
The product part number and the parallel data outputs number are shown in the following table.

Part number	Parallel data outputs number n	$\overline{Q1}$～$\overline{Qn}$	SQn
R8A66165SP	8-Bit	$\overline{Q1}$～$\overline{Q8}$	SQ8
R8A66166SP	16-Bit	$\overline{Q1}$～$\overline{Q16}$	SQ16
R8A66167SP	24-Bit	$\overline{Q1}$～$\overline{Q24}$	SQ24
R8A66168SP	32-Bit	$\overline{Q1}$～$\overline{Q32}$	SQ32

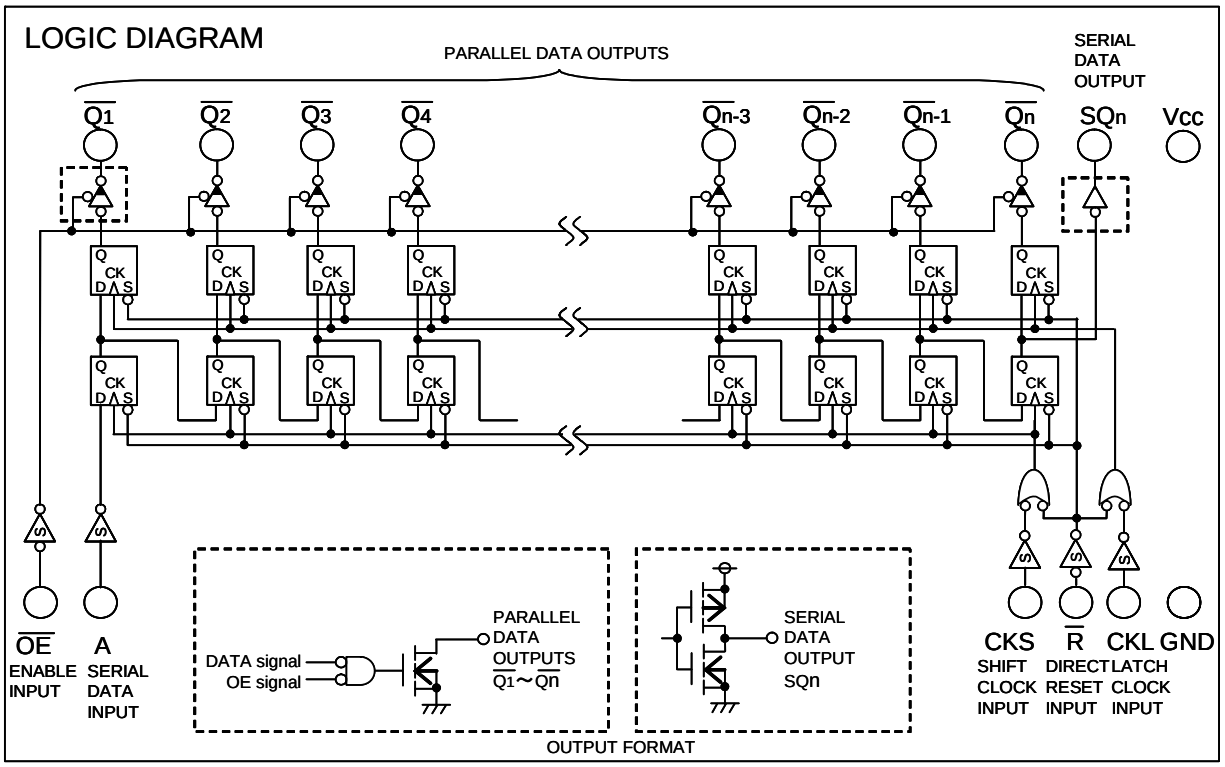
FEATURES

- Anode common LED drive
- V_{CC} 5V or 3.3V single power supply
- High voltage, High output current: all parallel outputs $\overline{Q1}$～$\overline{Qn}$ V_O =24V high voltage, I_{OL} =24mA simultaneous lighting available
- Low power dissipation: 100uW/package (max) (V_{CC} =5.0V, Ta =25℃, quiescent state)
- High noise margin: Schmitt input circuit provides responsiveness to a long line length
- Equipped with direct-coupled reset
- Open drain output: (except serial data output SQn)
- Wide operating temperature range: Ta = -40℃~+85℃

APPLICATION

- LED array drive, The various high voltage LED display modules

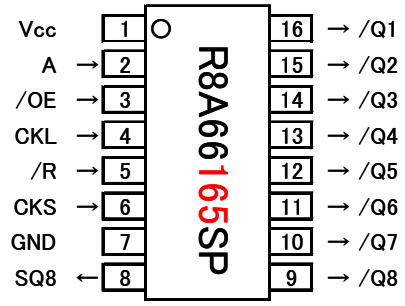
BLOCK DIAGRAM

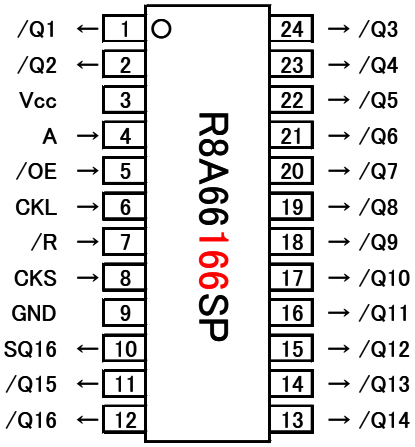


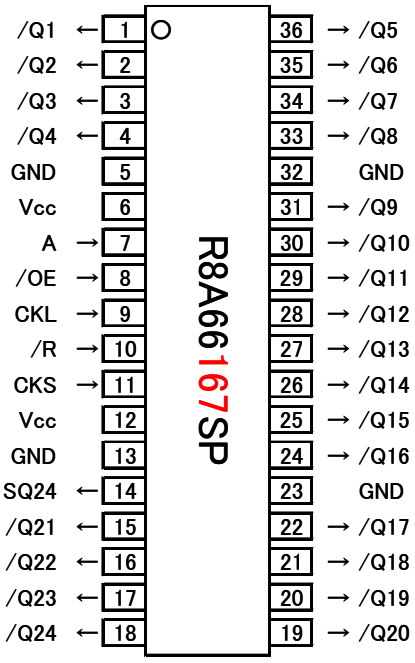
PIN SPECIFICATION

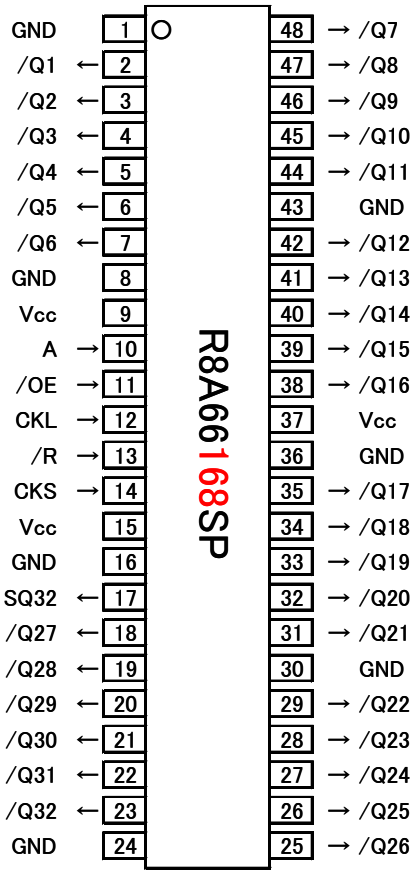
Pin Name	Symbol	In/Out	R8A66165SP 8-BIT	R8A66166SP 16-BIT	R8A66167SP 24-BIT	R8A66168SP 32-BIT
DIRECT RESET INPUT	/R	Input	1	1	1	1
SERIAL DATA INPUT	A	Input	1	1	1	1
SHIFT CLOCK INPUT	CKS	Input	1	1	1	1
LATCH CLOCK INPUT	CKL	Input	1	1	1	1
ENABLE INPUT	/OE	Input	1	1	1	1
PARALLEL DATA OUTPUTS	/Q1～/Qn	Output	8	16	24	32
SERIAL DATA OUTPUT	SQn	Output	1	1	1	1
Vcc	Vcc	-	1	1	2	3
GND	GND	-	1	1	4	7
Total pin count			16	24	36	48

PIN CONFIGURATION (TOP VIEW)









FUNCTIONAL DESCRIPTION

As R8A66165～R8A66168 uses silicon gate CMOS process. It realizes high-speed and high-output currents sufficient for LED drive while maintaining low power consumption and allowance for high noises.
Each bit of a shift register consists of two flip-flop having independent clocks for shifting and latching.
As for clock input, shift clock input CKS and latch clock input CKL are independent from each other, shift and latch operations being made when “L” changes to “H”.
Serial data input A is the data input of the first-step shift register and the signal of A shifts shifting registers one by one when a pulse is impressed to CKS. When A is “H”, the signal of “L” shifts.
When the pulse is impressed to CKL, the contents of the shifting register at that time are stored in a latching register, and they appear in the parallel data outputs from $\overline{Q1}$ ~ $\overline{Qn}$.
Outputs $\overline{Q1}$ ~ $\overline{Qn}$ are 24V high voltage open drain outputs.
To extend the number of bits, use the serial data output SQn which shows the output of the shifting register of the last n bit.
When reset input $\overline{R}$ is changed to “L”, $\overline{Q1}$ ~ $\overline{Qn}$ and SQn are reset. In this case, shifting and latching register are set.
If “H” is impressed to output enable input $\overline{OE}$, $\overline{Q1}$ ~ $\overline{Qn}$ reaches the high impedance state, but SQn does not reach the high impedance state. Furthermore, change in $\overline{OE}$ does not affect shift operation.

FUNCTION TABLE (Note 1)

Operation mode		Input					Parallel data output									Serial data output SQn	Remarks
		$\overline{R}$	CKS	CKL	A	$\overline{OE}$	$\overline{Q_1}$	$\overline{Q_2}$	$\overline{Q_3}$	$\overline{Q_4}$	------	$\overline{Q_{n-3}}$	$\overline{Q_{n-2}}$	$\overline{Q_{n-1}}$	$\overline{Q_n}$		
Reset		L	X	X	X	X	Z	Z	Z	Z	------	Z	Z	Z	Z	L	—
Shift Latch operation	Shift t_1	H	↑	X	H	L	$\overline{Q_1}^0$	$\overline{Q_2}^0$	$\overline{Q_3}^0$	$\overline{Q_4}^0$	------	$\overline{Q_{n-3}}^0$	$\overline{Q_{n-2}}^0$	$\overline{Q_{n-1}}^0$	$\overline{Q_n}^0$	q_{n-1}^0	Output Lighting “H”
	Latch t_2	H	X	↑	X	L	L	q_1^0	q_2^0	q_3^0	------	q_{n-4}^0	q_{n-3}^0	q_{n-2}^0	q_{n-1}^0	q_{n-1}^0	
	Shift t_1	H	↑	X	L	L	$\overline{Q_1}^0$	$\overline{Q_2}^0$	$\overline{Q_3}^0$	$\overline{Q_4}^0$	------	$\overline{Q_{n-3}}^0$	$\overline{Q_{n-2}}^0$	$\overline{Q_{n-1}}^0$	$\overline{Q_n}^0$	q_{n-1}^0	Output Lights-out “L”
	Latch t_2	H	X	↑	X	L	Z	q_1^0	q_2^0	q_3^0	------	q_{n-4}^0	q_{n-3}^0	q_{n-2}^0	q_{n-1}^0	q_{n-1}^0	
Output disable		X	X	X	X	H	Z	Z	Z	Z	------	Z	Z	Z	Z	q_n	—

Note1: ↑ : Change from low-level to high-level
$\overline{Q}^0$: Output state $\overline{Q}$ before CKL changed
X : Irrelevant
q^0 : Contents of shift register before CKS changed
q : Contents of shift register
t_1, t_2 : t_2 is set after t_1 is set
Z : High impedance

ABSOLUTE MAXIMUM RATINGS (Ta=-40~+85℃, unless otherwise noted)

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Supply voltage			−0.5～+7.0	V
V_I	Input voltage			−0.5～V_{CC}+0.5	V
V_O	Output voltage	$\overline{Q1}$～$\overline{Qn}$		−0.5～ +27	V
		SQn		−0.5～V_{CC}+0.5	V
I_O	Output current per Output pin	$\overline{Q1}$～$\overline{Qn}$		50	mA
		SQn		±25	
I_{CC}	Supply / GND current	R8A66165SP	V_{CC}、GND	−20、+220	mA
		R8A66166SP		−20、+410	
		R8A66167SP		−20、+600	
		R8A66168SP		−20、+790	
P_d	Power dissipation	R8A66165SP		500	mW
		R8A66166SP		500	
		R8A66167SP		650	
		R8A66168SP		650	
T_{stg}	Storage temperature range			−65～150	℃

RECOMMENDED OPERATING CONDITIONS (Ta=-40~+85℃, unless otherwise noted)

Symbol	Parameter			Limits			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage	5.0V support		4.5	5.0	5.5	V
		3.3V support		3.0	3.3	3.6	V
V_I	Input voltage			0		V_{CC}	V
V_O	Output voltage	SQn		0		V_{CC}	V
		$\overline{Q1}$～$\overline{Qn}$	I_{OZH}≦10uA	0		24	V
T_{opr}	Operating temperature range			−40		85	℃

ELECTRICAL CHARACTERISTICS (Ta=-40~+85℃,V_{CC}=3.0~5.5V, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
V_{T+}	Positive-going threshold voltage	V_O=0.1V, V_{CC}-0.1V		0.48xV_{CC}		0.70xV_{CC}	V
V_{T-}	Negative-going threshold voltage	V_O=0.1V, V_{CC}-0.1V		0.20xV_{CC}		0.46xV_{CC}	V
V_{OL}	Low-level output voltage $\overline{Q1}$～$\overline{Qn}$	V_I=V_{T+},V_{T-}	I_{OL}=24mA (Note 3)			0.55	V
V_{OH}	High-level output voltage SQn	V_I=V_{T+},V_{T-}	I_{OH}=-4mA	V_{CC}-0.40			V
V_{OL}	Low-level output voltage SQn	V_I=V_{T+},V_{T-}	I_{OL}=4mA			0.40	V
I_{IH}	High-level input current	V_I=V_{CC}				5	uA
I_{IL}	Low-level input current	V_I=GND				-5	uA
I_{OZ}	Off-state output leak current $\overline{Q1}$～$\overline{Qn}$	V_I=V_{T+},V_{T-}	V_O=0~24V			±10	uA
I_{CC}	Quiescent supply current	V_I=V_{CC},GND				1	mA

Note2 : ELECTRICAL CHARACTERISTICS (except I_{CC}) above is the specification per a pin.

Note3 : Each pin of $\overline{Q1}$～$\overline{Qn}$ guarantees I_{OL}=24mA.
Simultaneous lighting of all n-bits is available both for dynamic and static lighting.

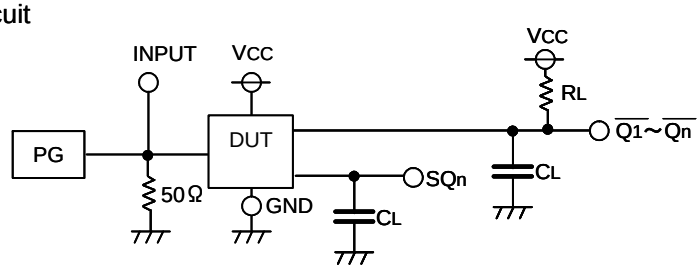
SWITCHING CHARACTERISTICS (Ta=-40~+85°C, V_{CC}=5.0V or 3.3V)

Symbol	Parameter		Test conditions	5.0V specification			3.3V specification			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
f_{max}	Maximum clock frequency					4			3.3	MHz
t_{PLH}	Output "L-H" and "H-L" propagation time	CKS-SQn				125			150	ns
t_{PHL}						125			150	ns
t_{PHL}	Output "H-L" propagation time	$\overline{R}$-SQn	C_L=50pF			125			150	ns
t_{PLZ}	Output "L-Z" propagation time	$\overline{R}$-$\overline{Q1}$~$\overline{Qn}$ (turned off)	R_L=1KΩ			200			220	ns
t_{PZL}	Output "Z-L" propagation time	CKL-$\overline{Q1}$~$\overline{Qn}$ (turned on)	(Note 4)			125			150	ns
t_{PLZ}	Output "L-Z" propagation time	CKL-$\overline{Q1}$~$\overline{Qn}$ (turned off)				200			220	ns
t_{PZL}	Output "Z-L" propagation time	$\overline{OE}$-$\overline{Q1}$~$\overline{Qn}$ (turned on)				125			150	ns
t_{PLZ}	Output "L-Z" propagation time	$\overline{OE}$-$\overline{Q1}$~$\overline{Qn}$ (turned off)				200			220	ns
C_I	Input capacitance					10			10	pF

TIMING REQUIREMENTS (Ta=-40~+85°C, V_{CC}=5.0V or 3.3V)

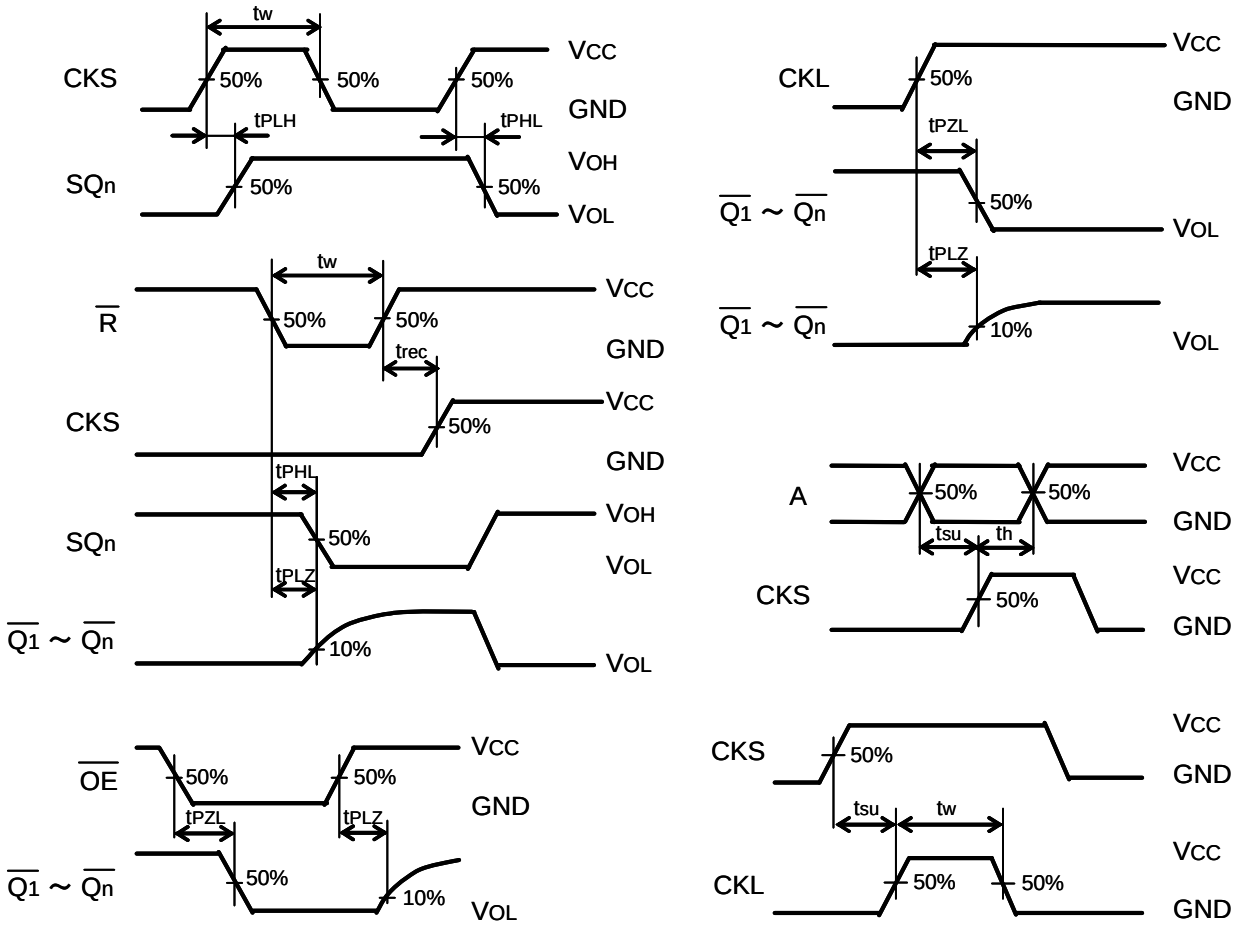
Symbol	Parameter	Test conditions	5.0V specification			3.3V specification			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_w	CKS,CKL,$\overline{R}$ pulse width	(Note 4)	125			150			ns
t_{su}	A setup time with respect to CKS		125			150			ns
t_{su}	CKS setup time with respect to CKL		125			150			ns
t_h	A hold time with respect to CKS		15			20			ns
t_{rec}	$\overline{R}$ recovery time with respect to CKS, CKL		70			80			ns

Note 4 : Test Circuit



(1) The pulse generator (PG) has the following characteristics (10%~90%). :tr = 6ns, tf = 6ns.
(2) The capacitance C_L includes stray wiring capacitance and the probe input capacitance.

TIMING DIAGRAM

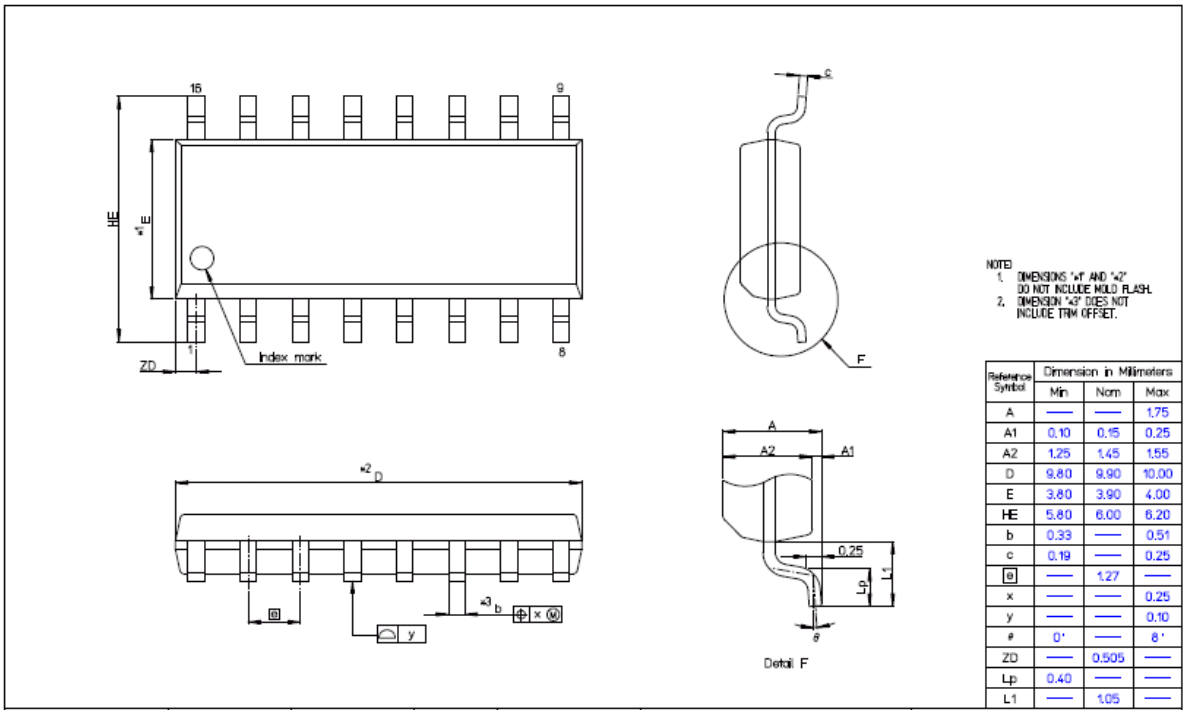


PACKAGE OUTLINE

Product part number	Package	RENESAS Code	Previous Code
R8A66165SP	16pin SOP	PRSP0016DJ-A	16P2X-E
R8A66166SP	24pin SOP	PRSP0024DF-A	24P2X-B
R8A66167SP	36pin SSOP	PRSP0036GC-A	36P2X-B
R8A66168SP	48pin SSOP	PRSP0048ZB-A	48P2X-A

R8A66165SP

PRSP0016DJ-A

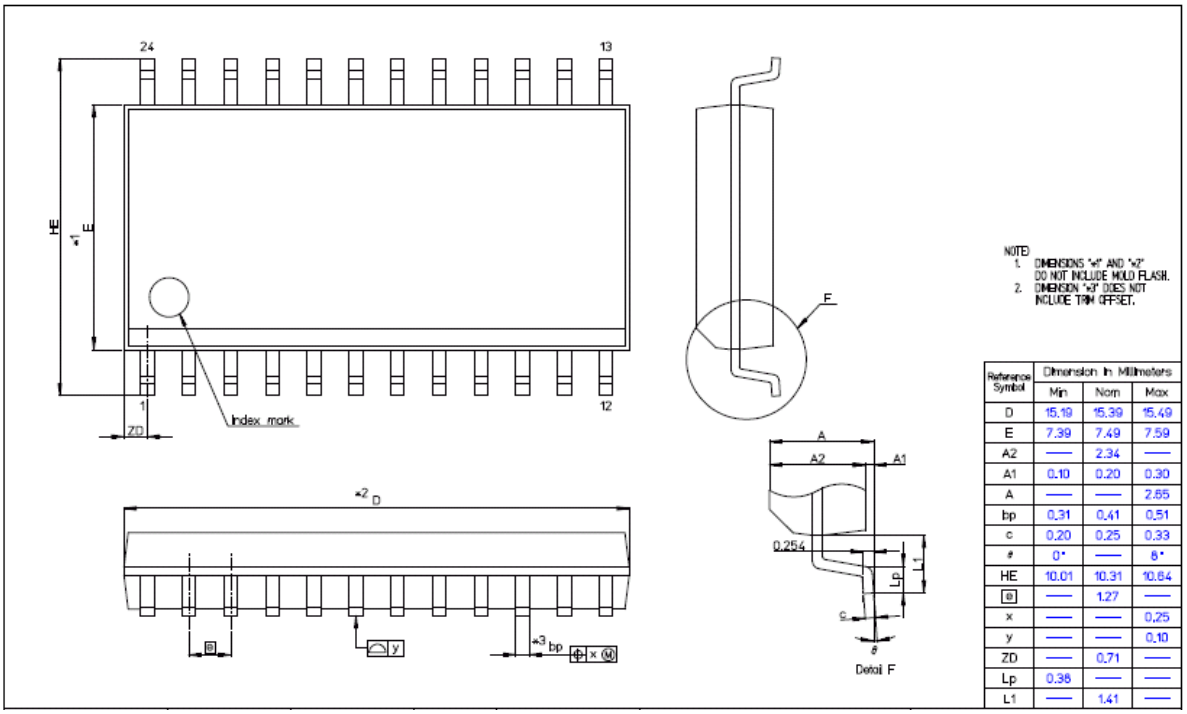


NOTE
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.55
D	9.80	9.90	10.00
E	3.80	3.90	4.00
HE	5.80	6.00	6.20
b	0.33	—	0.51
c	0.19	—	0.25
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
θ	0°	—	8°
ZD	—	0.505	—
Lp	0.40	—	—
L1	—	1.05	—

R8A66166SP

PRSP0024DF-A

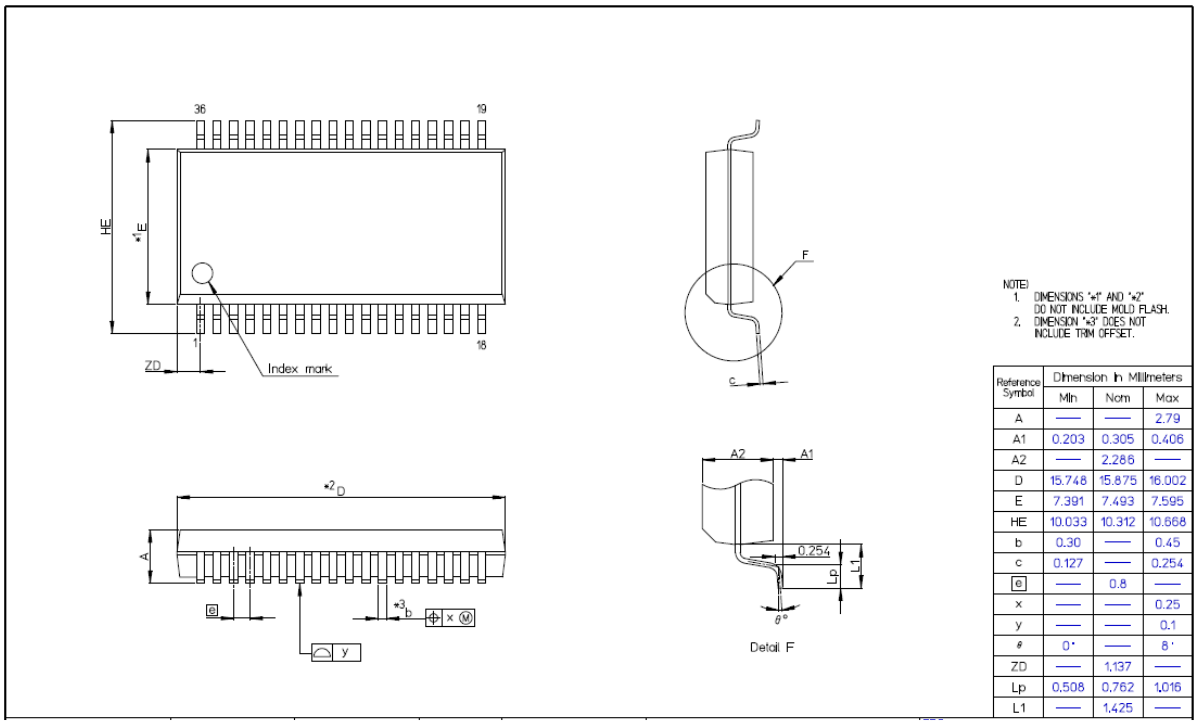


NOTE
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.19	15.39	15.49
E	7.39	7.49	7.59
A2	—	2.34	—
A1	0.10	0.20	0.30
A	—	—	2.65
bp	0.31	0.41	0.51
c	0.20	0.25	0.33
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	1.27	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.71	—
Lp	0.38	—	—
L1	—	1.41	—

R8A66167SP

PRSP0036GC-A

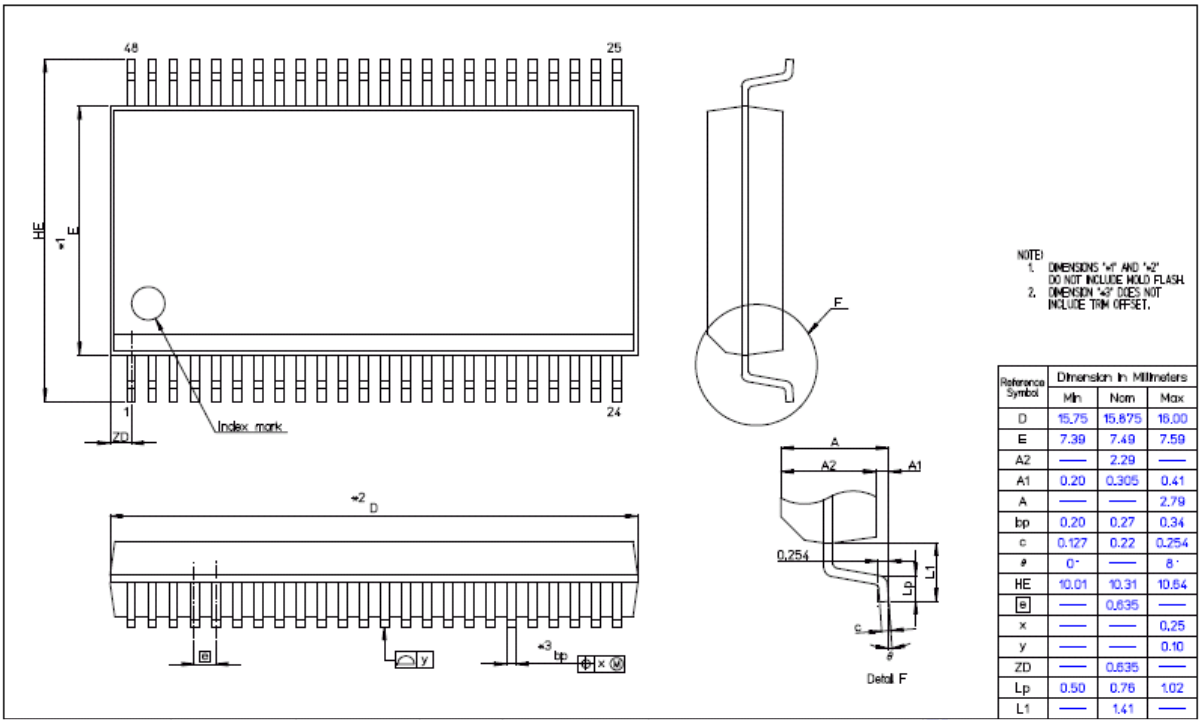


NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.79
A1	0.203	0.305	0.406
A2	—	2.286	—
D	15.748	15.875	16.002
E	7.391	7.493	7.595
HE	10.033	10.312	10.668
b	0.30	—	0.45
c	0.127	—	0.254
e	—	0.8	—
x	—	—	0.25
y	—	—	0.1
θ	0°	—	8°
ZD	—	1.137	—
Lp	0.508	0.762	1.016
L1	—	1.425	—

R8A66168SP

PRSP0048ZB-A



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	15.75	15.875	16.00
E	7.39	7.49	7.59
A2	—	2.29	—
A1	0.20	0.305	0.41
A	—	—	2.79
bp	0.20	0.27	0.34
c	0.127	0.22	0.254
θ	0°	—	8°
HE	10.01	10.31	10.64
e	—	0.635	—
x	—	—	0.25
y	—	—	0.10
ZD	—	0.635	—
Lp	0.50	0.76	1.02
L1	—	1.41	—

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