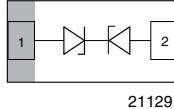


## Ultra Low Capacitance Bidirectional Symmetrical (BiSy) Single Line ESD Protection Diode in DFN1006-2B



21129



### MARKING (example only)



23190

Bar = cathode marking

X = date code

YY = type code (see table below)

### LINKS TO ADDITIONAL RESOURCES


**SPICE**  
Models

### FEATURES

- Ultra compact DFN1006-2B package
- Low package height < 0.5 mm
- 1-line ESD protection
- AEC-Q101 qualified available
- Working range  $\pm 5.5$  V
- Low leakage current < 0.01  $\mu$ A
- Ultra low load capacitance  $C_D = 0.36$  pF typ.
- ESD immunity acc. IEC 61000-4-2  
 $\pm 16$  kV contact discharge  
 $\pm 16$  kV air discharge
- e3 - Sn  
 Tin plated exposed side wall of lead frame
  - Soldering can be checked by standard vision inspection
  - AOI = Automated Optical Inspection
  - No X-ray necessary
- Lead material: Cu
- PATENT(S): [www.vishay.com/patents](http://www.vishay.com/patents)
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**  
**GREEN**  
(IS-2008)

### ORDERING INFORMATION

| PART NUMBER<br>(EXAMPLE) | ENVIRONMENTAL AND QUALITY CODE |   |       | PACKAGING CODE | ORDERING CODE<br>(EXAMPLE) |  |  |
|--------------------------|--------------------------------|---|-------|----------------|----------------------------|--|--|
|                          | AEC-Q101<br>QUALIFIED          | RoHS-COMPLIANT<br>+ LEAD (Pb)-FREE TERMINATIONS |       |                |                            |  |  |
|                          |                                | TIN<br>PLATED                                   | GREEN |                |                            |  |  |
| VBUS05N1-DD1             | -                              | G   | 3     | -08            | VBUS05N1-DD1-G3-08         |  |  |
| VBUS05N1-DD1             | H                              | G   | 3     | -08            | VBUS05N1-DD1HG3-08         |  |  |

### PACKAGE DATA

| DEVICE NAME  | PACKAGE NAME | TYPE CODE | WEIGHT  | SOLDERING CONDITIONS         |
|--------------|--------------|-----------|---------|------------------------------|
| VBUS05N1-DD1 | DFN1006-2B   | 5B        | 0.83 mg | Peak temperature max. 260 °C |

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER             | TEST CONDITIONS  | SYMBOL           | VALUE       | UNIT |
|-----------------------|--|------------------|-------------|------|
| Peak pulse current    | Acc. IEC 61000-4-5, 8/20 $\mu$ s/single shot                                     | I <sub>PPM</sub> | 4           | A    |
| Peak pulse power      | Pin 1 to pin 2<br>Acc. IEC 61000-4-5; t <sub>p</sub> = 8/20 $\mu$ s; single shot | P <sub>PP</sub>  | 90          | W    |
| ESD immunity          | Contact discharge acc. IEC 61000-4-2; 10 pulses                                  | V <sub>ESD</sub> | $\pm 16$    | kV   |
|                       | Air discharge acc. IEC 61000-4-2; 10 pulses                                      |                  | $\pm 16$    |      |
| Operating temperature | Junction temperature   | T <sub>J</sub>   | -55 to +150 | °C   |
| Storage temperature   |  | T <sub>stg</sub> | -55 to +150 | °C   |

**PATENT(S):** [www.vishay.com/patents](http://www.vishay.com/patents)

This Vishay product is protected by one or more United States and international patents.

**ESD PROTECTION FOR HIGH-SPEED SIGNAL OR DATA LINES**

The VBUS05N1-DD1 is a Bidirectional and Symmetrical (BiSy) ESD protection device which clamps positive and negative overvoltage transients to ground. Connected between the signal or data line and the ground the VBUS05N1-DD1 offers a high isolation (low leakage current, low capacitance) within the specified working range. Due to the short leads and small package size of the tiny DFN1006 package the line inductance is very low, so that fast transients like an ESD strike can be clamped with minimal over- or undershoots. Due to the very low capacitance the VBUS05N1-DD1 can be used for high speed data ports like HDMI, USB 3.0 or Thunderbolt.

| <b>ELECTRICAL CHARACTERISTICS</b> ( $T_{amb} = 25^{\circ}C$ , unless otherwise specified) |   |               |      |      |      |          |
|---|---|---------------|------|------|------|----------|
| PARAMETER   | TEST CONDITIONS/REMARKS   | SYMBOL        | MIN. | TYP. | MAX. | UNIT     |
| Protection paths  | Number of lines which can be protected                            | $N_{channel}$ | -    | -    | 1    | lines    |
| Reverse stand-off voltage   | Max. reverse working voltage                                      | $V_{RWM}$     | -    | -    | 5.5  | V        |
| Reverse voltage   | at $I_R = 0.1 \mu A$  | $V_R$         | 5.5  | -    | -    | V        |
| Reverse current   | at $V_{RWM} = 5.5 V$  | $I_R$         | -    | -    | 0.1  | $\mu A$  |
| Reverse breakdown voltage   | at $I_R = 1 mA$   | $V_{BR}$      | 7    | 8.5  | 10   | V        |
| Reverse clamping voltage  | at $I_{PP} = 1 A$   | $V_C$         | -    | 11.5 | 13   | V        |
|   | at $I_{PP} = I_{PPM} = 4 A$                                       | $V_C$         | -    | 18   | 21   | V        |
| Capacitance   | at $V_R = 0 V$ ; $f = 1 MHz$                                      | $C_D$         | -    | 0.36 | 0.4  | pF       |
|   | at $V_R = 3.3 V$ ; $f = 1 MHz$                                    | $C_D$         | -    | 0.36 | -    | pF       |
| Clamping voltage  | Transmission Line Pulse (TLP); $t_p = 100 ns$<br>$I_{TLP} = 8 A$  | $V_{C-TLP}$   | -    | 22   | -    | V        |
|   | Transmission Line Pulse (TLP); $t_p = 100 ns$<br>$I_{TLP} = 16 A$ |               | -    | 33   | -    |          |
| Dynamic resistance  | Transmission Line Pulse (TLP); $t_p = 100 ns$                     | $R_{DYN}$     | -    | 1.4  | -    | $\Omega$ |

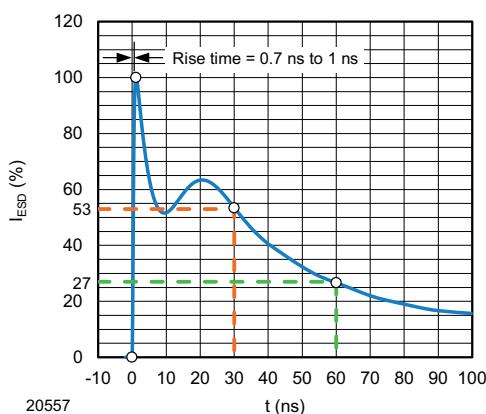
**TYPICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}C$ , unless otherwise specified)


Fig. 1 - ESD Discharge Current Wave Form  
acc. IEC 61000-4-2 (330  $\Omega$ /150 pF)

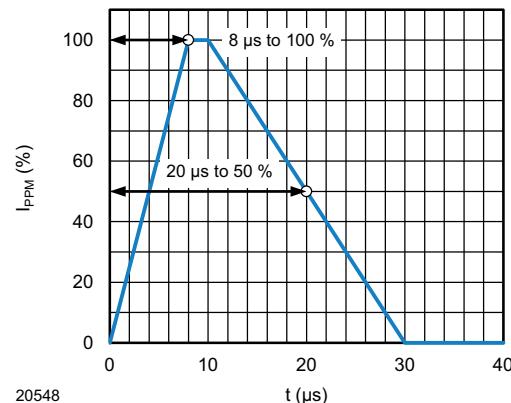


Fig. 2 - 8/20  $\mu$ s Peak Pulse Current Wave Form  
acc. IEC 61000-4-5

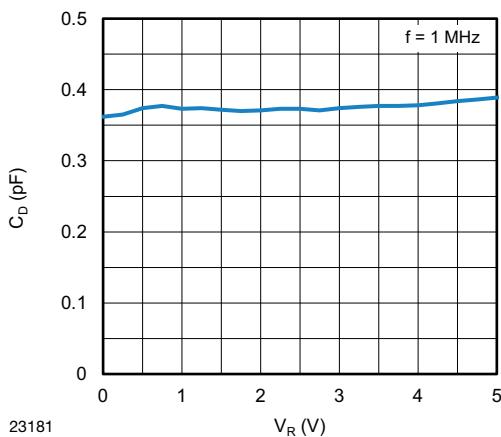


Fig. 3 - Typical Capacitance vs. Reverse Voltage

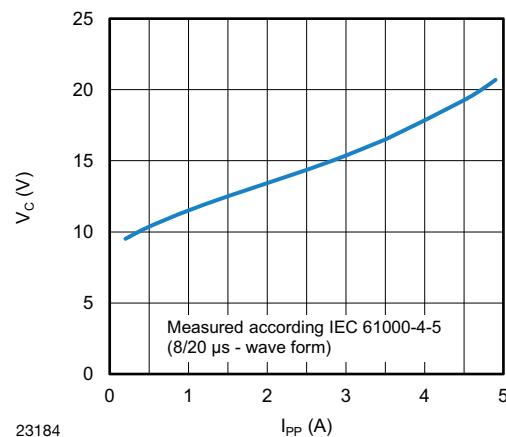


Fig. 6 - Typical Peak Clamping Voltage vs. Peak Pulse Current

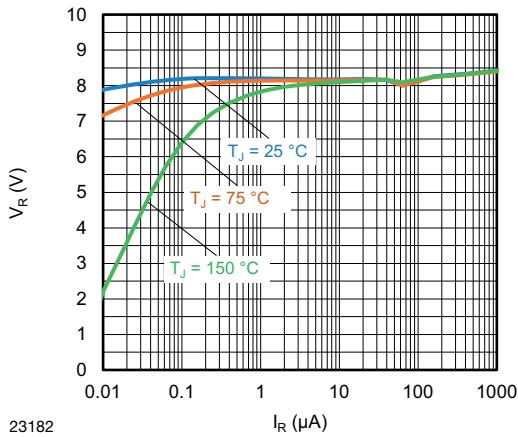


Fig. 4 - Typical Reverse Voltage vs. Reverse Current

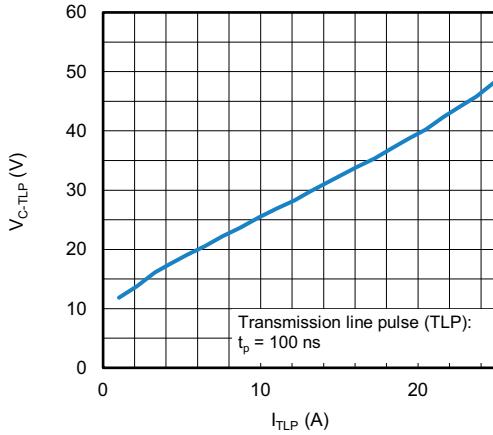
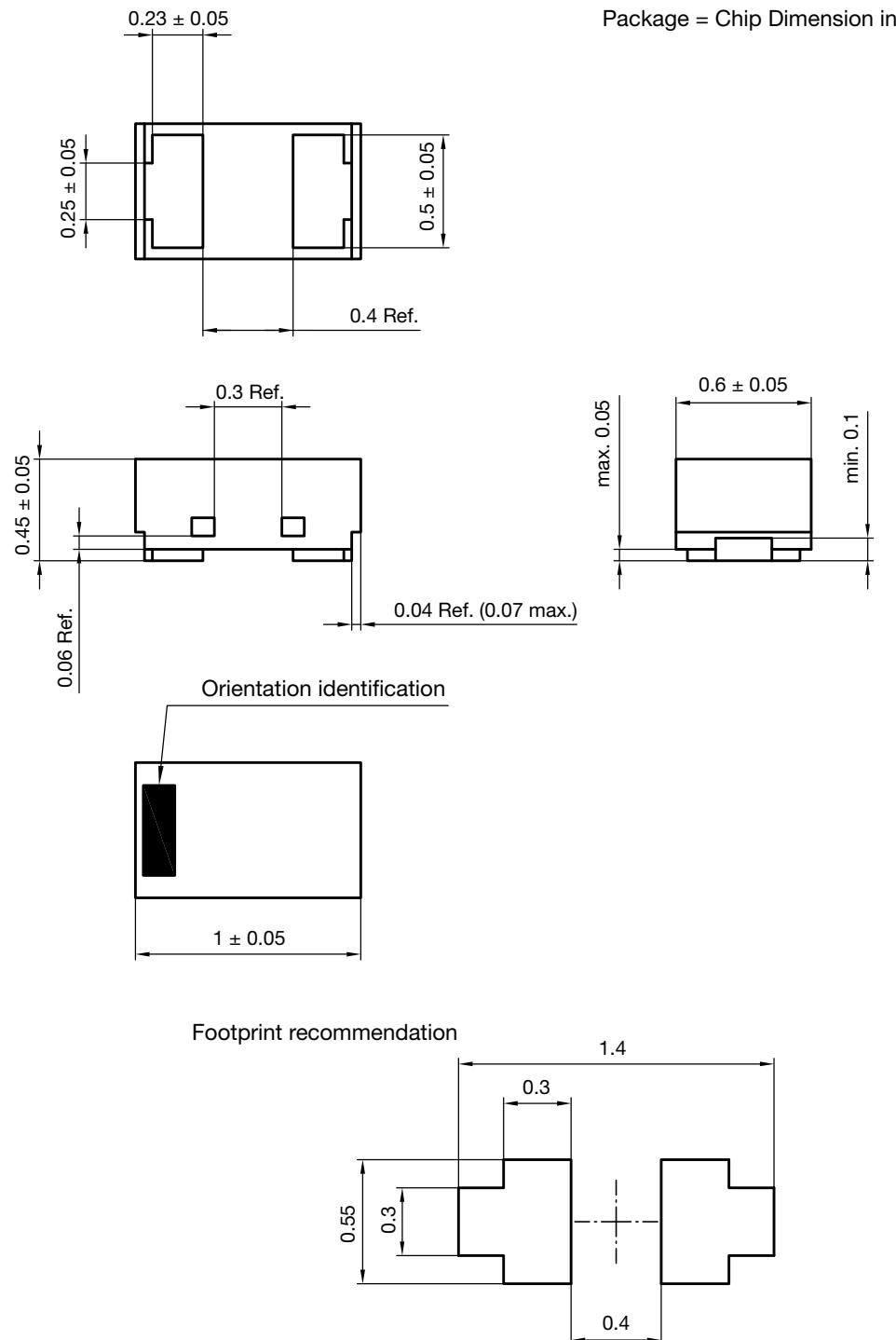


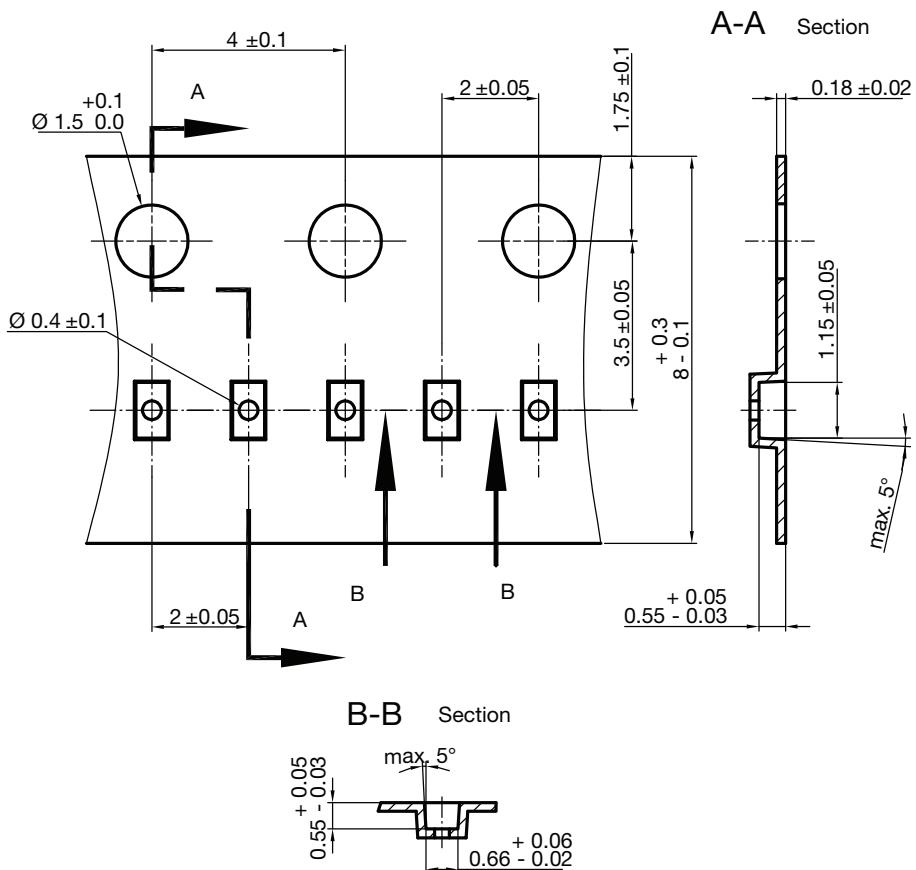
Fig. 5 - Typical Clamping Voltage vs. Peak Pulse Current

**PACKAGE DIMENSIONS** in millimeters (inches): **DFN1006-2B**


Document no.: S8-V-3906.04-059 (4)  
Created - Date: 11-Jul-2018  
Rev.5 - Date: 17-Sep-2021

23191

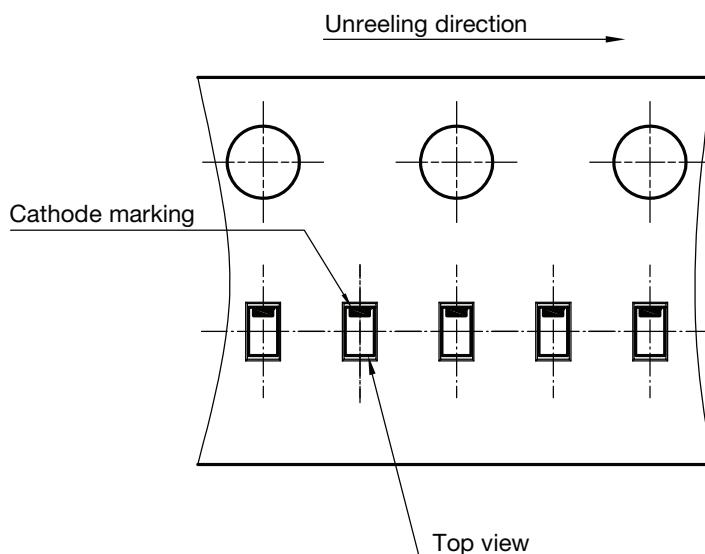
## **CARRIER TAPE DFN1006-2B**



S8-V-3906.04-063 (4)  
created 28.10.2019

surface resistance:  $10^5$  -  $10^{11} \frac{\text{OHMS}}{\text{SQ}}$   
 Cumulative tolerances of 10 sprocket holes is  $\pm 0.2$  mm

## ORIENTATION IN CARRIER TAPE DFN1006-2B



S8-V-3906.04-064 (4)  
created 28.10.2019

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