Battery Pack Front-End Charge/Discharge High-Side NFET Driver

GENERAL DESCRIPTION

The SiLM2660/SiLM2661 is a low-power, high-side N-channel FET driver for battery charge/discharge system control. A high-side control avoids ground disconnection in the system and allows continuous communication between the battery pack and host system. The SiLM2660 has additional P-channel FET control to allow low-current pre-charge to a deeply discharged battery, and it also integrates a PACK+ voltage monitor for the host to sense the PACK+ voltage.

The independent enable inputs allow charge and discharge FETs to be turned on and off separately, offering the great design flexibility for battery systems.

The SiLM2660 is available in TSSOP-16 and SiLM2661 is available in SOP8 package.

APPLICATIONS

- E-bikes, E-Scooter and E-Motors
- Energy storage systems
- Wireless base station battery systems
- 12V to 48V battery packs

FEATURES

- High side NFET driver with fast turn-on and turn-off times for battery protection
- Pre-charge PFET driver provides a current-limited pre-charge function for depleted cell-pack (only for SiLM2660)
- Independent enable control for charging and discharging
- Scalable external capacitor-based charge pump to accommodate a different range of FETs in parallel
- High voltage tolerant (100 V absolute maximum)
- Internal switch to enable pack-voltage sensing (only for SiLM2660)
- Common and separate charge and discharge path configuration support
- Low current consumption
  - Normal mode: 40 μA
  - Shutdown: less than 10 μA

TYPICAL APPLICATION CIRCUIT

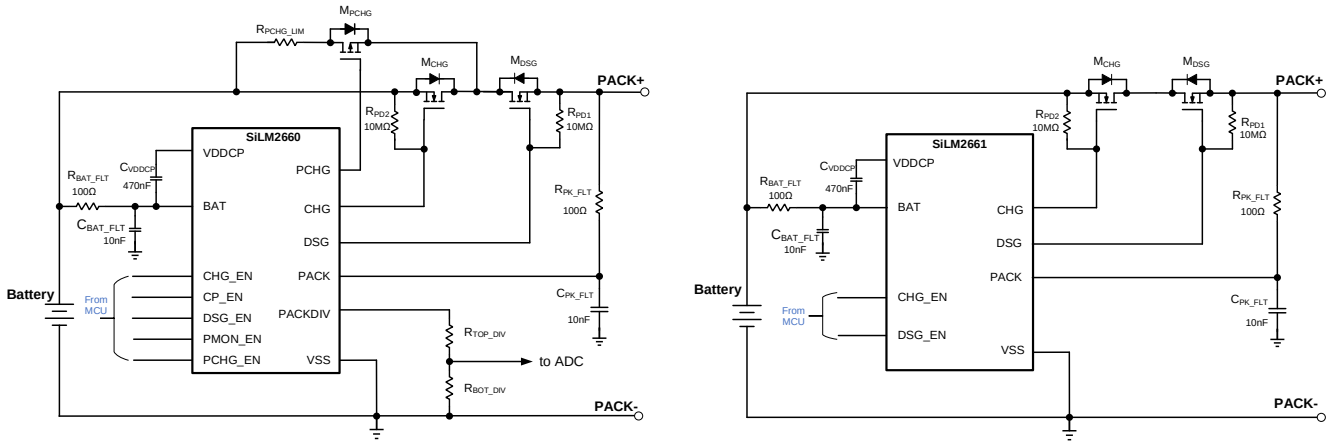
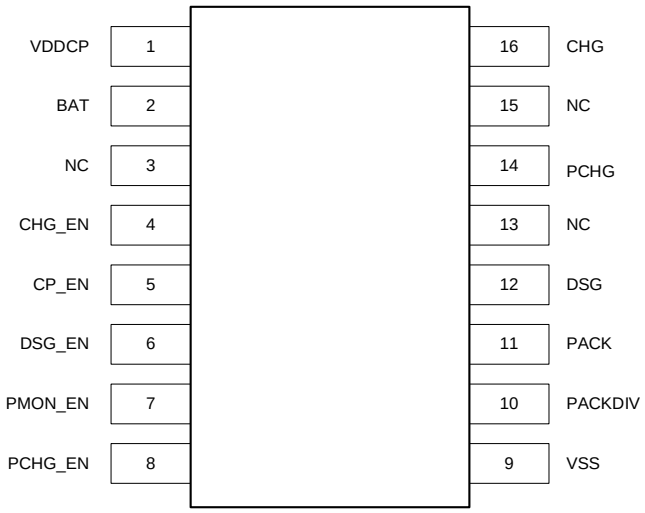
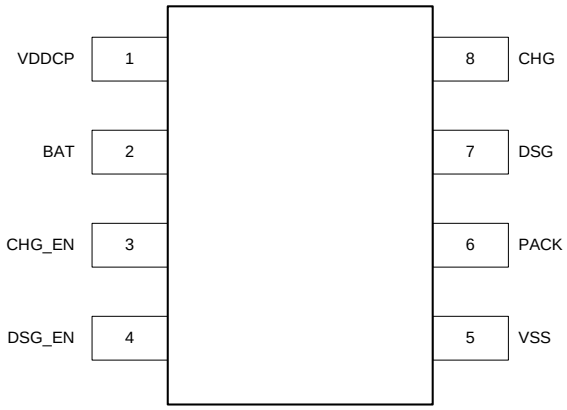


Figure 1. Typical Application Circuit

TABLE OF CONTENTS

PIN CONFIGURATION

Package	Pin Configuration (Top View)
TSSOP16	
SOP8	

PIN DESCRIPTION

No.		Pin	Description
TSSOP16	SOP8		
1	1	VDDCP	Charge pump output. Connect a capacitor to BAT pin. Do not add any load on this pin.
2	2	BAT	Top of battery stack.
4	3	CHG_EN	Charge FET enable.
5		CP_EN	Charge pump enable (internally logic OR'ed with CHG_EN and DSG_EN signals).
6	4	DSG_EN	Discharge FET enable.

No.		Pin	Description
TSSOP16	SOP8		
7		PMON_EN	Pack monitor enable. When the pack monitor is enabled, the internal switch between PACK and PACKDIV is closed, otherwise, the internal switch is turn off.
8		PCHG_EN	Pre-charge FET enable.
9	5	VSS	Ground reference.
10		PACKDIV	PACK voltage after internal switch. Connect to MCU ADC via resistor divider.
11	6	PACK	Analog input from PACK+ terminal.
12	7	DSG	Gate drive for discharge FET.
14		PCHG	Gate drive for pre-charge FET.
16	8	CHG	Gate drive for charge FET.
3,13,15		NC	No connect. Leave the pin floating.

ORDERING INFORMATION

Order Part No.	Package	QTY
SiLM2660CD-DG	TSSOP16	3000/Reel
SiLM2661CA-DG	SOP8	2500/Reel

FUNCTIONAL BLOCK DIAGRAM

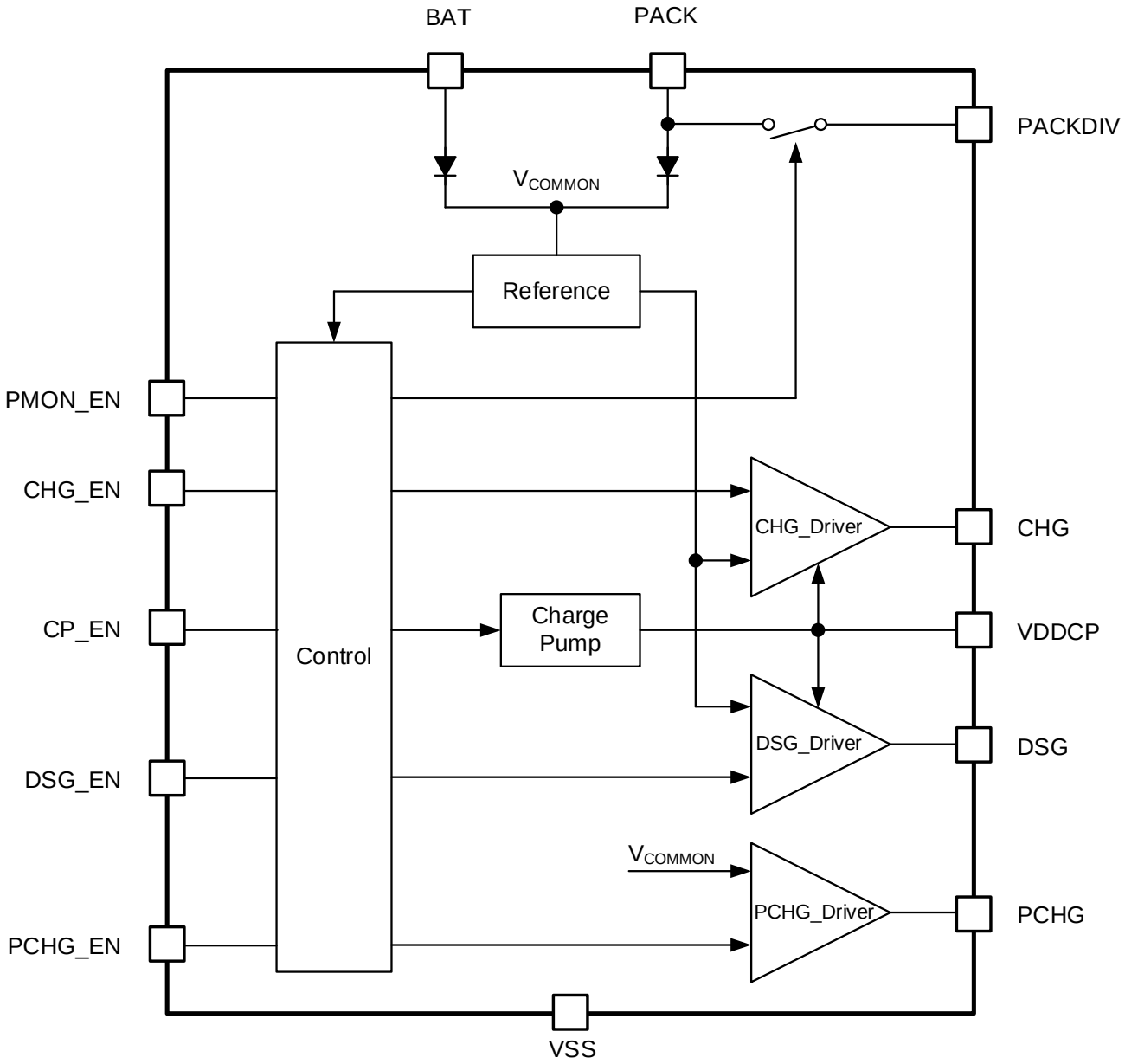


Figure 2. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Min	Max	Unit
BAT, PACK (both under charge pump disabled condition)	-0.3	100	V
CHG_EN, CP_EN, DSG_EN, PMON_EN, PCHG_EN	-0.3	15	
CHG, DSG, PCHG, PACKDIV, VDDCP	- 0.3	105	
Junction temperature, T_J	-40	150	°C
Storage temperature, T_S	-55	150	
Functional Temperature, T_{FUNC}	-40	110	

ESD RATINGS

Parameters	Value	Unit
Human-body model (HBM)	±1000	V
Charged-device model (CDM)	±2000	

RECOMMENDED OPERATION CONDITIONS

V_{BAT} = 48V, T_A = 25°C for typical values and V_{BAT} = 8V to 90V, T_A = -40°C to 85°C for minimum and maximum values, unless otherwise specified.

Symbol	Definition	Min	Nom	Max	Unit
V_{BAT}	Battery cell input supply voltage range	8		90	V
V_{PACK}	Charger/Load voltage range	0		90	
V_{IN}	CHG_EN, DSG_EN, PCHG_EN, PMON_EN, CP_EN	0		14	
C_{VDDCP}	Capacitor between VDDCP and BAT		470		nF
T_{OPR}	Operating free-range temperature	-40		85	℃

ELECTRICAL CHARACTERISTICS

V_{BAT} = 48V, T_A = 25°C for typical specifications and V_{BAT}= 8V to 90V, T_A = –40°C to 85°C for minimum/maximum specifications, unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Supply and Leakage Current						
I_{BAT}	Normal mode current (1)	C_{VDDCP} = 470nF, V_{BAT} = 8V, C_L = 10nF		70		μA
		C_{VDDCP} = 470nF, V_{BAT} ≥ 48V C_L = 10nF		40		μA
I_{SHUT}	Sum of current into BAT and PACK pin	Shutdown mode, V_{PACK} = 0V, V_{BAT} = 8V		6	10	μA
Charge Pump						
V_{VDDCP}	Charge pump voltage	No Load, CP_EN = high, V_{VDDCP} –V_{BAT}	9		14	V
t_{CPON}	Charge pump start up time from zero voltage	C_{VDDCP} = 470nF, 10% to 90% of V_{VDDCP}		50		ms
Enable Control Signals (CHG_EN, DSG_EN, PCHG_EN, CP_EN, PMON_EN)						
V_{IL}	Digital low input level				0.6	V
V_{IH}	Digital high input level		1.2			V
R_{PD}	Internal pull down	V_{IN} = 5 V	0.4	1	4	MΩ
Charger FET Driver						
$V_{CHG\_FET\_ON}$	CHG gate drive high voltage	C_L = 10nF, CHG_EN = High, V_{BAT} = V_{PACK}, V_{CHG} – V_{BAT}	9	12	14	V
$R_{CHG\_FET\_ON}$	CHG FET driver on resistance	V_{VDDCP} – V_{BAT} = 12 V, CHG_EN = High, V_{BAT} = V_{PACK}		0.5		kΩ
$R_{CHG\_FET\_OFF}$	CHG FET driver off resistance	V_{VDDCP} – V_{BAT} = 12 V, CHG_EN = Low, V_{BAT} = V_{PACK}		0.15		kΩ
Discharger FET Driver						
$V_{DSG\_FET\_ON}$	DSG gate drive high voltage	C_L = 10nF, DSG_EN = High, V_{BAT} = V_{PACK}, V_{DSG} – V_{PACK}	9	12	14	V
$R_{DSG\_FET\_ON}$	DSG FET driver on resistance	V_{VDDCP} – V_{BAT} = 12 V, DSG_EN = High, V_{BAT} = V_{PACK}		1.5		kΩ
$R_{DSG\_FET\_OFF}$	DSG FET driver off resistance	V_{VDDCP} – V_{BAT} = 12 V, DSG_EN = Low, V_{BAT} = V_{PACK}		0.5		kΩ
Pre-charge FET Driver						
$V_{PCH\_GFET\_ON}$	PCHG gate drive high voltage	V_{PACK} > 17 V, V_{BAT} < V_{PACK}, V_{PACK} – V_{PCHG}	9	12	14	V
PACK Monitor (PACK_DIV)						
R_{PMON_FET}	On resistance of internal FET between PACK and PACKDIV	PMON_EN = High	1.5	2.5	3.5	kΩ

(1) Normal mode is defined as CHG_EN = DSG_EN = CP_EN = High, PCHG_EN = PMON_EN = Low. Current value is averaged out over time.

TIMING CHARACTERISTICS

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
$t_{CHG\_FET\_ON}$	CHG on rise time + propagation delay	C_L = 10nF, (20% of CHG_EN from Low to High) to (80% of $V_{CHG\_FET\_ON}$), CP_EN = High, CP is already on		14	23	μs
$t_{CHG\_FET\_OFF}$	CHG off fall time + propagation delay	C_L= 10nF, (80% of CHG_EN from High to Low) to (20% of $V_{CHG\_FET\_ON}$), CHG_EN = High to Low		4	10	μs
$t_{PROP\ \_CHG}$	CHG EN to CHG output	C_L= 10nF, CP_EN = High, (CP is already on), see timing diagram		2.2		μs
$t_{DSG\_FET\_ON}$	DSG on rise time + propagation delay	C_L= 10nF, (20% of DSG_EN from Low to High) to (80% of $V_{DSG\_FET\_ON}$), CP_EN = High, (CP is already on)		17	35	μs
$t_{DSGFETOFF}$	DSG off fall time + propagation delay	C_L= 10nF, (80% of DSG_EN from High to Low) to (20% of $V_{DSG\_FET\_ON}$)		8	20	μs
t_{PROP_DSG}	DSG EN to DSG output propagation delay	C_L= 10nF, CP_EN = High, (CP already on), see timing Diagram		2.2		μs
t_{PCHG_OFF}	PCHG turn off time + propagation delay	C_L= 1nF, (20% of PCHG_EN from High to Low) to 80% of $V_{PCHG\_FET\_ON}$		15	30	μs
t_{PCHG_ON}	PCHG turn on time + propagation delay	C_L= 1nF, (80% of PCHG_EN from Low to High) to (20% of $V_{PCHG\_FET\_ON}$)		18	28	μs
t_{PROP_PCHG}	PCHG EN to PCHG propagation delay	C_L= 1nF		1		μs
t_{PROP_PMON}	PMON_EN and PACKDIV = PACK propagation delay			0.1		μs

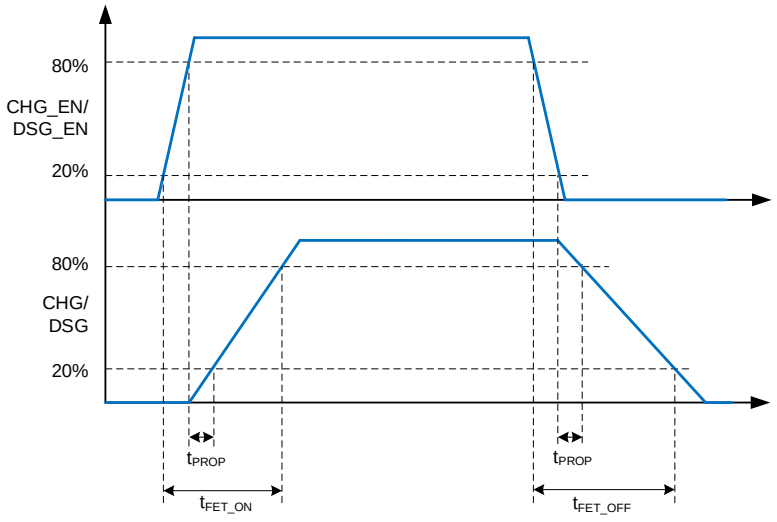


Figure 3. Timing Diagram (CP is already on)

TYPICAL PERFORMANCE CHARACTERISTICS

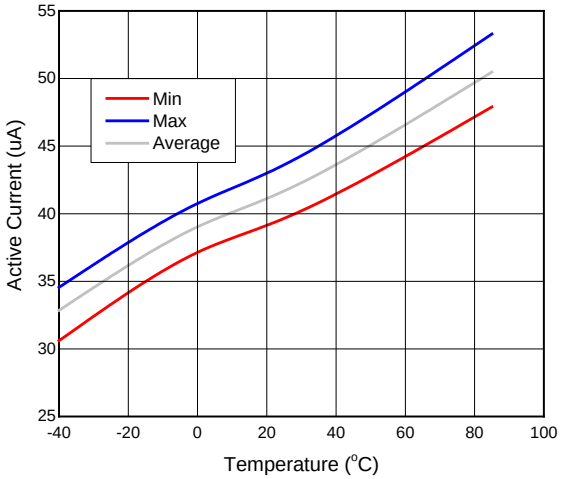


Figure 4. Normal Mode Current vs Battery

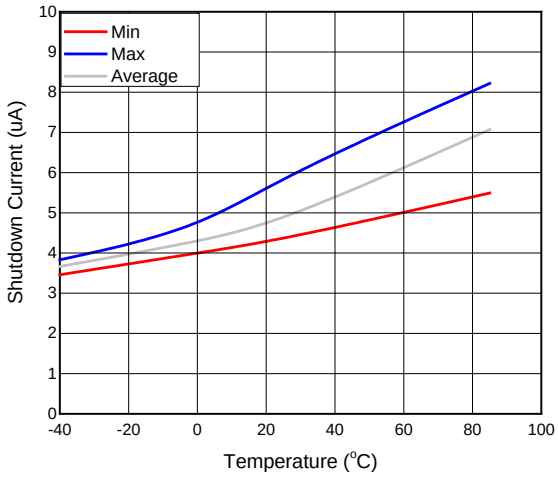


Figure 5. Shutdown Mode Current vs Battery

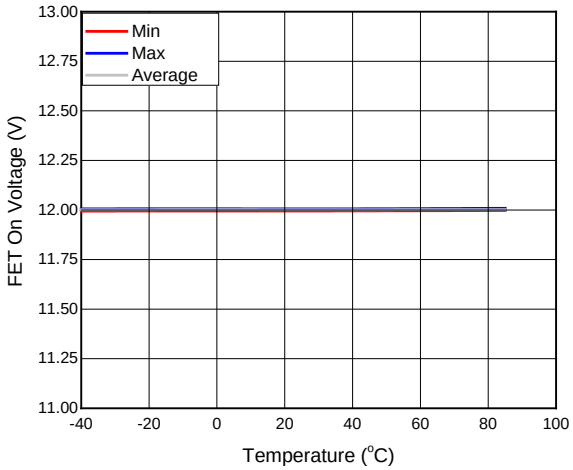


Figure 6. CHG/DSG FET On Voltage vs Temperature

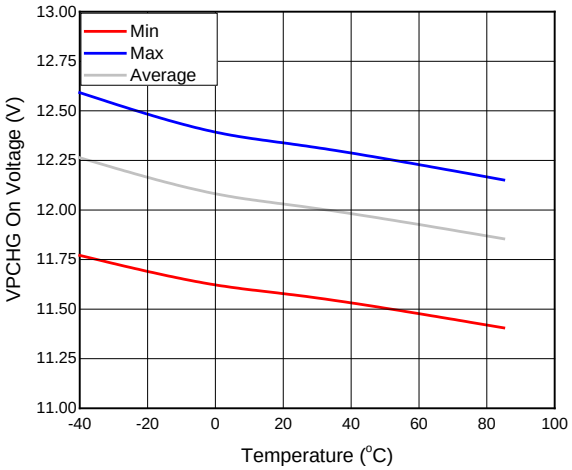


Figure 7. PCHG On Voltage vs Temperature

FUNCTION DESCRIPTION

Overview

The SiLM2660 is a low power, high-side, N-Channel MOSFET driver for battery-pack protection systems. High-side charge/discharge control offers a huge advantage versus low-side control system. With high-side implementation, a system-side processor can always communicate with the monitor or micro-controller (MCU) within the battery pack, regardless of whether the FETs are on or off. One key benefit of an ever-present communication link is the ability to read out critical pack parameters despite safety faults, thereby enabling the system to assess pack conditions before determining if normal operation may resume.

The SiLM2660 allows independent control on charging and discharge via the digital enable pins. The device has integrated charge pump which is enabled by the CP_EN pin. The enable inputs, CHG_EN, DSG_EN, and PCHG_EN control the CHG, DSG, and PCHG FET gate drivers, respectively. The enable inputs can be connected to a battery pack controller or a MCU which will determine the state of the enable inputs based on the system control.

In normal mode, the battery pack controller or the MCU enables the CHG_EN and DSG_EN, turning on the CHG and DSG FET drivers to connect the battery power to the PACK+ terminal. When a fault is detected by the battery pack controller or the MCU, it can disable the CHG_EN and/or DSG_EN to turn off the charge or discharge path for protection. Note that when either the CHG_EN or DSG_EN is enabled, the charge pump will be automatically enabled even if the CP_EN is in the disable state. It is recommended to enable the charge pump via CP_EN pin during system start-up to avoid adding the t_{CPON} time into the FET switching time during normal operation.

A lower charging current is usually applied to a deeply depleted battery pack. The PCHG_EN input provides an option to implement a P-Channel MOSFET pre-charge path (current-limited path) in the battery pack.

The SiLM2660 provides a PMON_EN pin which will connect the PACK+ voltage onto the PACKDIV pin when the PMON_EN is high. An external resistor divider can be used on the PACKDIV to scale down the PACK+ voltage and this scaled down PACK+ voltage can be connected to an ADC input for voltage measurement. The system can use this information for charger detection or to implement advanced charging control. If no Pack voltage measurement needed, the PMON_EN can be set as low to save system power consumption.

For safety purposes, all the enable inputs are internally pulled down. If the battery pack controller or MCU is turned off, or if the PCB trace is damaged, the internal pull down of the enable inputs will keep CHG, DSG, PCHG in an off state and the PACK+ voltage does not switch onto the PACKDIV pin.

Charge Pump Control

The SiLM2660 has an integrated charge pump. A minimum of 470nF capacitor is required between the VDDCP and BAT pin to ensure proper function of the charge pump. If the VDDCP capacitor is disconnected, a residual voltage could reside at the CHG and/or DSG output if CHG_EN and/or DSG_EN are enabled. Such a fault condition can put the external FETs in high Rdson state and result in FET damage.

The VDDCP capacitor can be scaled up to support more FETs in parallel (such as high-total FET-gate capacitance) than the value specified in the electrical characteristics table. A higher VDDCP capacitance results in longer t_{CPON} time. See the **Application Information** section for more information. Note that probing the VDDCP pin may increase the loading on the charge pump and result in lower measurement value than the V_{VDDCP} specification. Using higher impedance probe can reduce such effect on the measurement.

The charge pump is controlled by CP_EN and also OR'ed with the CHG_EN and DSG_EN inputs. This means by enabling CHG_EN or DSG_EN alone, the charge pump will automatically turn on even if the CP_EN pin is disabled. The PCHG_EN controls the PCHG pin, which is a P-channel FET driver and does not require the function of the charge pump. The charge pump is turned off by default. When CP_EN is high, the charge pump turns on regardless of the status of the CHG_EN and DSG_EN inputs.

When CP_EN is enabled, the charge pump voltage starts to ramp up. Once the voltage is above an internal UVLO level, about 9V typical above V_{BAT}, the charge pump is considered on. The charge pump voltage should continuously ramp to the V_{VDDCP} level. If the CHG_EN and/or DSG_EN is enabled, the CHG and/or DSG voltage will starts to turn on after the charge pump voltage is above the UVLO level, and ramp up along the charge pump voltage to the V_{VDDCP} level. Otherwise, the CHG and DSG do not turn on if the charge pump voltage fails to ramp up above UVLO. For example, if the C_{VDDCP} is not scaled properly to support the number of FETs in parallel, the heavy loading would prevent the charge pump to ramp up above UVLO and CHG and DSG would not be turned on in this case.

When CHG_EN and/or DSG_EN is enabled after the charge pump is fully turned on, the CHG_EN to CHG on delay (or DSG_EN to DSG on delay) is simply the sum of propagation delay and the FET rise time. If the CP_EN is not used (it's is connected to ground) and the charge pump is controlled by the CHG_EN or DSG_EN, the CHG_EN to CHG on delay (or DSG_EN to DSG on delay) will be the sum of the charge pump start up time, the propagation delay and the FET rise time. It is highly recommended to enable CP_EN at system start-up and keep the CP_EN enabled during normal operation.

The charge pump is turned off when CP_EN, CHG_EN and DSG_EN are all low. The charge pump is not actively driven low and the voltage on the VDDCP capacitor bleeds off passively. If any of the CP_EN, CHG_EN, or DSG_EN signals is switched high again while the VDDCP capacitor is still bleeding off its charge, the charge pump start-up time, t_{CPON}, will be shorter.

CHG and DSG Output Driver Control

The CHG_EN and DSG_EN pins provide direct control of the CHG and DSG FET driver. summarizes the CHG and DSG statute with respect to the CP_EN, CHG_EN and DSG_EN inputs.

Table 1. CHG and DSG with Respect to CP_EN, CHG_EN and DSG_EN

CP_EN	CHG_EN	DSG_EN	CHARGE PUMP	CHG	DSG
Low (Default)	Low (Default)	Low (Default)	OFF (Default)	OFF (Default)	OFF (Default)
Low	Low	High	ON	OFF	ON
Low	High	Low	ON	ON	OFF
Low	High	High	ON	ON	ON
High	Low	Low	ON	OFF	OFF
High	Low	High	ON	OFF	ON
High	High	Low	ON	ON	OFF
High	High	High	ON	ON	ON

PCHG Output Driver Control

The PCHG output driver is designed to drive a P-channel FET and is controlled by the PCHG_EN pin. The PCHG driver provides an option to implement a separate charging path with a P-channel FET to charge the battery when the cells are deeply depleted. A resistor should be added in series to the P-channel pre-charge FET to limit the charging current. A pre-charge current is usually at or less than 1/10 of the normal charge current if the charger does not support lower current pre-charge. Refer to the battery cell specification from the cell manufacturer charging for the appropriate current limit.

PCHG_EN	PCHG
Low (Default)	OFF (Default)
High	ON

Pack Monitor Enable

The SiLM2660 provides a PMON_EN pin to control the internal switch between PACK pin and PACKDIV pin. When the PMON_EN is high, the internal switch is on and the PACKDIV is connected to PACK through this internal switch. A resistor divider can be connected to the PACKDIV pin externally to divide down the PACK+ voltage into a measurable range of an ADC.

The internal switch has an on resistance of R_{PMON_FET}. The external resistor divider for PACKDIV pin should be selected to avoid exceeding the absolute maximum of the PACKDIV pin and should also keep the loading current less than 500μA. If this function is not used, the PACKDIV pin should leave floating. To reduce power consumption, the PMON_EN should be enabled only when PACK+ voltage measurement is needed.

Device Functional Mode

The SiLM2660 provides two functional modes: Normal mode and shutdown mode.

In normal mode, the SiLM2660 charge pump is turned on by enabling either CP_EN, CHG_EN, or DSG_EN. In this mode, typically the CHG and DSG outputs are driven to V_{BAT} + V_{VDDCP}.

In shutdown mode, the SiLM2660 is completely powered down. When CHG_EN, DSG_EN, and CP_EN are all driven low, the device enters shutdown mode, and the outputs are driven low.

Functional Mode	Condition
Normal Mode	CHG_EN=High, DSG_EN=High, CP_EN=High, PCHG_EN=don't care, PMON_EN=don't care
Shutdown Mode	CHG_EN=Low, DSG_EN=Low, CP_EN=Low, PCHG_EN=Low, PMON_EN=Low

APPLICATION INFORMATION

Slave Device

The SiLM2660 is a FET driver. It controls the output pins (CHG, DSG, PCHG, and PACKDIV) according to the input pin (CHG_EN, DSG_EN, PCHG_EN, CP_EN, and PMON_EN) status. The SiLM2660 does not validate if the inputs should or should not be turned on or off. For example, if both CHG_EN and PCHG_EN are enabled, SiLM2660 will turn on both CHG and PCHG simultaneously, enabling two charging paths to the system. The system designer should avoid undesirable enable combinations.

Scalable VDDCP Capacitor to Support Multiple FETs in Parallel

The SiLM2660 requires a minimum 470nF capacitor to be connected between the VDDCP and BAT pin in order to turn on the integrated charge pump. The Electrical Characteristics Specification of this document specified the device performance based on 10nF loading with 470nF VDDCP capacitor. The loading capacitance varies with FET choices, number of FETs in use, and in parallel and simultaneous switching versus sequential switching of CHG and DSG FET.

The more FETs that are in parallel, the higher the loading capacitance. Similarly, simultaneously switching of the CHG and DSG FET loads down the charge pump more than sequentially switching both FETs. Eventually, the loading capacitance can exceed the supported range of a 470nF VDDCP capacitor. A larger capacitance that higher than 470nF between VDDCP and BAT pin can be used to support higher-loading capacitance.

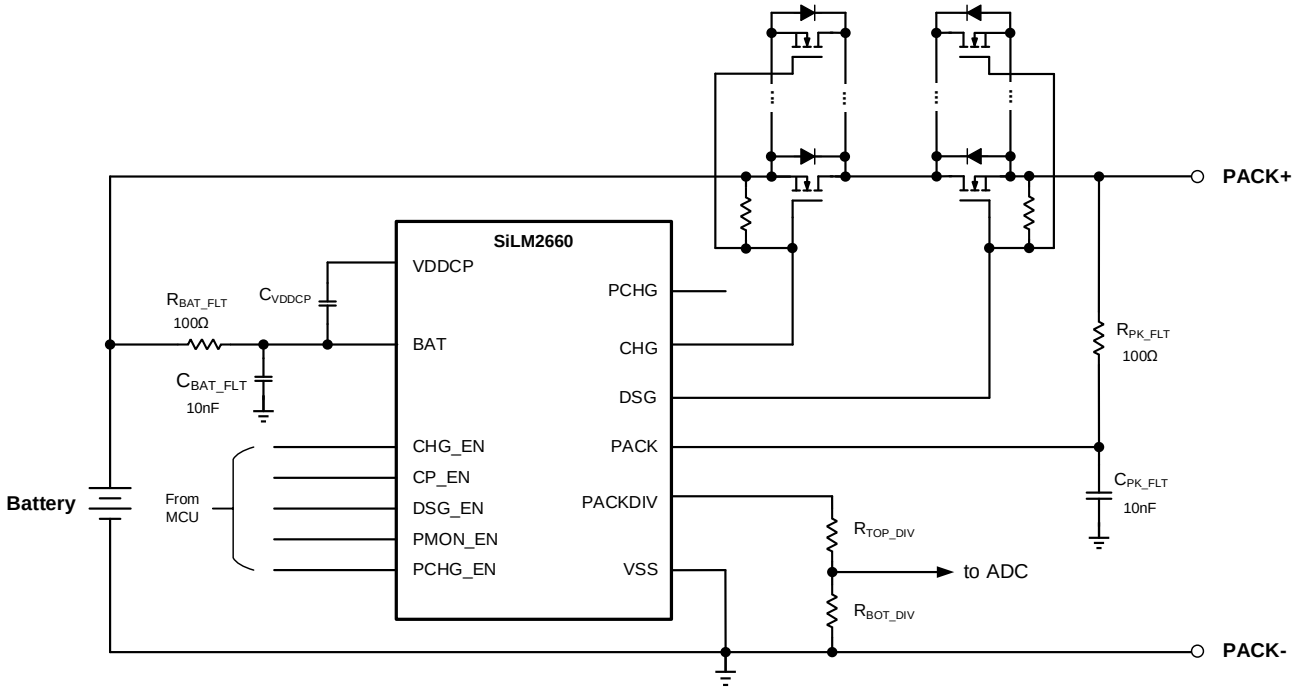


Figure 8. Scale VDDCP Capacitor to Support Multiple FETs in Parallel

The ratio of the VDDCP capacitance and loading capacitance is around 15 to 20. For example, a 470nF VDDCP capacitor can support up to approximately 30nF loading capacitance. A larger VDDCP capacitor increases the charge pump start up time; a higher loading capacitance increases the FET on and off time. During the design, system performance should be checked across the operation range and ensure the design margin.

Precharge and Predischarge Support

For a deeply depleted battery pack, a much lower charging current, for example, a C/10 rate, is usually used to precharage the battery cells. This allows the passivating layer of the cell to be recovered slowly (the passivating layer might be dissolved in the deep discharge state).

The SiLM2660 has a PCHG output to drive an external P-channel FET to support battery precharge. In this scenario, the external P-channel FET is placed in parallel with the CHG FET and a power resistor can be connected in series of the P-channel FET to limit the charging current during the precharge state. The MCU can be used to control the PCHG_EN pin to determine the entry and exit of the precharge mode.

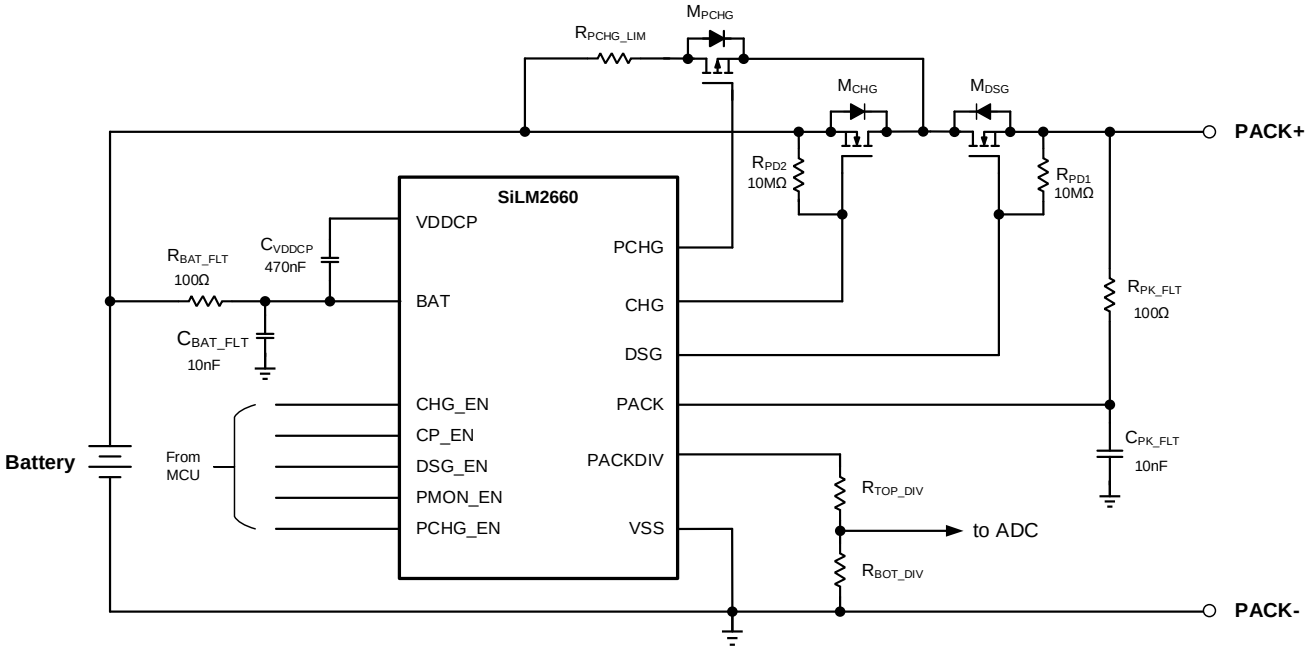


Figure 9. P-Channel FET in Parallel with CHG FET for Pre-Charging

Alternatively, the CHG pin can also be used to precharge a battery pack given if the charging current is controlled by the system (that is, does not require external component to limit the charging current such as a smart charger) and the battery stack voltage is higher than minimum operation voltage of the SiLM2660 (that is the charge pump can start to turn on the CHG FET). PCHG should leave floating if it is not used in the application.

The PCHG output can be used to predischarge a high-capacitive system. For example, a load removal can be one of the recovery requirements after a discharge related fault has been detected. In a high-capacitive system, the residual voltage at the system side can take a significant time to bleed off. This results in an additional delay in fault recovery. The PCHG output can be used to control an external P-channel FET placed in parallel with the DSG FET to predischarge the residual voltage in order to speed up the fault recovery process.

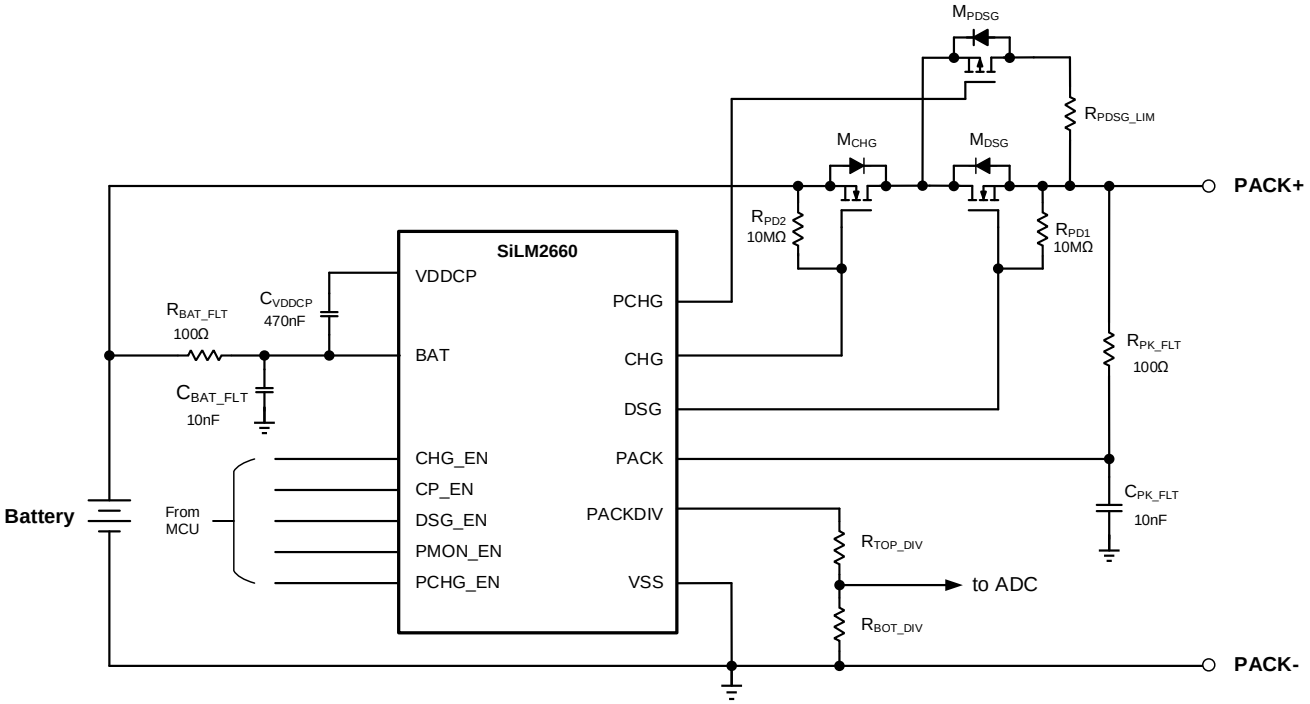


Figure 10. P-Channel FET in Parallel with DSG FET for Pre-Discharging

Optional External Gate Resistor

The CHG and DSG have certain internal on and off resistance. However, an optional external gate resistor can be added to CHG and/or DSG FET to slow down the FET on and off timing.

Separate Charge and Discharge Paths

In some systems, the charging current might be significantly lower than the discharge current. In such systems, the system designer may prefer to implement a separate charge and discharge paths in which the number of FET in parallel for charge and discharge can be different to reduce to BOM cost.

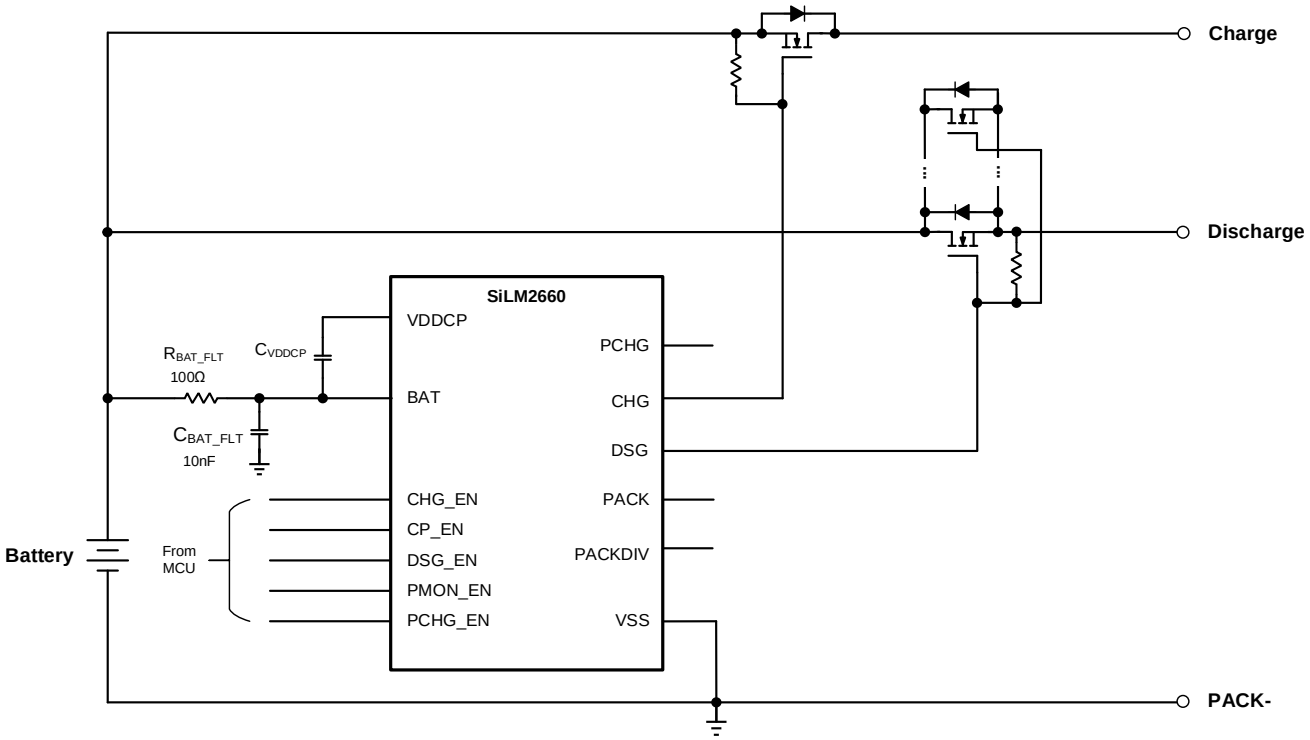
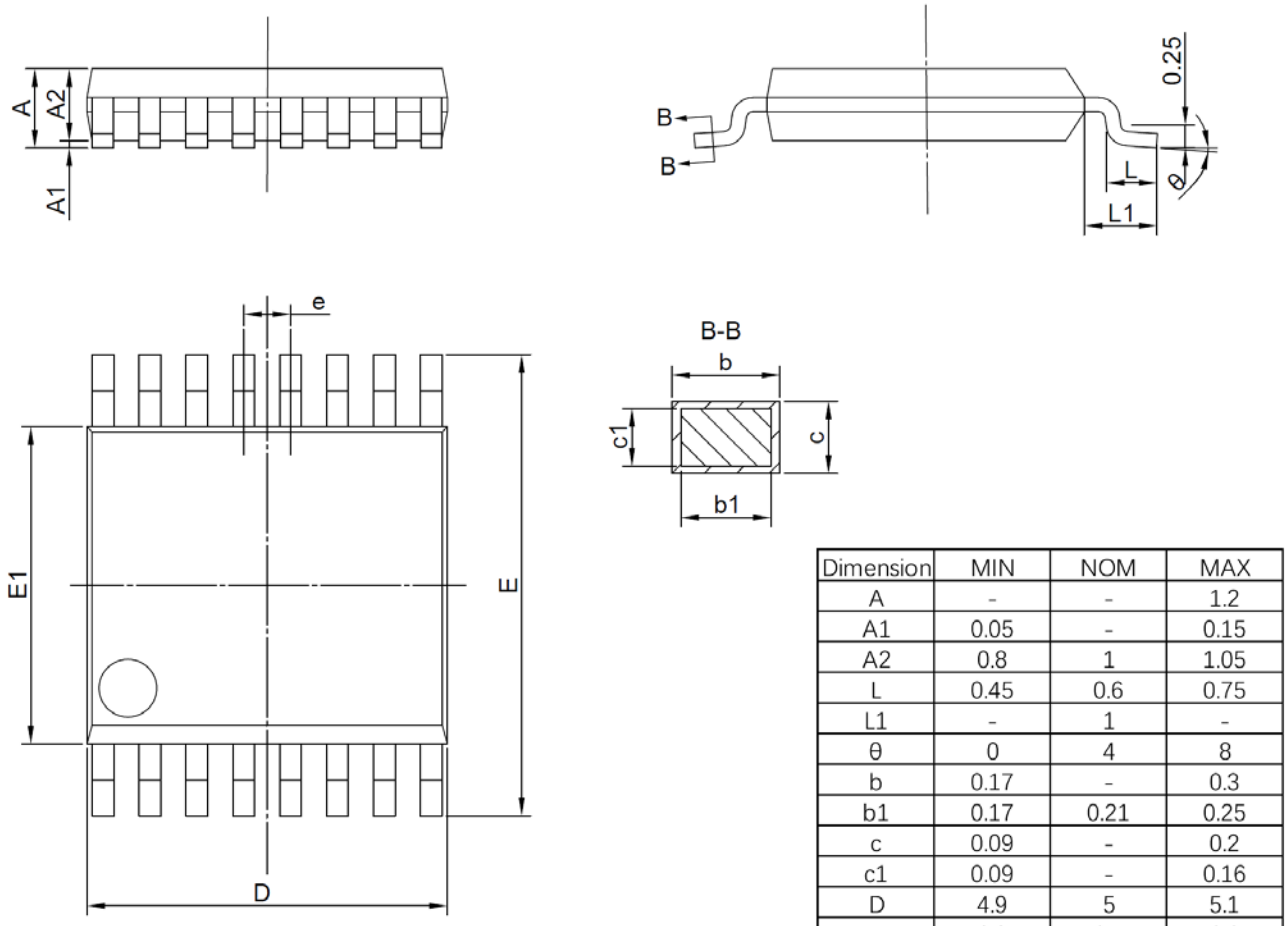


Figure 11. Separate Charge and Discharge Paths

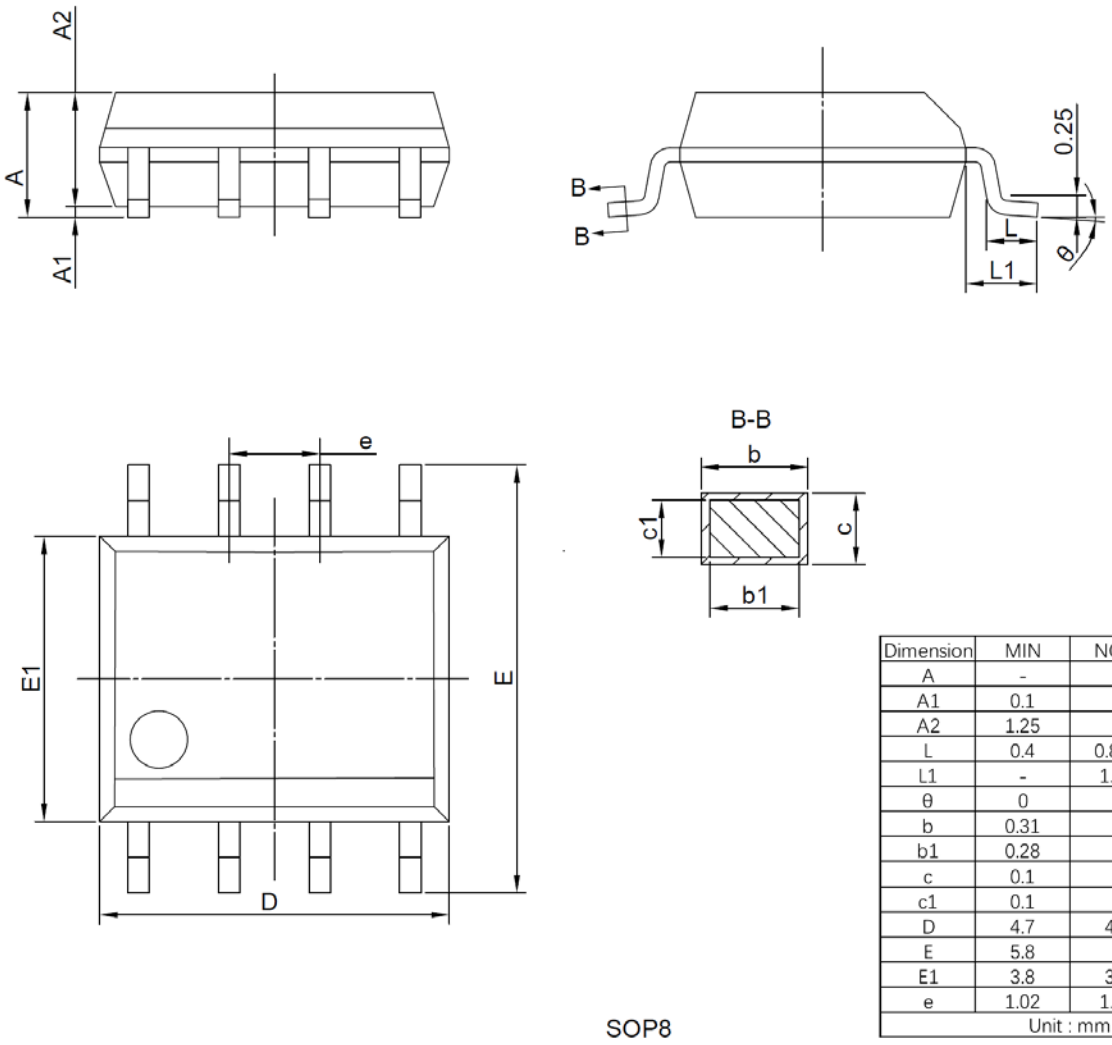
PACKAGE CASE OUTLINES



Dimension	MIN	NOM	MAX
A	-	-	1.2
A1	0.05	-	0.15
A2	0.8	1	1.05
L	0.45	0.6	0.75
L1	-	1	-
θ	0	4	8
b	0.17	-	0.3
b1	0.17	0.21	0.25
c	0.09	-	0.2
c1	0.09	-	0.16
D	4.9	5	5.1
E	6.2	6.4	6.6
E1	4.3	4.4	4.5
e	0.55	0.65	0.75
Unit : mm			

TSSOP16

Figure 12. TSSOP16 Outline Dimensions



Dimension	MIN	NOM	MAX
A	-	-	1.75
A1	0.1	-	0.25
A2	1.25	-	-
L	0.4	0.835	1.27
L1	-	1.04	-
θ	0	-	8
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.1	-	0.25
c1	0.1	-	0.25
D	4.7	4.9	5.1
E	5.8	6	6.2
E1	3.8	3.9	4
e	1.02	1.27	1.52
Unit : mm			

SOP8

Figure 13. SOP8 Outline Dimensions

REVISION HISTORY

Note: page numbers for previous revisions may differ from page numbers in current version

Page or Item	Subjects (major changes since previous revision)
Rev 1.0 datasheet, 2023-11-20	
Whole document	Initial release