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# FAN7317

## LCD Backlight Inverter Drive IC

### Features

- High-Efficiency Single-Stage Power Conversion
- Wide Input Voltage Range: 6V to 24V
- Backlight Lamp Ballast and Soft Dimming
- Minimal Required External Components
- Precision Voltage Reference Trimmed to 2%
- ZVS Full-Bridge Topology
- Soft-Start
- PWM Control at Fixed Frequency
- Burst Dimming Function
- Programmable Striking Frequency
- Open-Lamp Protection
- Open-Lamp Regulation
- Arc Protection
- Short-Lamp Protection
- CMP-High Protection
- High-FB Protection
- Thermal Shutdown
- 20-Pin SOIC

### Applications

- LCD TV
- LCD Monitor

### Description

The FAN7317 is a LCD backlight inverter drive IC that controls P-N full-bridge topology by using the new proprietary phase-shift method.

The FAN7317 provides a low-cost solution and reduces external components by integrating full wave rectifiers for open-lamp protection and regulation. The operating voltage range of the FAN7317 is wide, so an external regulator isn't necessary to supply the voltage to the IC.

The FAN7317 provides various protections, such as open-lamp regulation, open-lamp protection, arc protection, short-lamp protection, CMP-high protection, and FB-high protection, to increase the system reliability. The FAN7317 provides burst dimming function and analog dimming is possible, in a narrow range, by adding some external components.


The FAN7317 is available in a 20-SOIC package.

**20-SOIC**



### Ordering Information

Part Number	Package	Operating Temperature	Packing Method
FAN7317M	20-SOIC	-25 to +85°C	RAIL
FAN7317MX	20-SOIC	-25 to +85°C	TAPE & REEL

 All packages are lead free per JEDEC: J-STD-020B standard.

# Block Diagram

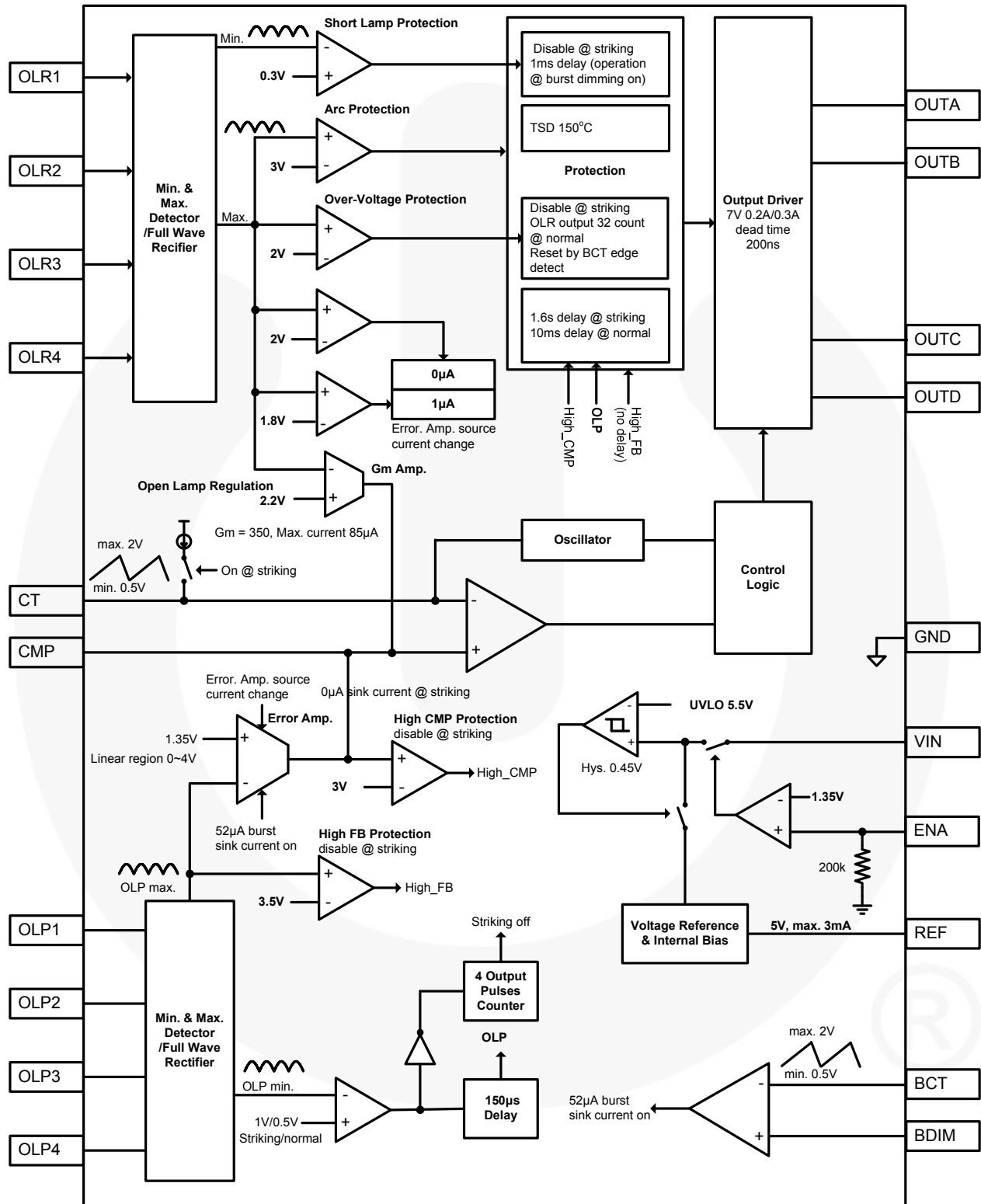
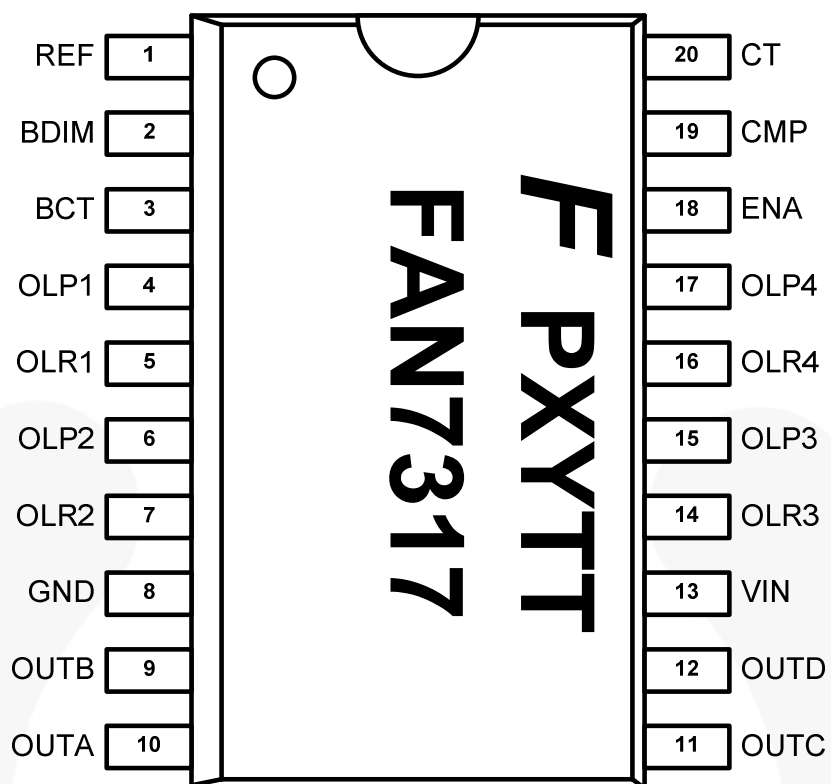


Figure 1. Internal Block Diagram

## Pin Configuration



**F** : Fairchild logo  
**P** : Assembly site code  
**XY** : Year & weekly code  
**TT** : Die run code  
**FAN7317** : Device name

Figure 2. Package Diagram

## Pin Definitions

Pin #	Name	Description
1	REF	This pin is 5V reference output. Typically, resistors are connected to this pin from CT pin and BCT pin.
2	BDIM	This pin is the input for burst dimming. The voltage range of 0.5 to 2V at this pin controls burst mode duty cycle from 0% to 100%.
3	BCT	This pin is for programming the frequency of the burst dimming. Typically, a capacitor is connected to this pin from ground and a resistor is connected to this pin from the REF pin.
4	OLP1	This pin is for open-lamp protection and feedback control of lamp currents. It has the same functions as other OLP pins and is connected to the full-wave rectifier internally. In striking mode, if the minimum of rectified OLP inputs is less than 1V for 1.6s; or in normal mode, if the minimum of rectified OLP inputs is less than 0.5V for 10ms; the IC shuts down to protect the system in open lamp condition. The maximum of rectified OLP inputs is inputted to the negative of the error amplifier for feedback control of lamp current.
5	OLR1	This pin is for open-lamp regulation. It has the same functions as other OLR pins and is connected to the full-wave rectifier internally. When the maximum of rectified OLR inputs is between 1.8V and 2V, the error amplifier output current is limited to 1 $\mu$ A; and when the maximum of rectified OLR inputs reaches 2V, the error amplifier output current is 0A and its output voltage maintains constant. The maximum of rectified OLR inputs is inputted to the negative of another error amplifier for feedback control of lamp voltage. When the maximum of rectified OLR inputs is more than 2.2V, another error amplifier for OLR is operating and lamp voltage is regulated.
6	OLP2	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.
7	OLR2	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.
8	GND	This pin is the ground.
9	OUTB	This pin is NMOS gate-drive output.
10	OUTA	This pin is PMOS gate-drive output.
11	OUTC	This pin is PMOS gate-drive output.
12	OUTD	This pin is NMOS gate-drive output.
13	VIN	This pin is the supply voltage of the IC.
14	OLR3	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.
15	OLP3	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.
16	OLR4	This pin is for open-lamp regulation. Its functions are the same as the OLR1 pin.
17	OLP4	This pin is for open-lamp protection and feedback control of lamp currents. Its functions are the same as the OLP1 pin.
18	ENA	This pin is for turning on/off the IC.
19	CMP	Error amplifier output. Typically, a compensation capacitor is connected to this pin from the ground.
20	CT	This pin is for programming the switching frequency. Typically, a capacitor is connected to this pin from ground and a resistor is connected to this pin from the REF pin.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{IN}$	IC Supply Voltage	6	24	V
$T_A$	Operating Temperature Range	-25	+85	°C
$T_J$	Operating Junction Temperature		+150	°C
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$\theta_{JA}$	Thermal Resistance Junction-Air <sup>(1,2)</sup>		90	°C/W
$P_D$	Power Dissipation		1.4	W

### Notes:

1. Thermal resistance test board. Size: 76.2mm x 114.3mm x 1.6mm (1S0P); JEDEC standard: JESD51-2, JESD51-3.
2. Assume no ambient airflow.

## Pin Breakdown Voltage

Pin #	Name	Value	Unit	Pin #	Name	Value	Unit
1	REF	7	V	11	OUTC	24	V
2	BDIM	7		12	OUTD	7	
3	BCT	7		13	VIN	24	
4	OLP1	±7		14	OLR3	±7	
5	OLR1	±7		15	OLP3	±7	
6	OLP2	±7		16	OLR4	±7	
7	OLR2	±7		17	OLP4	±7	
8	GND	7		18	ENA	7	
9	OUTB	7		19	CMP	7	
10	OUTA	24		20	CT	7	

## Electrical Characteristics

For typical values,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 15\text{V}$ , and  $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , unless otherwise specified. Specifications to  $-25^\circ\text{C} \sim 85^\circ\text{C}$  are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Under-Voltage Lockout Section (UVLO)</b>						
$V_{th}$	Start Threshold Voltage		4.9	5.2	5.5	V
$V_{thys}$	Start Threshold Voltage Hysteresis		0.20	0.45	0.60	V
$I_{st}$	Start-up Current	$V_{IN} = 4.5\text{V}$		70	100	$\mu\text{A}$
$I_{op}$	Operating Supply Current	$V_{IN} = 15\text{V}$ , Not switching		2.0	3.5	mA
<b>ON/OFF Section</b>						
$V_{on}$	On State Input Voltage		2		5	V
$V_{off}$	Off Stage Input Voltage				0.7	V
$I_{sb}$	Stand-by Current	$V_{IN} = 15\text{V}$ , ENA = Low		120	170	$\mu\text{A}$
$R_{ENA}$	Pull-down Resistor		130	200	270	k $\Omega$
<b>Reference Section (Recommend 1<math>\mu\text{F}</math> X7R Capacitor)</b>						
$V_5$	5V Regulation Voltage	$0 \leq I_5 \leq 3\text{mA}$	4.9	5.0	5.1	V
$V_{5line}$	5V Line Regulation	$6 (( V_{IN} ((( 24\text{V}$			50	mV
$V_{5load}$	5V Load Regulation	$I_5 = 3\text{mA}$			50	mV
<b>Oscillator Section (Main)</b>						
$f_{osc}$	Oscillation Frequency	$T_A = 25^\circ\text{C}$ , CT = 220pF, RT = 100k $\Omega$	93.9	97.0	100.5	kHz
		CT = 220pF, RT = 100k $\Omega$	93	97	101	
$f_{str}$	Oscillator Frequency in Striking Mode	$T_A = 25^\circ\text{C}$ , CT = 220pF, RT = 100k $\Omega$	120	124	129	kHz
		CT = 220pF, RT = 100k $\Omega$	119	124	129	
$I_{ctdcs}$	CT Discharge Current	Striking	0.99	1.14	1.29	mA
$I_{ctdc}$		Normal	740	840	940	$\mu\text{A}$
$I_{ctcs}$	CT Charge Current	Striking	-15	-12	-9	$\mu\text{A}$
$V_{cth}$	CT High Voltage			2		V
$V_{ctl}$	CT Low Voltage			0.4		V
<b>Oscillator Section (Burst)</b>						
$f_{oscb}$	Burst Oscillation Frequency	$T_A = 25^\circ\text{C}$ , BCT = 4.7nF, BRT = 1.4M $\Omega$	303	314	326	Hz
		BCT = 4.7nF, BRT = 1.4M $\Omega$	302	314	326	
$I_{bctdc}$	BCT Discharge Current		14	26	38	$\mu\text{A}$
$V_{bcth}$	BCT High Voltage			2		V
$V_{bctl}$	BCT Low Voltage			0.5		V

**Electrical Characteristics** (Continued)

For typical values,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 15\text{V}$ , and  $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , unless otherwise specified. Specifications to  $-25^\circ\text{C} \sim 85^\circ\text{C}$  are guaranteed by design based on final characterization results.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
<b>Error Amplifier Section</b>						
$A_V$	Open-loop Gain <sup>(3)</sup>			37		dB
$G_m$	Error Amplifier Trans-conductance		20	40	60	$\mu\text{mho}$
$I_{sin}$	Output Sink Current	OLP = 2.25V	-50	-35	-20	$\mu\text{A}$
$I_{sur}$	Output Source Current	OLP = 0.8V	12	22	32	$\mu\text{A}$
$I_{bsin}$	Burst CMP Sink Current		38	52	66	$\mu\text{A}$
$V_{135p}$	1.35V Regulation Voltage	$T_A = 25^\circ\text{C}$	1.275	1.350	1.421	V
			1.255	1.350	1.444	
$I_{olpi}$	OLP Input Current	OLP = 2V	-1	0	1	$\mu\text{A}$
$I_{olpo}$	OLP Output Current	OLP = -2V	-30	-20	-10	$\mu\text{A}$
$V_{olpr}$	OLP Input Voltage Range <sup>(3)</sup>		-4		4	V
<b>Open-Lamp Regulation Section</b>						
$I_{olr1}$	Error Amplifier Source Current for Open-Lamp Regulation	Striking, OLR = $V_{olr1} + 0.05$	-2.0	-1.0	-0.1	$\mu\text{A}$
$I_{olr2}$		OLR = 2.1V		0		$\mu\text{A}$
$V_{olr1}$	Open-Lamp Regulation Voltage 1	Striking	1.65	1.80	1.95	V
$V_{olr2}$	Open-Lamp Regulation Voltage 2	Striking	1.95	2.05	2.15	V
$V_{olr3}$	Open-Lamp Regulation Voltage 3		2.1	2.2	2.3	V
$G_{mOLR}$	OLR Error Amplifier Trans-conductance		200	350	500	$\mu\text{mho}$
$I_{olrsi}$	OLR Error Amplifier Sink Current	Normal, OLR = 2.5V	50	70	90	$\mu\text{A}$
$I_{olri}$	OLR Input Current	OLR = 1.5V	10	17	24	$\mu\text{A}$
$I_{olro}$	OLR Output Current	OLR = -1.5V	-25	-15	-7	$\mu\text{A}$
$V_{olrr}$	OLR Input Voltage Range <sup>(3)</sup>		-4		4	V

**Note:**

3. These parameters, although guaranteed, are not 100% tested in production.



**Electrical Characteristics** (Continued)

For typical values,  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 15\text{V}$ , and  $-25^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$ , unless otherwise specified. Specifications to  $-25^\circ\text{C} \sim 85^\circ\text{C}$  are guaranteed by design based on final characterization results.

Protection Section						
$V_{olp0}$	Open-Lamp Protection Voltage 0 <sup>(4)</sup>	Open Lamp in Striking	0.95	1.00	1.05	V
$V_{olp1}$	Open-Lamp Protection Voltage 1	Open Lamp	0.44	0.51	0.58	V
$V_{cmpr}$	CMP-High Protection Voltage		2.95	3.05	3.15	V
$V_{arcp}$	Arc Protection Voltage		2.90	3.05	3.20	V
$V_{hfbp}$	High-FB Protection Voltage <sup>(4)</sup>		3.4	3.5	3.6	V
$V_{slp}$	Short Lamp Protection Voltage		0.24	0.32	0.40	V
$T_{olps}$	Open-Lamp Protection Delay <sup>(4)</sup>	Striking, $f_{osc} = 330\text{Hz}$		1.6		s
$T_{olpn}$		Normal, $f_{osc} = 100\text{kHz}$		10		ms
$T_{cmprs}$	High-CMP Protection Delay <sup>(4)</sup>	Striking, $f_{osc} = 330\text{Hz}$		1.6		s
$T_{cmprn}$		Normal, $f_{osc} = 100\text{kHz}$		10		ms
$T_{olr}$	Open-Lamp Regulation Delay <sup>(4)</sup>	Normal, $f_{osc} = 100\text{kHz}$		320		$\mu\text{s}$
$T_{slp}$	Short Lamp Protection Delay <sup>(4)</sup>	Normal, $f_{osc} = 100\text{kHz}$		1		ms
TSD	Thermal Shutdown <sup>(4)</sup>			150		$^\circ\text{C}$
Output Section						
$V_{pdhv}$	PMOS Gate High Voltage <sup>(4)</sup>	$V_{IN} = 15\text{V}$		$V_{IN}$		V
$V_{phlv}$	PMOS Gate Low Voltage	$V_{IN} = 15\text{V}$	$V_{IN}-6.5$	$V_{IN}-7$	$V_{IN}-7.5$	V
$V_{ndhv}$	NMOS Gate High Voltage	$V_{IN} = 15\text{V}$	6.5	7.0	7.5	V
$V_{ndlv}$	NMOS Gate Low Voltage <sup>(4)</sup>	$V_{IN} = 15\text{V}$		0		V
$V_{puv}$	PMOS Gate Voltage with UVLO Activated	$V_{IN} = 4.5\text{V}$	$V_{IN}-0.3$			V
$V_{nuv}$	NMOS Gate Voltage with UVLO Activated	$V_{IN} = 4.5\text{V}$			0.3	V
$I_{pdsur}$	PMOS Gate Drive Source Current <sup>(4)</sup>	$V_{IN} = 15\text{V}$		-200		mA
$I_{pdsin}$	PMOS Gate Drive Sink Current <sup>(4)</sup>	$V_{IN} = 15\text{V}$		300		mA
$I_{nds sur}$	NMOS Gate Drive Source Current <sup>(4)</sup>	$V_{IN} = 15\text{V}$		200		mA
$I_{nds in}$	NMOS Gate Drive Sink Current <sup>(4)</sup>	$V_{IN} = 15\text{V}$		-300		mA
$t_r$	Rising Time <sup>(4)</sup>	$V_{IN} = 15\text{V}$ , $C_{load} = 2\text{nF}$		70		ns
$t_f$	Falling Time <sup>(4)</sup>	$V_{IN} = 15\text{V}$ , $C_{load} = 2\text{nF}$		70		ns
Maximum / Minimum Overlap						
	Minimum Overlap Between Diagonal Switches <sup>(4)</sup>	$f_{osc} = 100\text{kHz}$		0		%
	Maximum Overlap Between Diagonal Switches <sup>(4)</sup>	$f_{osc} = 100\text{kHz}$	86		90	%
Dead Time						
	PDR_A/NDR_B <sup>(4)</sup>		150	200	250	ns
	PDR_C/NDR_D <sup>(4)</sup>		150	200	250	ns

**Note:**

4. These Parameters, although guaranteed, are not 100% tested in production.

## Typical Performance Characteristics

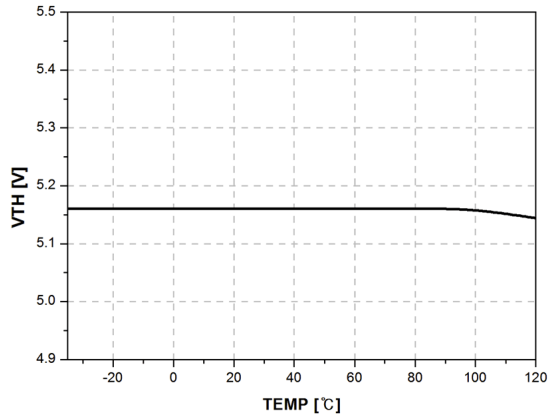


Figure 3. Start Threshold Voltage vs. Temp.

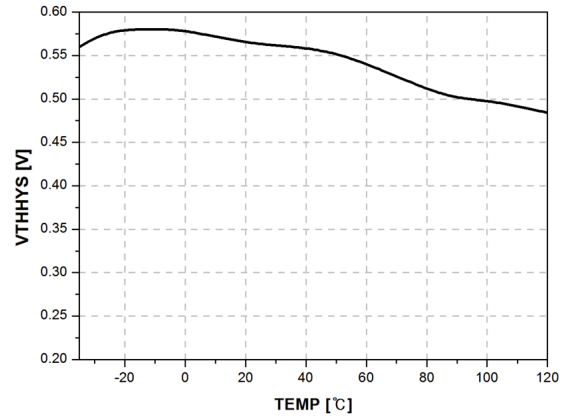


Figure 4. Start Threshold Voltage Hys. vs. Temp.

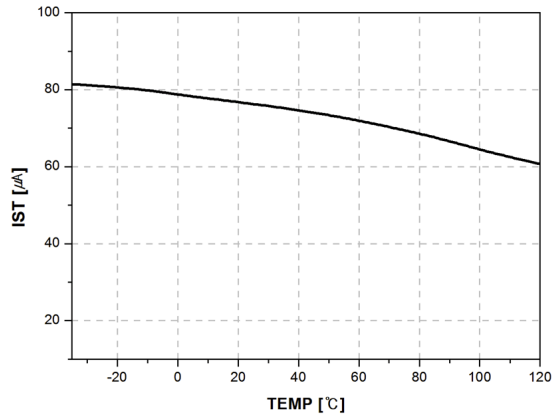


Figure 5. Start-up Current vs. Temp.

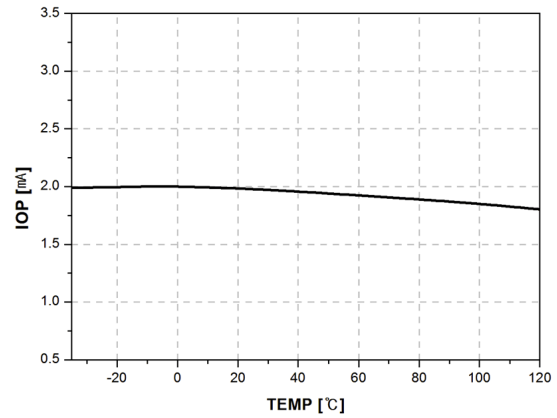


Figure 6. Operating Current vs. Temp.

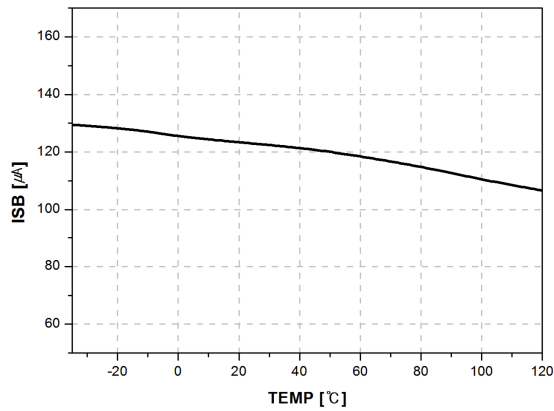


Figure 7. Standby Current vs. Temp.

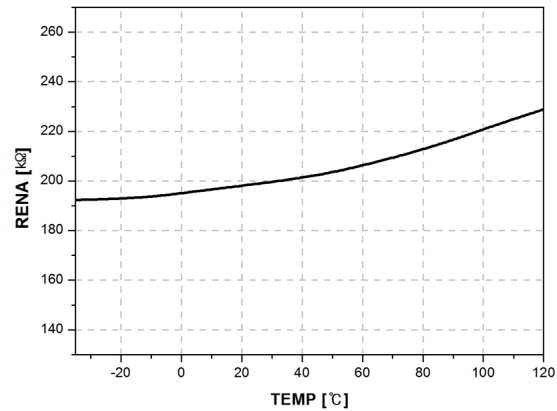


Figure 8. Pull-down Resistor vs. Temp.

## Typical Performance Characteristics (Continued)

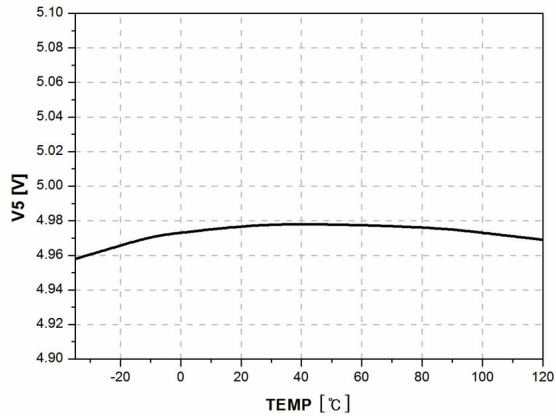


Figure 9. 5V Regulation Voltage vs. Temp.

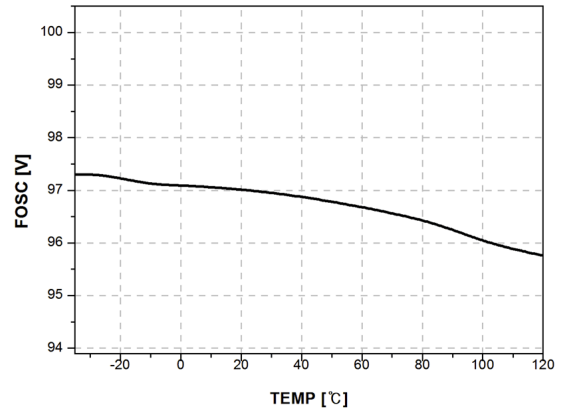


Figure 10. Oscillation Frequency vs. Temp.

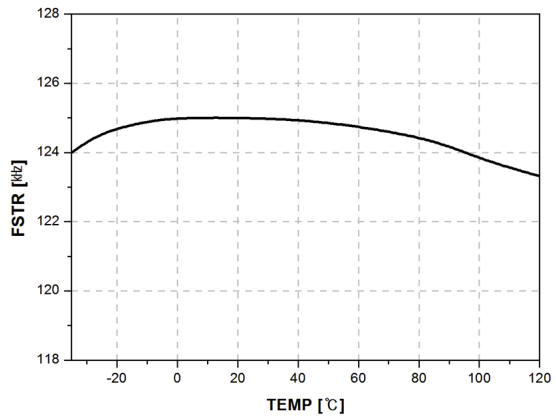


Figure 11. Oscillation Frequency in Striking vs. Temp.

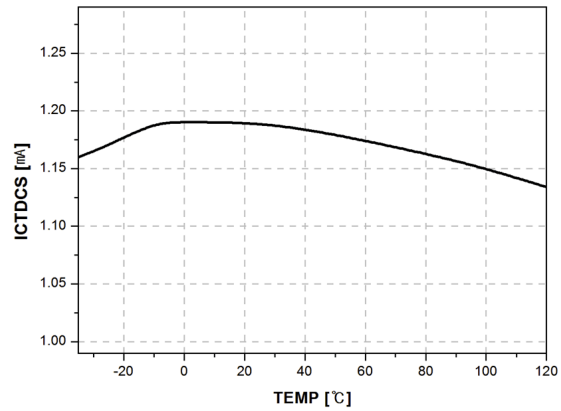


Figure 12. CT Discharge Current in Striking vs. Temp.

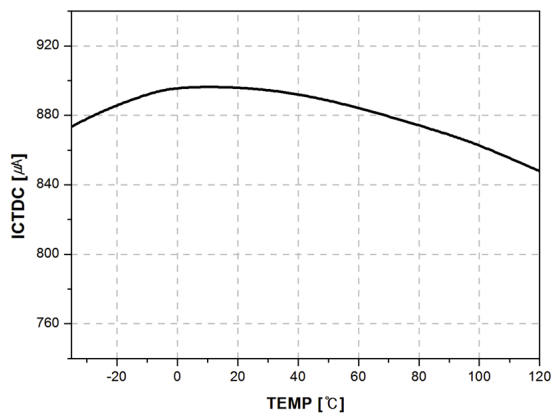


Figure 13. CT Discharge Current vs. Temp.

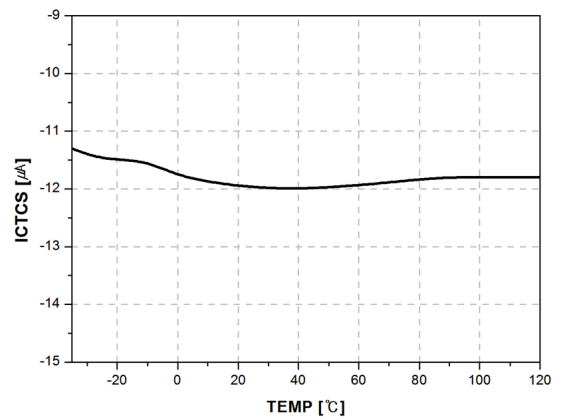


Figure 14. CT Charge Current vs. Temp.

## Typical Performance Characteristics (Continued)

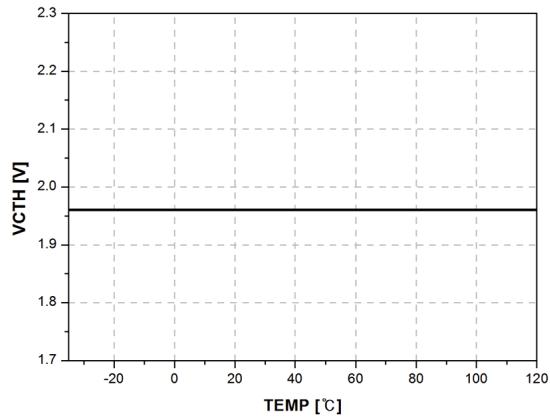


Figure 15. CT High Voltage vs. Temp.

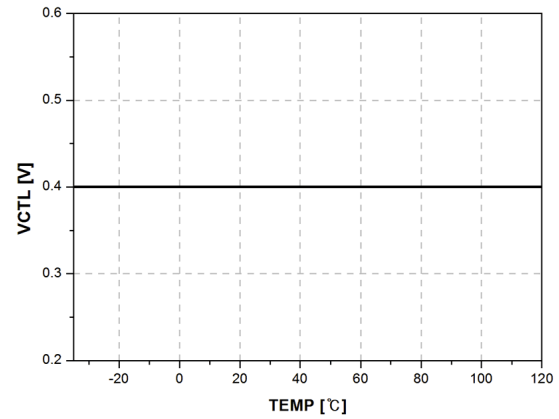


Figure 16. CT Low Voltage vs. Temp.

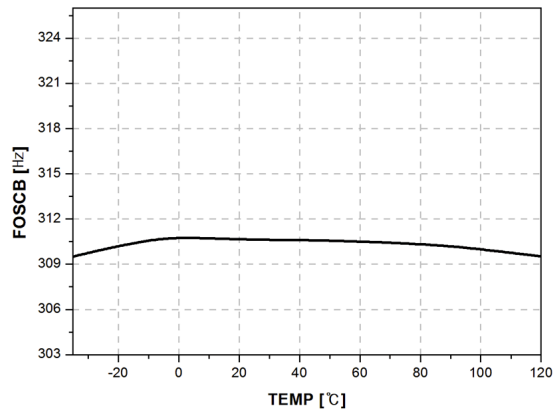


Figure 17. Burst Dimming Frequency vs. Temp.

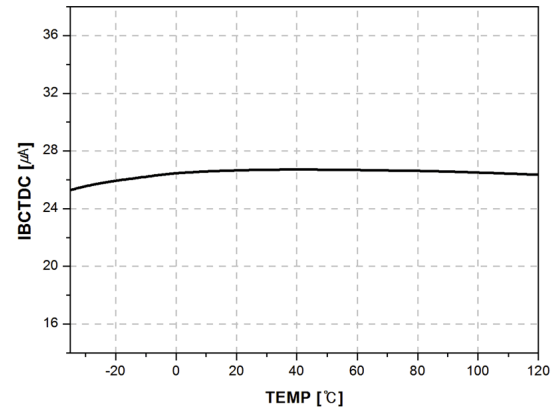


Figure 18. BCT Discharge Current vs. Temp.

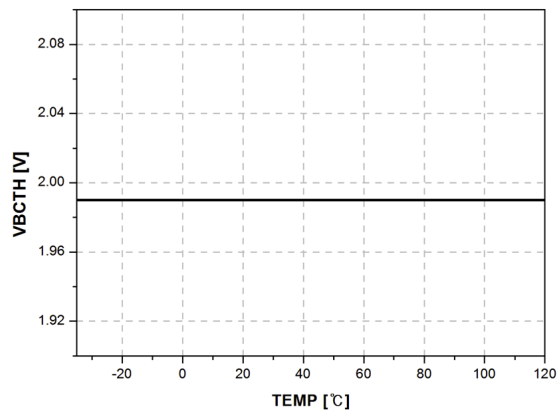


Figure 19. BCT High Voltage vs. Temp.

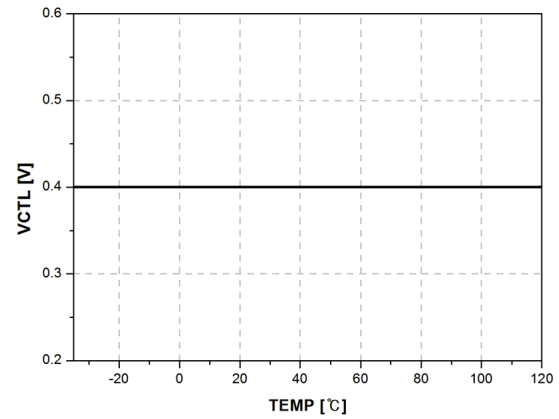


Figure 20. BCT Low Voltage vs. Temp.

# Typical Performance Characteristics (Continued)

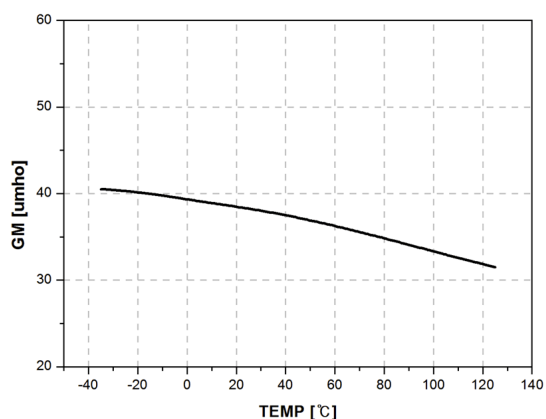


Figure 21. Error Amp. GM vs. Temp.

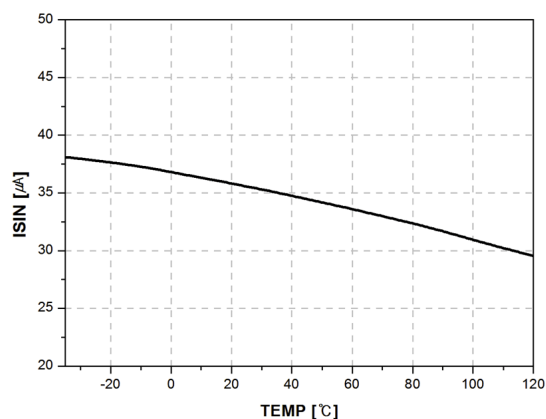


Figure 22. Error Amp. Sink Current vs. Temp.

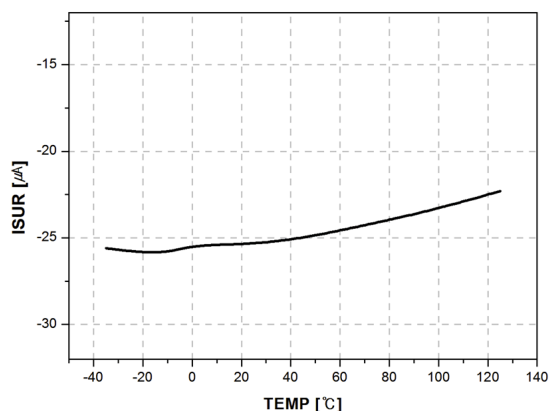


Figure 23. Error Amp. Source Current vs. Temp.

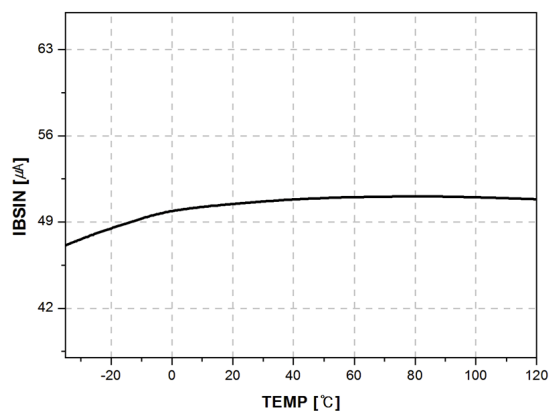


Figure 24. Burst CMP Sink Current vs. Temp.

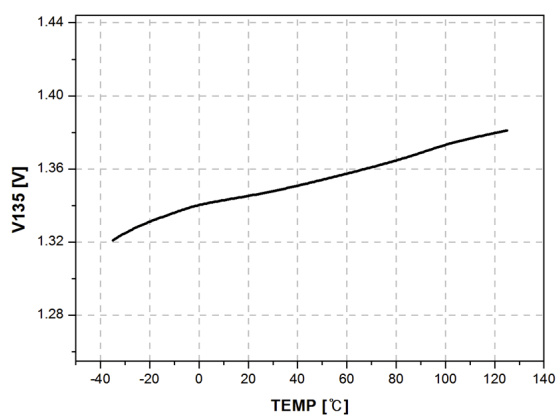


Figure 25. 1.35V Regulation Voltage vs. Temp.

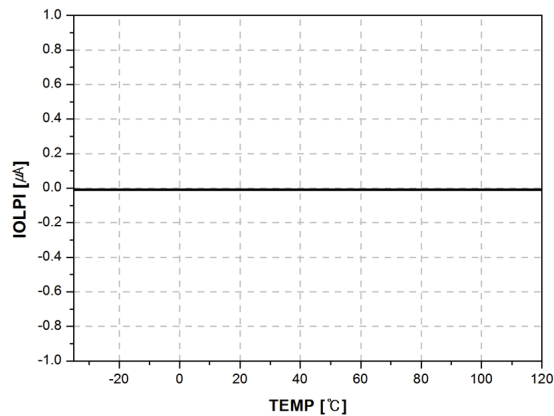


Figure 26. OLP Input Current vs. Temp.

## Typical Performance Characteristics (Continued)

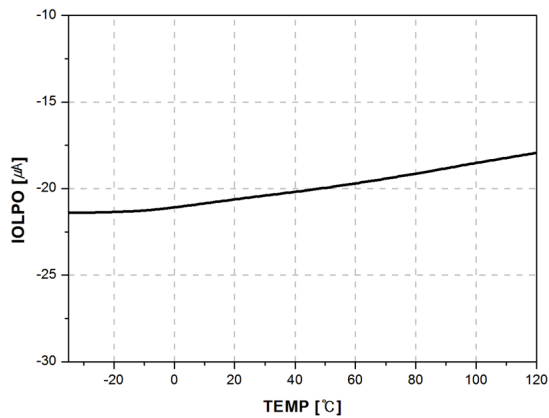


Figure 27. OLP Output Current vs. Temp.

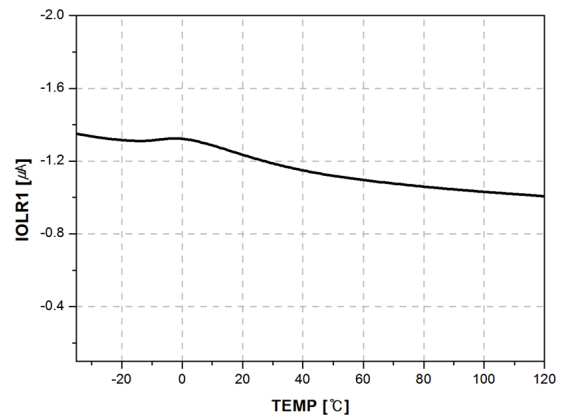


Figure 28. Error Amp. Source Current 1 vs. Temp.

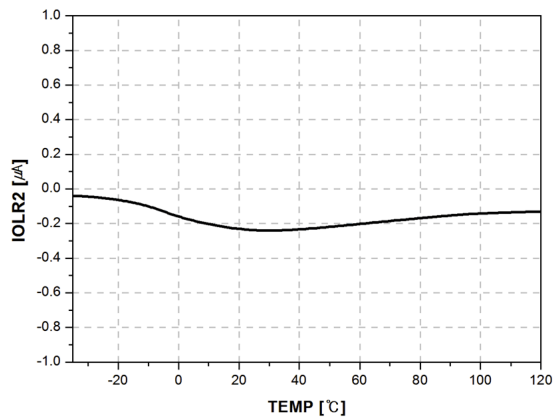


Figure 29. Error Amp. Source Current 2 vs. Temp.

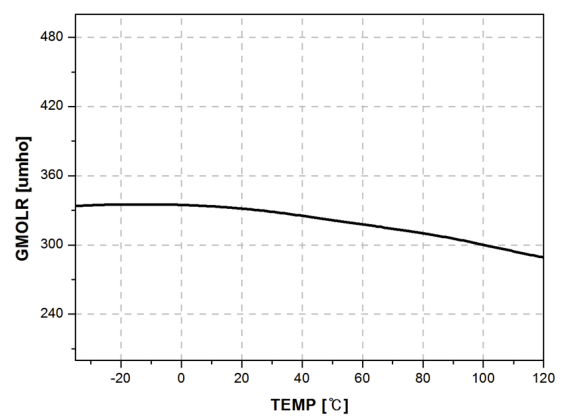


Figure 30. OLR Error Amp. GM vs. Temp.

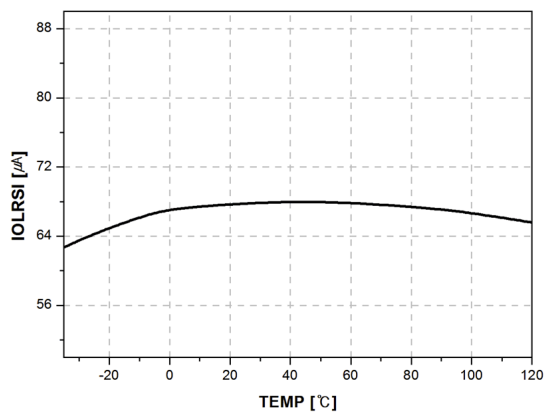


Figure 31. OLR Error Amp. Sink Current vs. Temp.

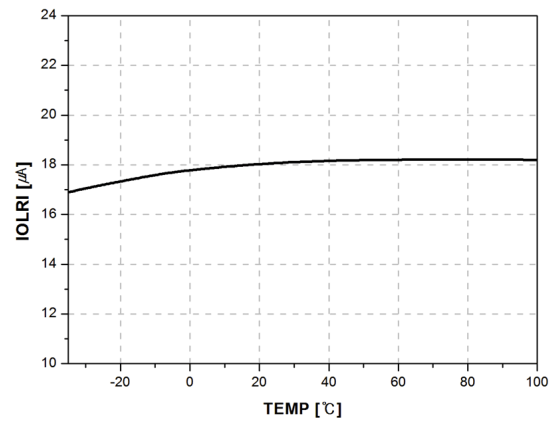


Figure 32. OLR Input Current vs. Temp.

## Typical Performance Characteristics (Continued)

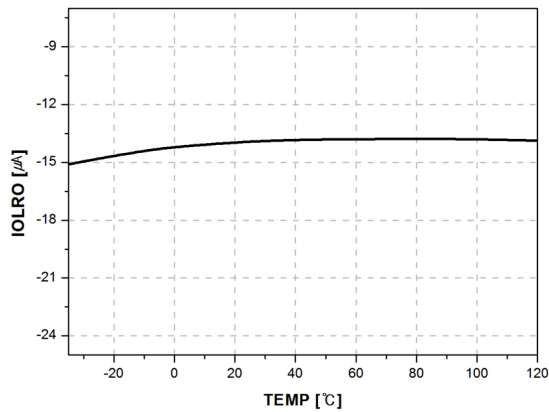


Figure 33. OLR Output Current vs. Temp.

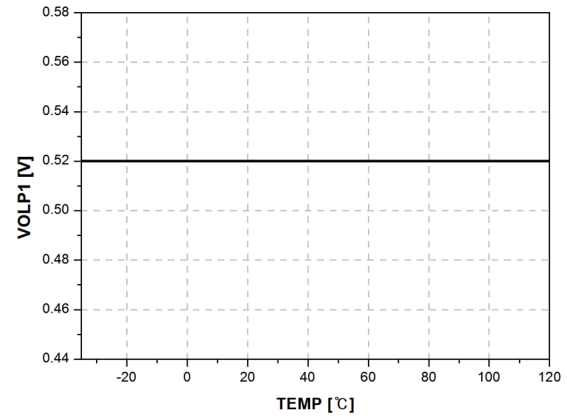


Figure 34. Open-Lamp Protection Voltage1 vs. Temp.

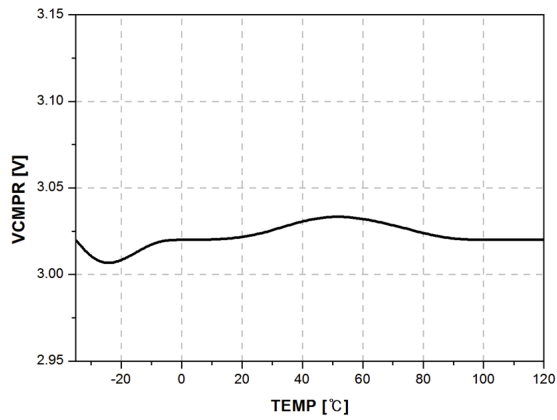


Figure 35. High-CMP Protection Voltage vs. Temp.

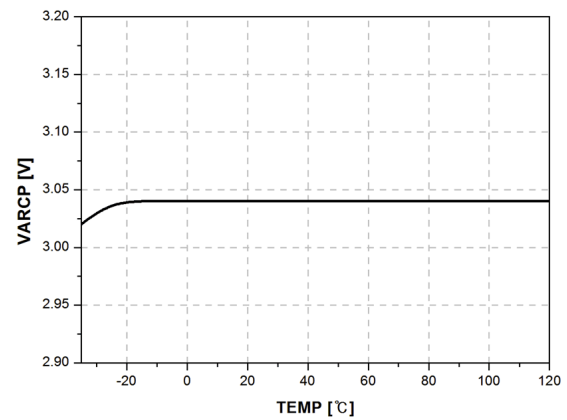


Figure 36. Arc Protection Voltage vs. Temp.

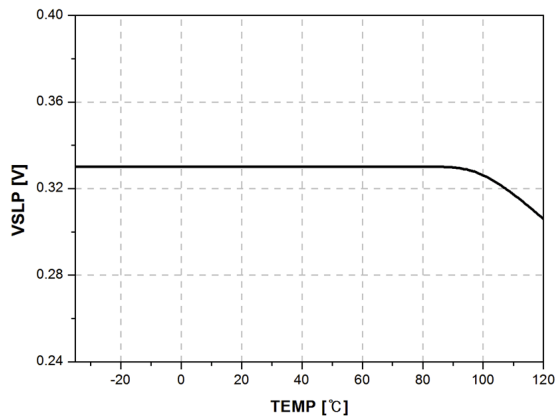


Figure 37. Short Lamp Protection Voltage vs. Temp.

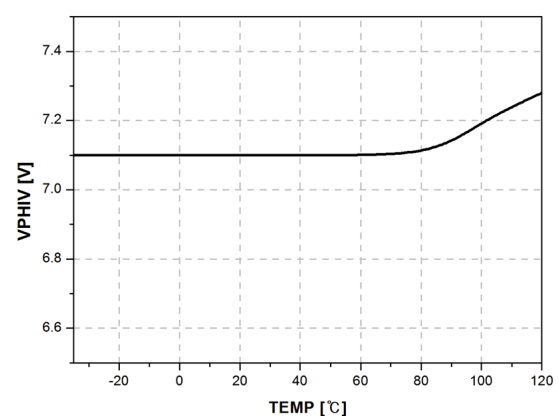


Figure 38. PMOS Gate Low Voltage vs. Temp.

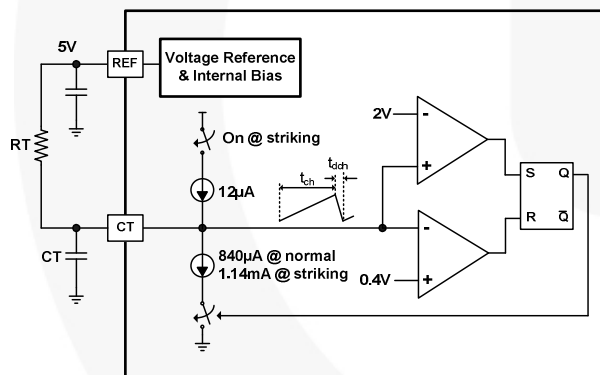
## Functional Description

**UVLO:** The under-voltage lockout (UVLO) circuit guarantees the stable operation of the IC's control circuit by stopping and starting it as a function of the  $V_{IN}$  value. The UVLO circuit turns on the control circuit when  $V_{IN}$  exceeds 5.2V. When  $V_{IN}$  is lower than 4.75V, the IC start-up current is less than 100 $\mu$ A.

**ENA:** Applying voltage higher than 2V to the ENA pin enables the IC. Applying voltage lower than 0.7V to the ENA pin disables the IC.

**Main Oscillator:** In normal mode, the external timing capacitor (CT) is charged by the current flowing from the reference voltage source, which is formed by the timing resistor (RT) and the timing capacitor (CT). The sawtooth waveform charges up to 2V. Once CT voltage reaches 2V, the CT begins discharging down to 0.4V. Next, the CT starts charging again and a new switching cycle begins, as shown in Figure 39. The main frequency is programmed by adjusting the RT and CT value. The main frequency is calculated as:

$$f_{\text{osc}} = \frac{1}{RT \cdot CT \cdot \ln \left( \frac{3.864 \cdot RT - 13800}{2.52 \cdot RT - 13800} \right)} [\text{Hz}] \quad (1)$$



### Figure 39. Main Oscillator Circuit

In striking mode, the external timing capacitor (CT) is charged by the current flowing from the reference voltage source and 12 $\mu$ A current source, which increases the frequency. If the product of RT and CT value is constant, the striking frequency is depending on CT and is calculated as:

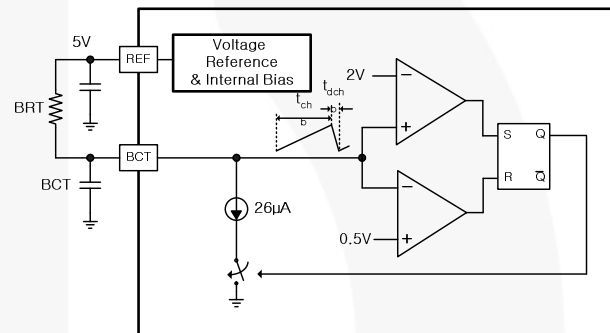
$$f_{\text{str}} = \frac{1}{RT \cdot CT \cdot \ln \left( \frac{13.8 + (3I_1 - 4.6I_2)RT}{13.8 + (4.6I_1 - 3I_2)RT} \right)} [\text{Hz}] \quad (2)$$

$$\therefore I_1 = 12 \times 10^{-6} \text{ A}, I_2 = 1.128 \times 10^{-3} \text{ A}$$

**Burst Dimming Oscillator:** The burst dimming timing capacitor (BCT) is charged by the current flowing from the reference voltage source, which is formed by the burst dimming timing resistor (BRT) and the burst dimming timing capacitor (BCT). The sawtooth waveform charges up to 2V. Once the BCT voltage reaches 2V, the capacitor begins discharging down to 0.5V. Next, the BCT starts charging again and a new burst dimming cycle begins, as shown in Figure 40. The burst dimming frequency is programmed by adjusting the BCT and BRT values. The burst dimming frequency is calculated as:

$$f_{\text{OSCB}} = \frac{1}{\text{BRT} \cdot \text{BCT} \cdot \ln\left(\frac{0.039 \cdot \text{BRT} - 4500}{0.026 \cdot \text{BRT} - 4500}\right)} [\text{Hz}] \quad (3)$$

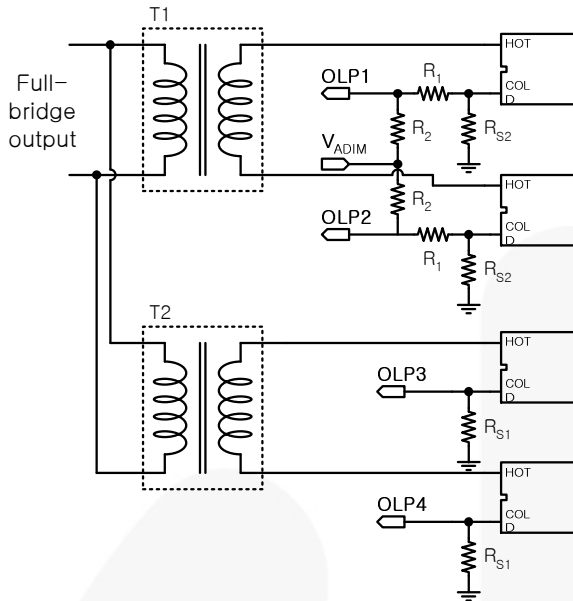
To avoid visible flicker, the burst dimming frequency should be greater than 120Hz.



**Figure 40. Burst Dimming Oscillator Circuit**

**Analog Dimming:** For analog dimming, the lamp intensity is controlled with the external dimming signal ( $V_{ADIM}$ ) and resistors. Figure 41 shows how to implement an analog dimming circuit. The polarity of OLP1 should be reversed with respect to OLP2.





**Figure 41. Analog Implementation Circuit**

In full brightness, the maximum rms value of the lamp current is calculated as:

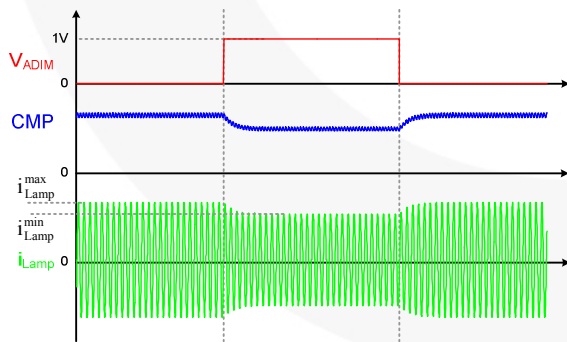
$$i_{rms}^{max} = 1.35 \frac{\pi}{2\sqrt{2}R_{S1}} [A] \quad (4)$$

The lamp intensity is inversely proportional to  $V_{ADIM}$ . As  $V_{ADIM}$  increases, the lamp intensity decreases and the rms value of the lamp current is calculated as:

$$i_{rms} = i_{rms}^{max} - \frac{\pi}{2\sqrt{2}} \frac{R_1}{R_{S2}R_2} V_{ADIM} [A] \quad (5)$$

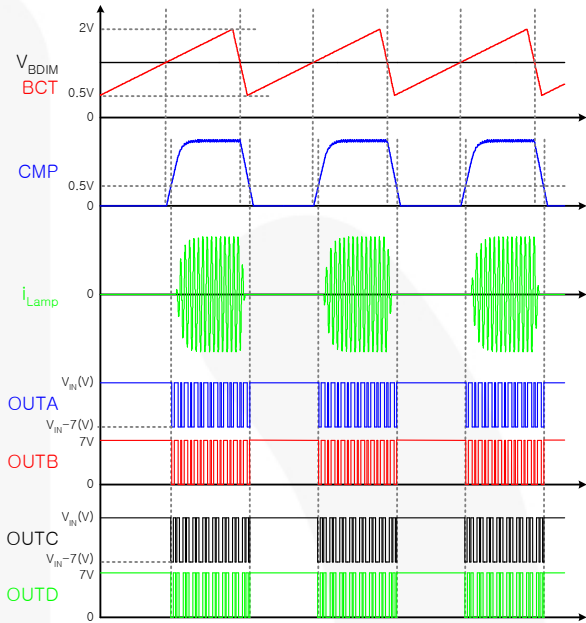
$$\therefore R_{S2} = \frac{R_1 + R_2}{R_2} R_{S1} [\Omega]$$

Figure 42 shows the lamp current waveform vs.  $V_{ADIM}$  in an analog dimming mode.



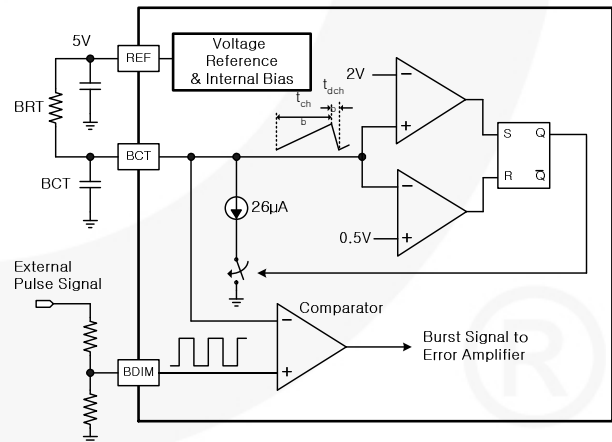
**Figure 42. Analog Dimming Waveforms**

**Burst Dimming:** Lamp intensity is controlled with the BDIM signal over a wide range. When BDIM voltage is lower than BCT voltage, the lamp current is turned on; so, 0V on BDIM commands full brightness. The duty cycle of the PWM pulse determines the lamp brightness. The lamp intensity is inversely proportional to BDIM voltage. As BDIM voltage increases, the lamp intensity decreases. Figure 43 shows the lamp current waveform vs. DIM in negative analog dimming mode.



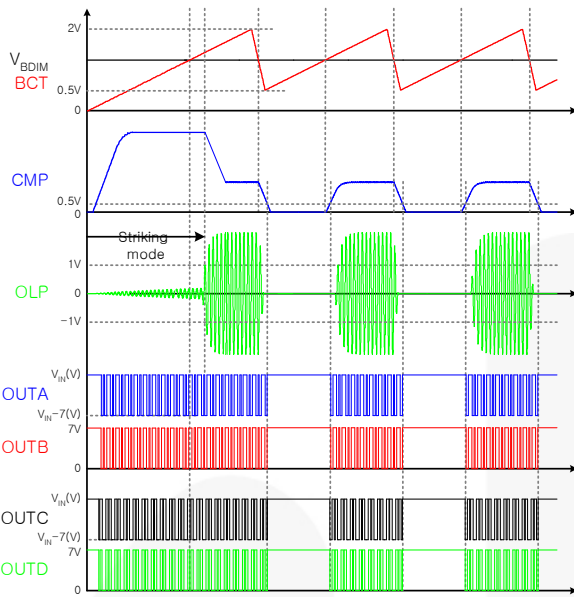
**Figure 43. Burst Dimming Waveforms**

Burst dimming can be implemented not only DC voltage, but also using PWM pulse as the BDIM signal. Figure 44 shows how to implement burst dimming using PWM pulse as BDIM signal.



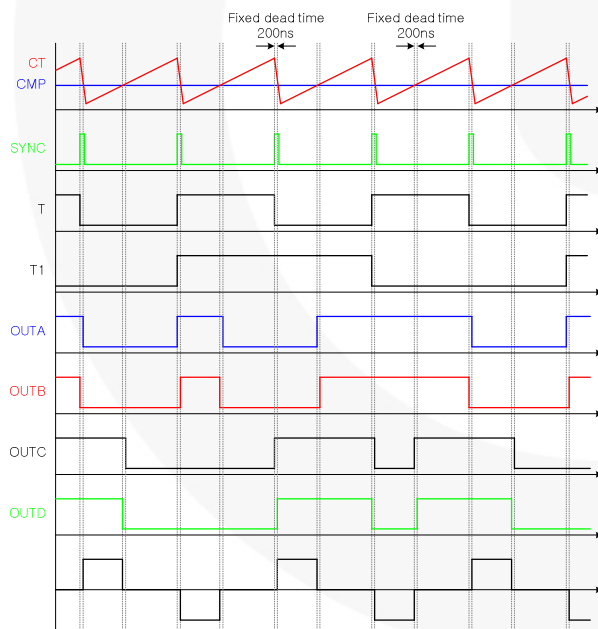
**Figure 44. Burst Dimming Using an External Pulse**

During striking mode, burst dimming operation is disabled to guarantee continuous striking time. Figure 45 shows burst dimming is disabled during striking mode.



**Figure 45. Burst Dimming During Striking Mode**

**Output Drives:** FAN7317 uses the new phase-shift method for full-bridge Cold Cathode Fluorescent Lighting (CCFL) drive. As a result, the temperature difference between the left and the right leg is almost zero, because ZVS occurs in both of the legs by turns. The detail timing is shown in Figure 46.

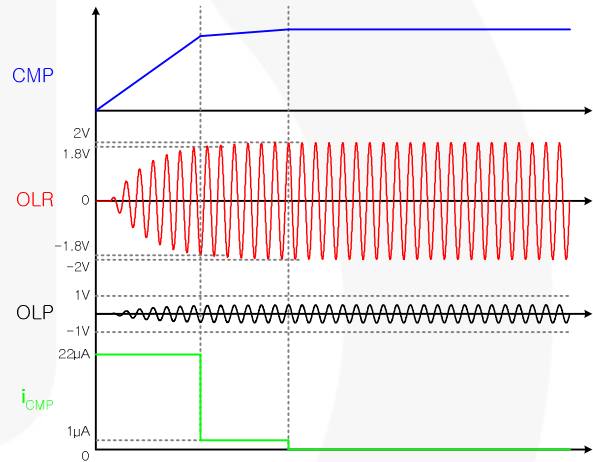


**Figure 46. MOSFETs Gate Drive Signal**

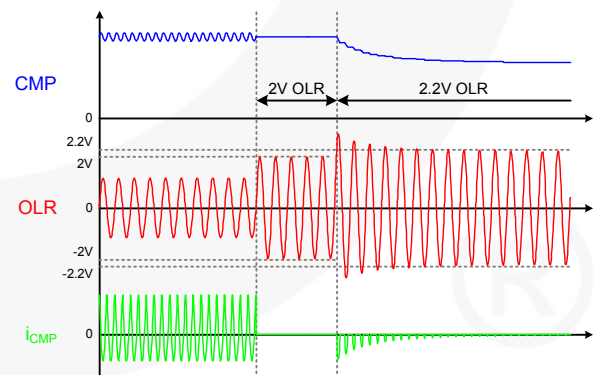
**Protections:** The FAN7317 provides the following latch-mode protections: Open-Lamp Regulation (OLR), Arc Protection, Open-Lamp Protection (OLP), Short-Lamp Protection (SLP), CMP-High Protection, and Thermal Shutdown (TSD). The latch is reset when  $V_{IN}$  falls to the UVLO voltage or ENA is pulled down to GND.

**Open-Lamp Regulation:** When the maximum of the rectified OLR input voltages ( $V_{OLR}^{max}$ ) is more than 2V, the IC enters regulation mode and controls CMP voltage. The IC limits the lamp voltage by decreasing CMP source current. If  $V_{OLR}^{max}$  is between 1.8V and 2V, CMP source current decreases from 22 $\mu$ A to 1 $\mu$ A. Then, if  $V_{OLR}^{max}$  reaches 2V, CMP source current decreases to 0 $\mu$ A, so CMP voltage remains constant and the lamp voltage also remains constant, as shown in Figure 47. Finally, if  $V_{OLR}^{max}$  is more than 2.2V, the error amplifier for OLR is operating and CMP sink current increases, so CMP voltage decreases and the lamp voltage maintains the determined value.

At the same time, while  $V_{OLR}^{max}$  is more than 2V, the counter starts counting 32 rectified OLR pulses in normal mode, then the IC enters shutdown, as shown in Figure 49. This counter is reset by detecting the positive edge of BCT. This protection is disabled in striking mode to ignite lamps reliably.



**Figure 47. Open-Lamp Regulation in Striking Mode**



**Figure 48. Open-Lamp Regulation in Normal Mode**

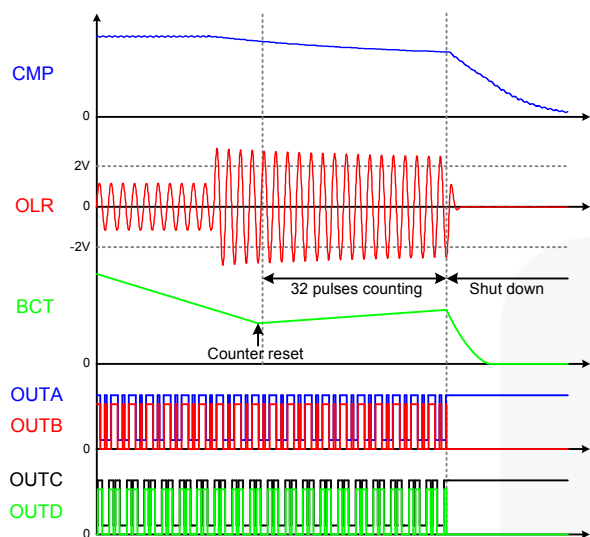


Figure 49. Over-Voltage Protection in Normal Mode

**Arc Protection:** If the maximum of the rectified OLR input voltages ( $V_{OLR}^{\max}$ ) is higher than 3V, the IC enters shutdown mode without delay, as shown in Figure 50.

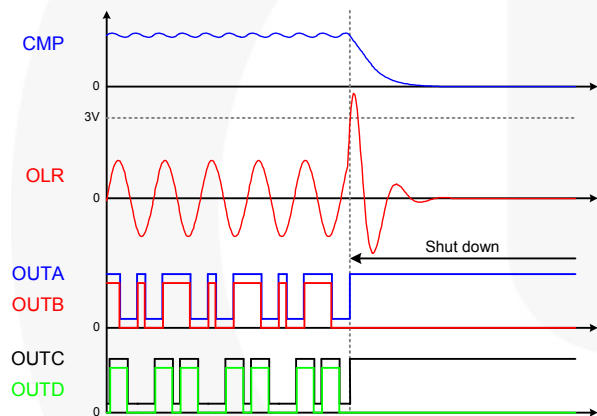


Figure 50. Arc Protection

**Open-Lamp Protection:** If the minimum of the rectified OLP voltages ( $V_{OLP}^{\min}$ ) is less than 1V during initial operation, the IC operates in striking mode only for 1.6s, as shown in Figure 51. After ignition, if  $V_{OLP}^{\min}$  is less than 0.5V in normal mode, the IC is shut down after a delay of 10ms, as shown in Figure 52.

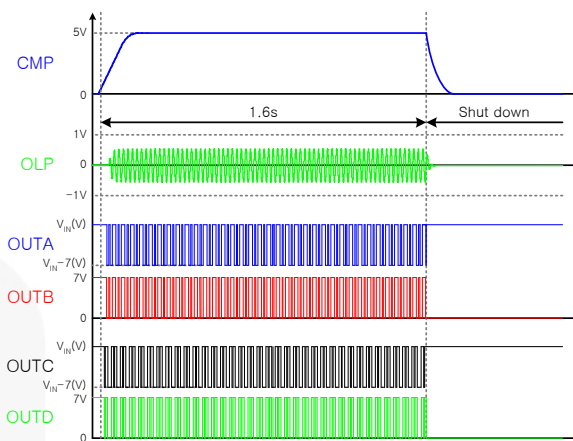


Figure 51. Open-Lamp Protection in Striking Mode

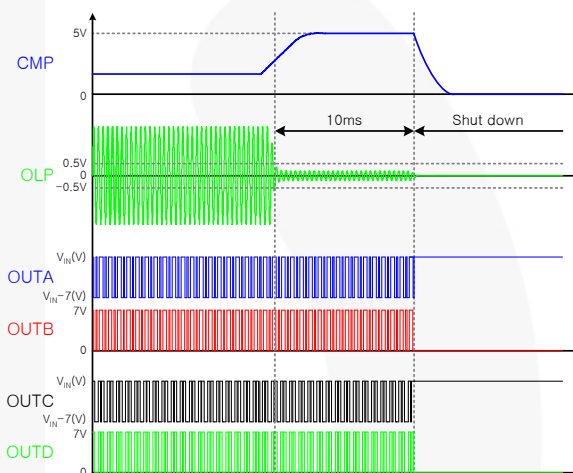


Figure 52. Open-Lamp Protection in Normal Mode

**Short-Lamp Protection:** If the minimum of the rectified OLR voltages ( $V_{OLR}^{\min}$ ) is less than 0.3V in normal mode, the IC is shut down after a delay of 1ms, as shown in Figure 53. This protection is disabled in striking mode to ignite lamps reliably.

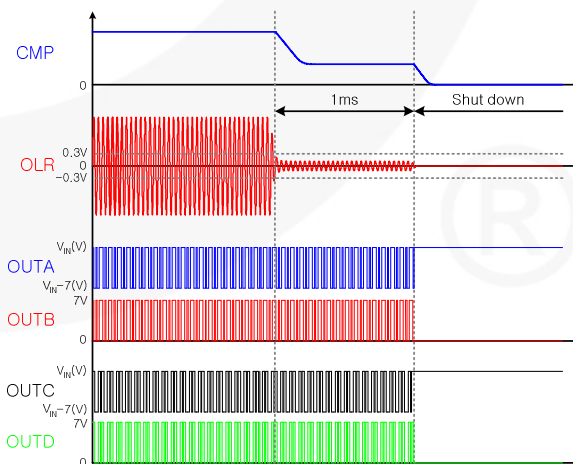


Figure 53. Short-Lamp Protection

**CMP-High Protection:** If CMP is more than 3V in normal mode, the IC is shut down after a delay of 10ms, as shown in Figure 54. This protection is disabled in striking mode to ignite lamps reliably.

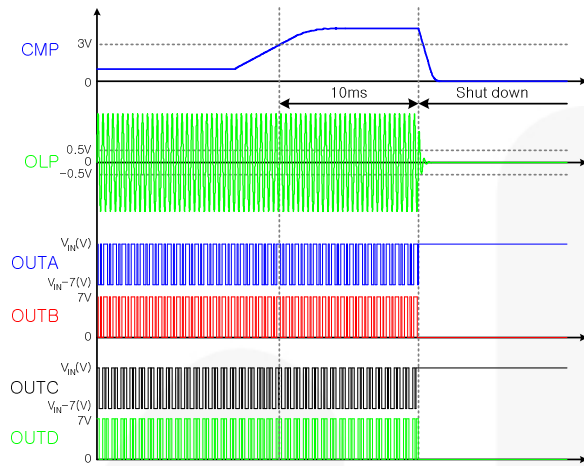


Figure 54. CMP-High Protection

**High-FB Protection:** If the minimum of the rectified OLP voltages(  $V_{OLP}^{max}$  ) is more than 3.5V, the counter starts counting eight rectified OLP pulses in normal mode, then the IC enters shutdown, as shown in Figure 55. This counter is reset by detecting the positive edge of BCT. This protection is disabled in striking mode to ignite lamps reliably.

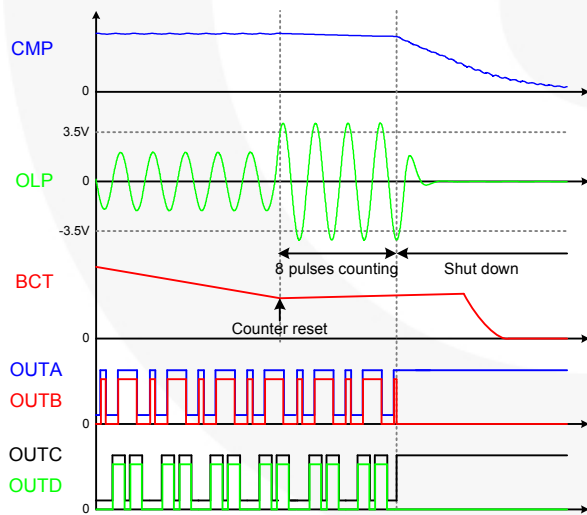


Figure 55. High-FB Protection

**Thermal Shutdown:** The IC provides the function to detect the abnormal over-temperature. If the IC temperature exceeds approximately 150°C, the thermal shutdown triggers.

## Typical Application Circuit (LCD Backlight Inverter)

Application	Device	Input Voltage Range	Number of lamps
22-Inch LCD Monitor	FAN7317	13±10%	4

### 1. Features

- High-Efficiency Single-Stage Power Conversion
- P-N Full-Bridge Topology
- Reduces Required External Components
- Enhanced System Reliability through Protection Functions

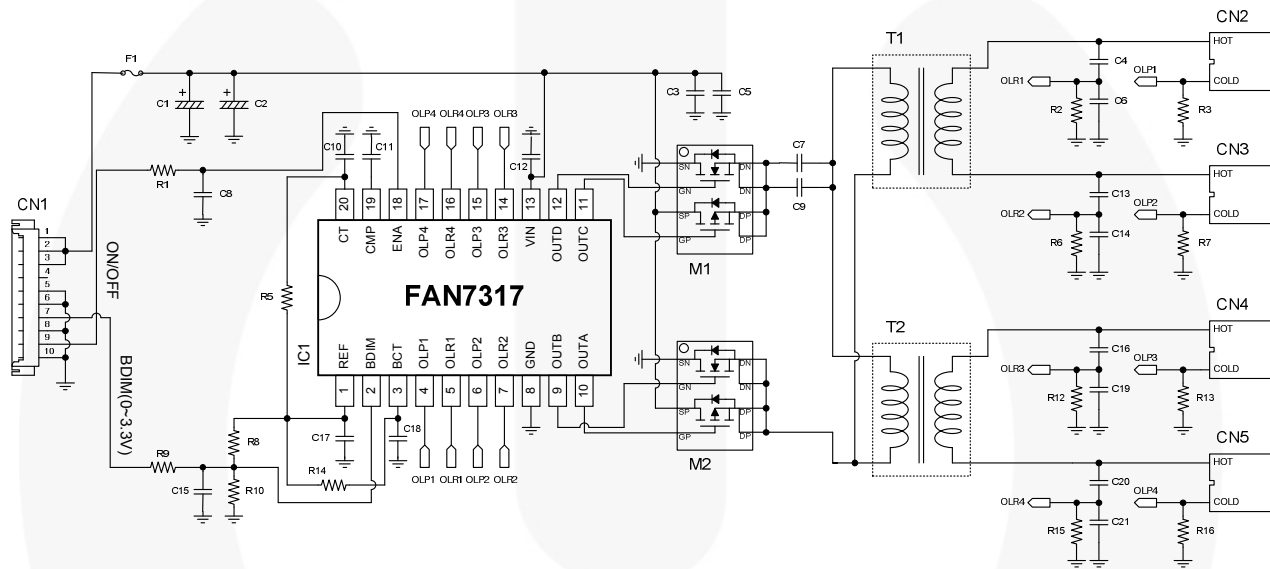


Figure 56. Typical Application Circuit

### 2. Transformer Schematic Diagram

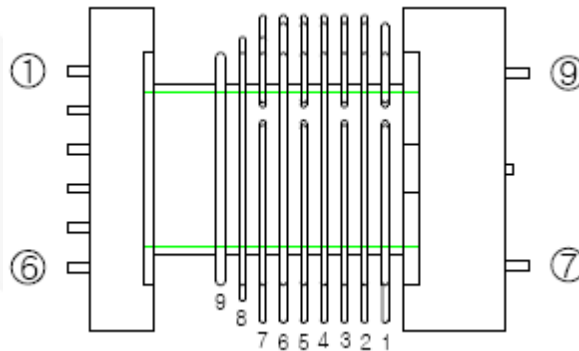


Figure 57. Transformer Schematic Diagram

### 3. Core & Bobbin

- Core: EFD2126
- Material: PL7
- Bobbin: EFD2126

#### 4. Winding Specification

Pin No.	Wire	Turns	Inductance	Leakage Inductance	Remarks
5 → 2	1 UEW 0.4φ	17	250μH	16μH	1kHz, 1V
7 → 9	1 UEW 0.04φ	2256( = 0+0+376•6)	4.2H	290mH	1kHz, 1V

#### 5. BOM of the Application Circuit





Part Ref.	Value	Description	Part Ref.	Value	Description
<b>Fuse</b>			C14	3.3n	50V 1608 K
F1	24V 3A	FUSE	C15	100n	50V 1608 K
<b>Resistor (SMD)</b>			C17	1μ	50V 2012 K
R1	10k	1608 J	C18	4.7n	50V 1608 K
R2	10k	1608 J	C19	3.3n	50V 1608 K
R3	200	1608 F	C21	3.3n	50V 1608 K
R5	100k	1608 F	<b>Capacitor (DIP)</b>		
R6	10k	1608 J	C4	3p	3KV
R7	200	1608 F	C13	3p	3KV
R8	75k	1608 J	C16	3p	3KV
R9	10k	1608 J	C20	3p	3KV
R10	8.2k	1608 J	<b>Electrolytic capacitor</b>		
R12	10k	1608 J	C1	220μ	25V
R13	200	1608 F	C2	220μ	25V
R14	1.5M	1608 F	<b>MOSFET (SMD)</b>		
R15	10k	1608 J	M1	FDD8424H	Fairchild Semiconductor
R16	200	1608 F	M2	FDD8424H	Fairchild Semiconductor
<b>Capacitor (SMD)</b>			<b>Wafer (SMD)</b>		
C3	1μ	50V 2012 K	CN1	12505WR-10	
C5	1μ	50V 2012 K	CN2	35001WR-02A	
C6	3.3n	50V 1608 K	CN3	35001WR-02A	
C7	10μ	16V 3216	CN4	35001WR-02A	
C8	10n	50V 1608 K	CN5	35001WR-02A	
C9	10μ	16V 3216	<b>Transformer (DIP)</b>		
C10	220p	50V 1608 K	TX1		EFD2126
C11	10n	50V 1608 K	TX2		EFD2126
C12	1μ	50V 2012 K			





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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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