1. DESCRIPTION

The XD754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V. The device is designed to drive inductive loads such as relays,solenoids, DC and bipolar stepping motors, as well as other high-current/high-voltage loads in positive- supply applications.

All inputs are compatible with TTL-and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source.Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers and their outputs are off and in a high- impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage V_{CC2} is used for the output circuits.

2. FEATURES

- 1-A Output-Current Capability Per Driver

- Applications Include Half-H and Full-H Solenoid Drivers and Motor Drivers

- Designed for Positive-Supply Applications

- Wide Supply-Voltage Range of 4.5 V to 36 V

- TTL- and CMOS-Compatible High-Impedance Diode-Clamped Inputs

- Separate Input-Logic Supply

- Thermal Shutdown

- Internal ESD Protection

- Input Hysteresis Improves Noise Immunity

- 3-State Outputs

- Minimized Power Dissipation

- Sink/Source Interlock Circuitry Prevents Simultaneous Conduction

- No Output Glitch During Power Up or Power Down
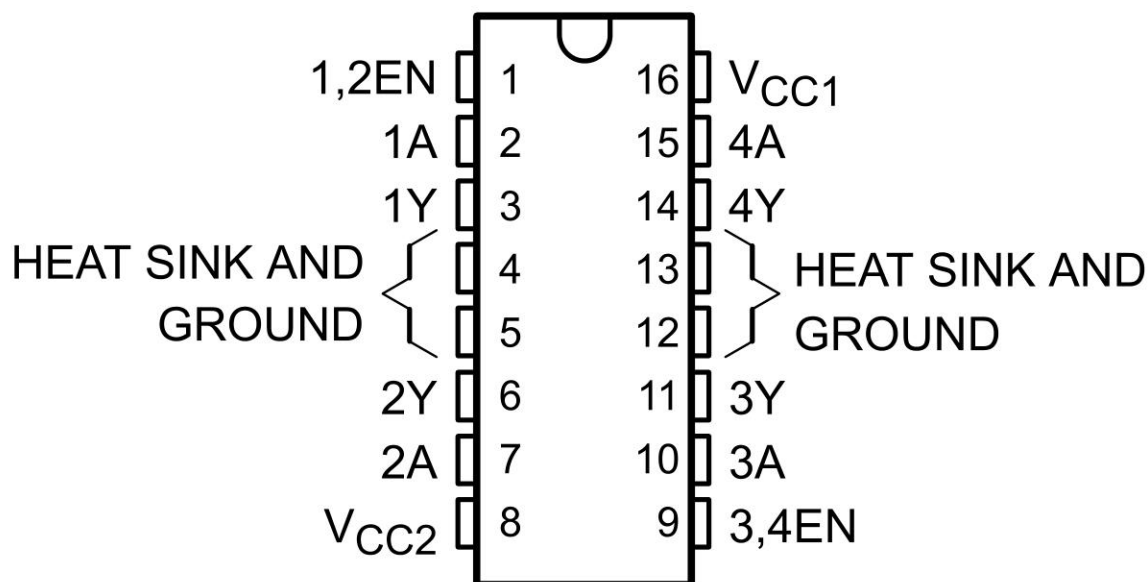
3. APPLICATIONS

- Stepper Motor Drivers

- DC Motor Drivers

- Latching Relay Drivers

4. SIMPLIFIED SCHEMATIC
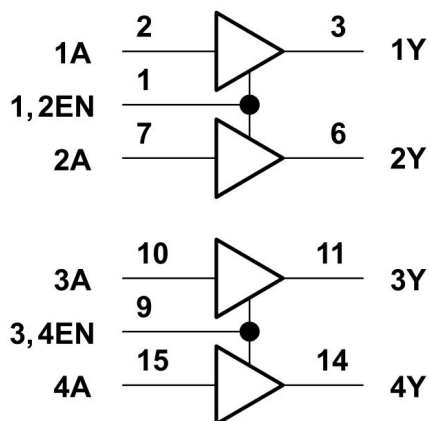
5. PIN CONFIGURATION AND FUNCTIONS

(TOP VIEW)

PIN		TYPE	DESCRIPTION
NAME	NO.		
1,2EN	1	I	Enable driver channels 1 and 2 (active high input)
<1:4>A	2, 7, 10, 15	I	Driver inputs, non-inverting
<1:4>Y	3, 6, 11, 14	O	Driver outputs
GROUND	4, 5, 12, 13	—	Device ground and heat sink pin. Connect to circuit board ground plane with multiple solid vias
V_{CC2}	8	—	Power VCC for drivers 4.5V to 36V
3,4EN	9	I	Enable driver channels 3 and 4 (active high input)
V_{CC1}	16	—	5V supply for internal logic translation

6. SPECIFICATIONS

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2]

		MIN	MAX	UNIT
V_{CC1}	Output supply voltage range	−0.5	36	V
V_{CC2}	Output supply voltage range	−0.5	36	V
V_I	Input voltage	−0.5	36	V
V_O	Output voltage range	−3	V_{CC2} + 3	V
I_P	Peak output current		±2	A
I_O	Continuous output current		±1	A
P_D	Continuous total power dissipation at (or below) 25°C free-air temperature[3]		2075	mW
T_A	Operating free-air temperature range	−40	85	°C
T_J	Operating virtual junction temperature range	−40	150	°C
T_{stg}	Storage temperature range		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network GND.

(3) For operation above 25°C free-air temperature, derate linearly at the rate of 16.6 mW/°C. To avoid exceeding the design maximum virtual junction temperature, these ratings should not be exceeded. Due to variations in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection can be activated at power levels slightly above or below the rated dissipation.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC1}	Logic supply voltage	4.5	5.5	V
V_{CC2}	Output supply voltage	4.5	36	V
V_{IH}	High-level input voltage	2	5.5	V
V_{IL}	Low-level input voltage	−0.3[1]	0.8	V
T_J	Operating virtual junction temperature	−40	85	°C
T_A	Operating free-air temperature	−40	85	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for logic voltage levels.

6.3 Thermal Information

THERMAL METRIC[1]		XD754410	UNIT
		NE	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.

6.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IK}	Input clamp voltage	$I_I = -12$ mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	$I_{OH} = -0.5$ A		$V_{CC2} - 1.5$	$V_{CC2} - 1.1$		V
		$I_{OH} = -1$ A			$V_{CC2} - 2$		
		$I_{OH} = -1$ A, $T_J = 25°C$		$V_{CC2} - 1.8$	$V_{CC2} - 1.4$		
V_{OL}	Low-level output voltage	$I_{OL} = 0.5$ A			1	1.4	V
		$I_{OL} = 1$ A				2	
		$I_{OL} = 1$ A, $T_J = 25°C$			1.2	1.8	
V_{OKH}	High-level output clamp voltage	$I_{OK} = -0.5$ A			$V_{CC2} + 1.4$	$V_{CC2} + 2$	V
		$I_{OK} = 1$ A			$V_{CC2} + 1.9$	$V_{CC2} + 2.5$	
V_{OKL}	Low-level output clamp voltage	$I_{OK} = 0.5$ A			−1.1	−2	V
		$I_{OK} = -1$ A			−1.3	−2.5	
$I_{OZ(off)}$	Off-state high-impedance-state output current	$V_O = V_{CC2}$				500	µA
		$V_O = 0$				−500	
I_{IH}	High-level input current	$V_I = 5.5$ V				10	µA
I_{IL}	Low-level input current	$V_I = 0$				−10	µA
I_{CC1}	Output supply current	$I_O = 0$	All outputs at high level			38	mA
			All outputs at low level			70	
			all outputs at high impedance			25	
I_{CC2}	Output supply current	$I_O = 0$	All outputs at high level			33	nA
			All outputs at low level			20	
			All outputs at high impedance			5	

6.5 Switching Characteristics

over operating free-air temperature range (unless otherwise noted), $V_{CC1} = 5$ V, $V_{CC2} = 24$ V, $C_L = 30$ pF, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{d1}	Delay time, high-to-low-level output from A input	See Figure 3		400		ns
t_{d2}	Delay time, low-to-high-level output from A input			800		ns
t_{TLH}	Transition time, low-to-high-level output			300		ns
t_{THL}	Transition time, high-to-low-level output			300		ns
t_{en1}	Enable time to the high level	See Figure 4		700		ns
t_{en2}	Enable time to the low level			400		ns
t_{dis1}	Disable time from the high level			900		ns
t_{dis2}	Disable time from the low level			600		ns

6.5 Typical Characteristics

$V_{CC1} = 5$ V, $V_{CC2} = 24$ V

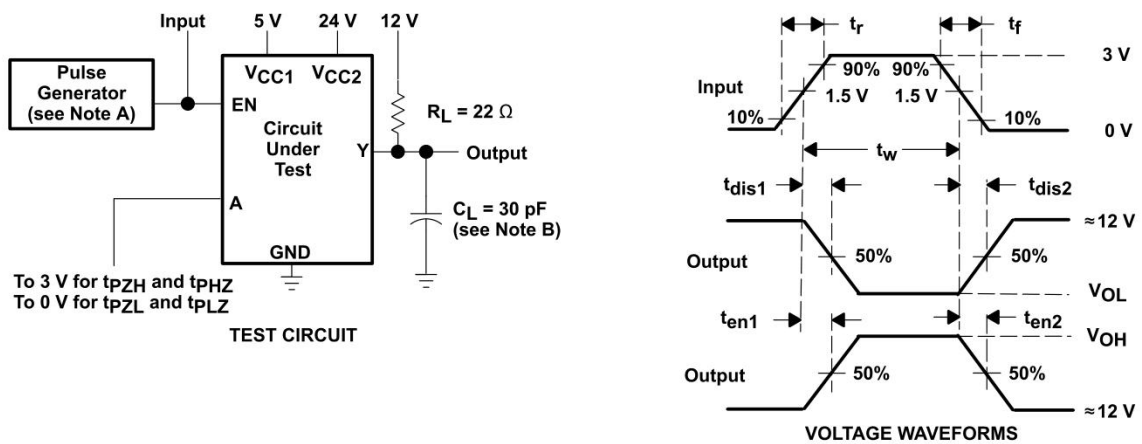Figure 1. V_{OH} vs I_{OH}

Figure 2. V_{OL} vs I_{OL}
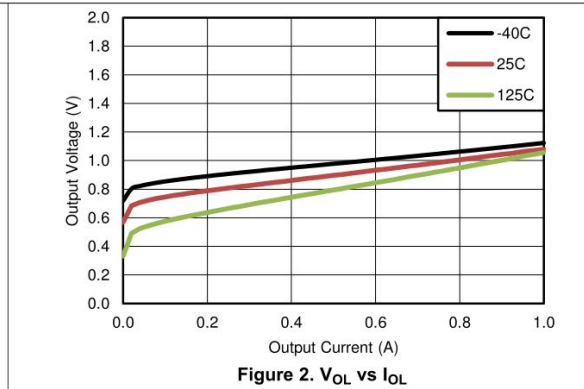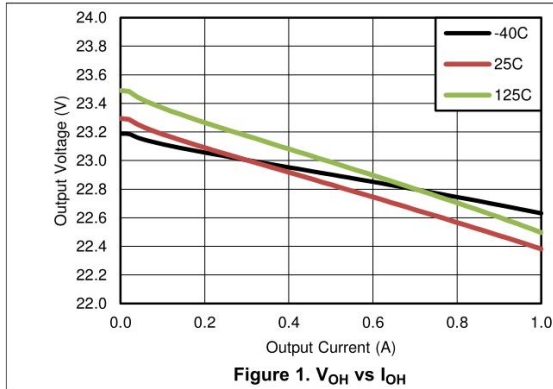
7. PARAMETER MEASUREMENT INFORMATION
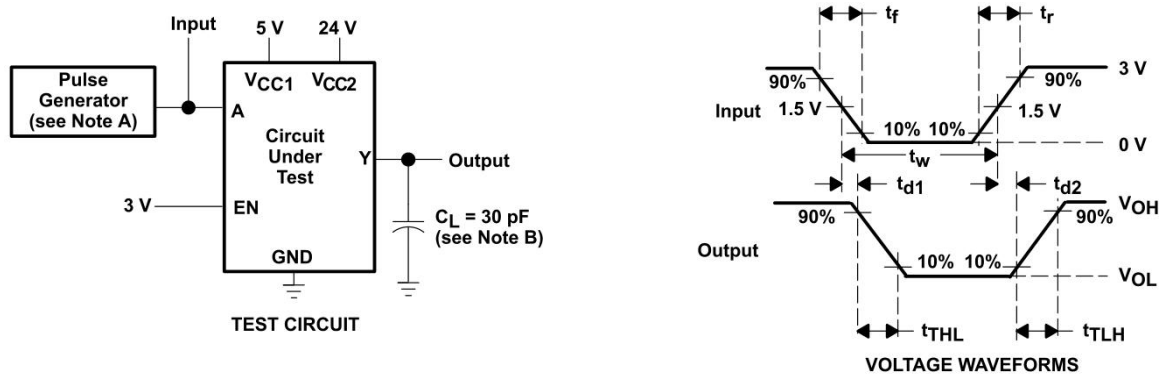
A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ μs, $P_{RR} = 5$ kHz, $Z_O = 50$ Ω
B. C_L includes probe and jig capacitance.

Figure 3. Test Circuit and Switching Times from Data Inputs

A. The pulse generator has the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, $t_w = 10$ μs, $P_{RR} = 5$ kHz, $Z_O = 50$ Ω
B. C_L includes probe and jig capacitance.

**Figure 4. Test Circuit and Switching Times from Enable Inputs**

8. DETAILED DESCRIPTION

8.1 Overview

The XD754410 is a quadruple high-current half-H driver designed to provide bidirectional drive currents up to 1 A at voltages from 4.5 V to 36 V. The device is designed to drive inductive loads such as relays, solenoids, DC and bipolar stepping motors, as well as other high-current/high-voltage loads in positive-supply applications. All inputs are compatible with TTL and low-level CMOS logic. Each output (Y) is a complete totem-pole driver with a Darlington transistor sink and a pseudo-Darlington source. Drivers are enabled in pairs with drivers 1 and 2 enabled by 1,2EN and drivers 3 and 4 enabled by 3,4EN. When an enable input is high, the associated drivers are enabled and their outputs become active and in phase with their inputs. When the enable input is low, those drivers are disabled and their outputs are off and in a high-impedance state. With the proper data inputs, each pair of drivers form a full-H (or bridge) reversible drive suitable for solenoid or motor applications.

A separate supply voltage (V_{CC1}) is provided for the logic input circuits to minimize device power dissipation. Supply voltage V_{CC2} is used for the output circuits. The XD754410 is designed for operation from −40°C to 85°C.

8.2 Functional Block Diagram
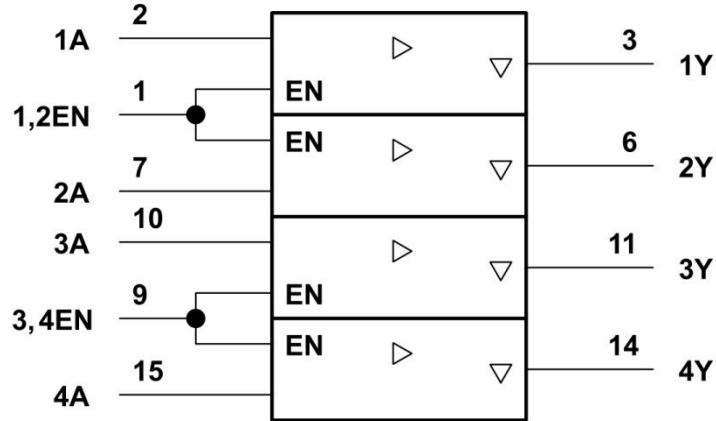
8.3 Feature Description

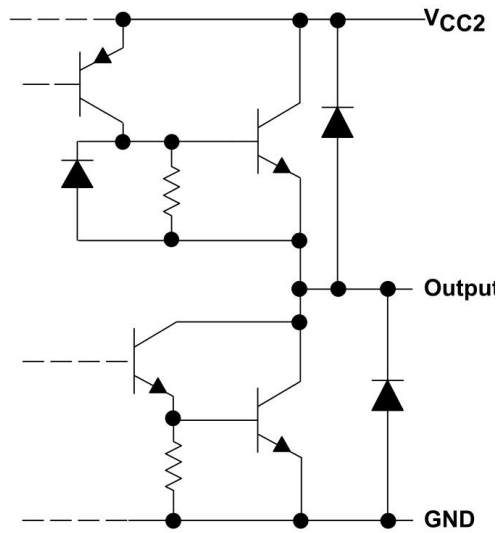### 8.3.1 High Current,High Voltage Outputs

Figure 5. Typical of All Outputs

8.3.2 TTL Compatible Inputs

Data inputs and enable inputs are compatible with TTL. 3.3-V CMOS logic is also acceptable, however open or high impedance input voltage can approach V_{CC1} voltage.
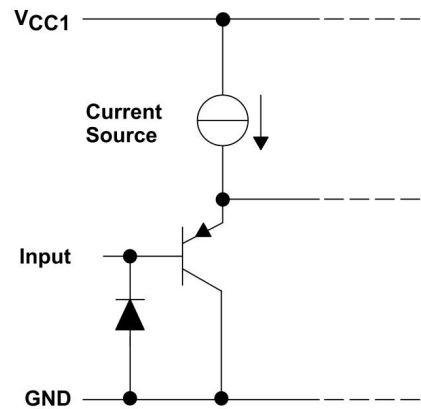

Figure 6. Equivalent of Each Input

8.4 Device Functional Modes

Table 1. Function Table[1]

INPUTS[2]		OUTPUTS Y
A	EN	
H	H	H
L	H	L
X	L	Z

(1)   H = high-level

L = low-level

X = irrelevant

Z = high-impedance (off)

(2)   In the thermal shutdown mode, the output is in a high-impedance state regardless of the input levels.

9. APPLICATION AND IMPLEMENTATION

NOTE
Information in the following applications sections is not part of the XINLUDA component specification, and XINLUDA does not warrant its accuracy or completeness. XINLUDA's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Provide a 5-V supply to V_{CC1} and valid logic input levels to data and enable inputs. V_{CC2} must be connected to a power supply capable of suppling the needed current and voltage demand for the loads connected to the outputs.
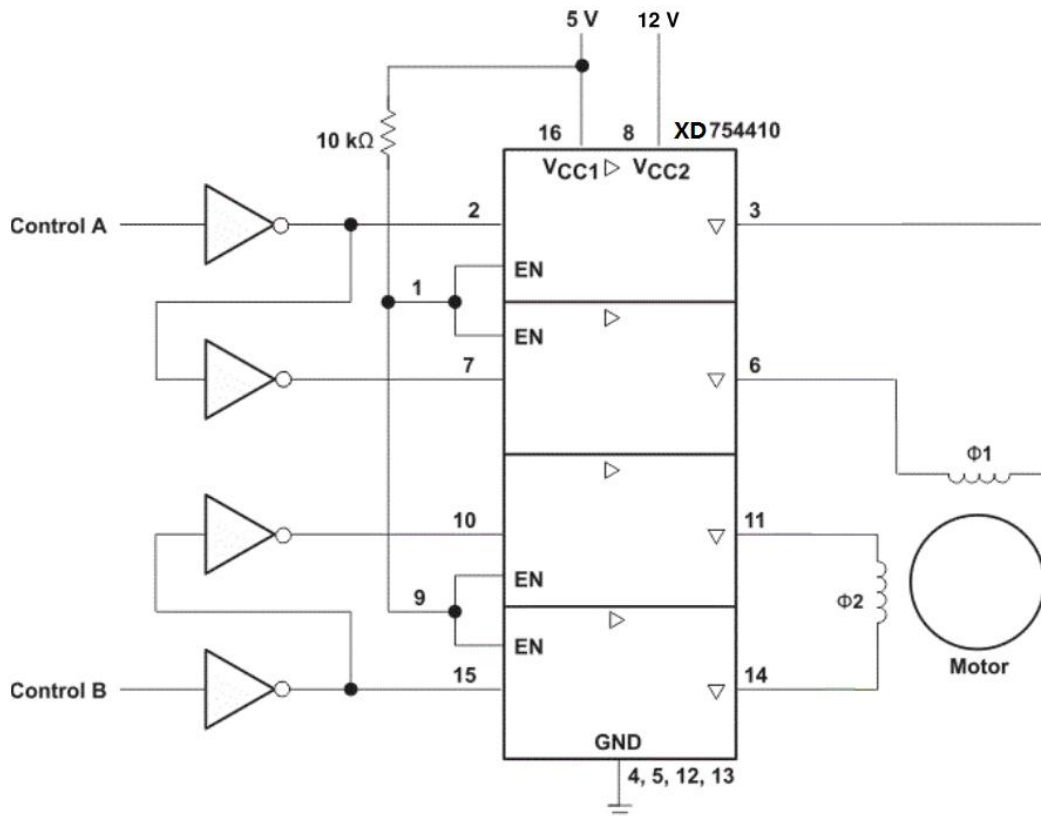
9.2 Typical Application

Figure 7. Typical Application Schematic

9.2.1 Design Requirements

The design techniques in the following sections may be used for applications which fall within the following requirements.

- 4.5-V minimum and 36-V maximum V_{CC2} voltage
- 1000-mA or less output current per channel
- 5-V supply with 10% tolerance or less
- TTL compatible logic inputs

Typical Application (continued)

10.2.2 Design Requirements

Driver output voltage waveform with a two phase stepper motor; 12-V 20-Ω coils.
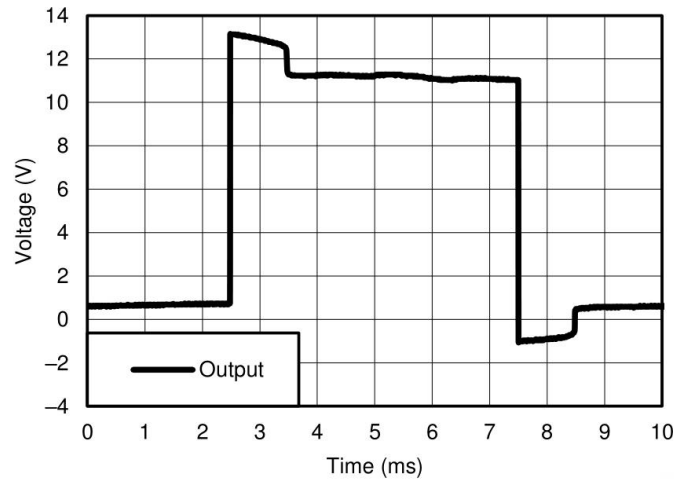

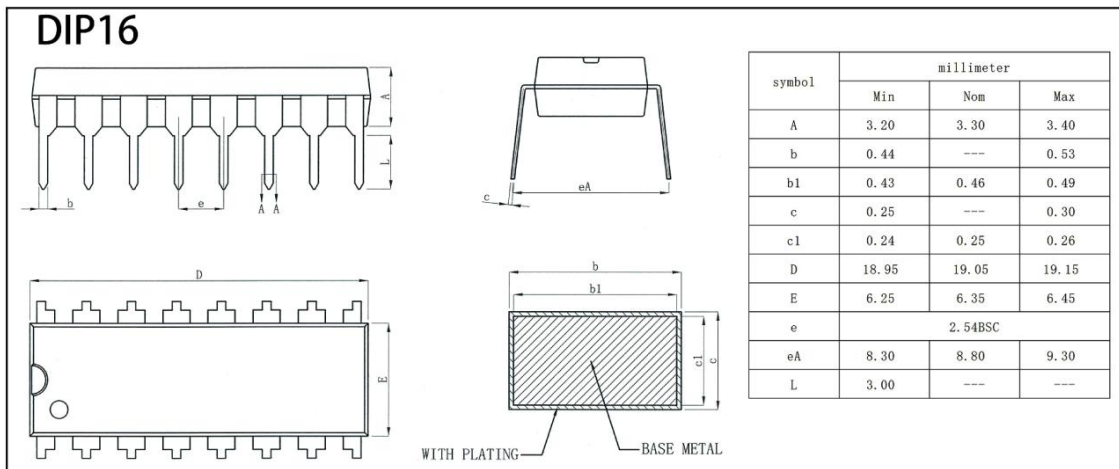**Figure 8. 100 Hz Driver Output Waveform**

10.   POWER SUPPLY RECOMMENDATIONS

V_{CC1} is 5 V ± 0.5 V and V_{CC2} can be same supply as V_{CC1} or a higher voltage supply with peak voltage up to 36 V. Bypass capacitors of 0.1 uF or greater should be used at V_{CC1} and V_{CC2} pins. There are no power up or power down supply sequence order requirements.

11. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD754410	XD754410	DIP16	19.05 ∗ 6.35	- 40 to 85	MSL3	Tube 25	1000

12. DIMENSIONAL DRAWINGS

symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---

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