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May 2015

FAN6230A
Secondary-Side Synchronous Rectification Controller for Flyback Converters

Features

- Secondary-Side SR Controller for Flyback
- Seamless Transition between DCM and CCM
- Shunt Regulator Integrated (1.25 V Reference)
- Charge Pump Circuit Integrated for Low Output Voltage in CC Mode
- Output Cable Compensation Circuit Integrated
- PWM Frequency Tracking using Secondary side Winding Voltage
- Ultra Low V_{DD} Operating Voltage for 5 V, 9 V, 12 V Output Application
- Ultra Low Green Mode Operating Current (Typical: 0.5 mA)
- Boost Entire Efficiency and Green-Mode Operation for Less Power Consumption at No Load Condition
- 16-Pin MLP33 Package
- RES Dropping Protection (Enter Green Mode)
- LPC Falling Detect Protection (Disable Gate Drive)
- Causal Period Protection (Disable Gate Drive)

Description

The FAN6230A is a secondary-side synchronous rectifier (SR) MOSFET controller for high efficiency applications. It has internal shunt regulator with low bias current and internal charge pump circuit to reduce external part counts, total cost and overall system power consumption. With the internal charge pump circuit, the FAN6230A guarantees stable operation of SR switching even with low bias voltage in CC regulation. The FAN6230A also features internally adjustable cable compensation that helps maintain precise constant voltage regulations at the end of cable.

Unlike the traditional SR current sensing methods, which measure the SR MOSFET drain voltage that is sensitive to the noise introduced by poor PCB layout. The FAN6230A utilizes a novel Linear-Prediction Timing Control (LPC) circuit to estimate the SR current zero crossing instant without additional current sensing circuitry.

While running in Green Mode, the FAN6230A shuts off the SR MOSFET and lowers its bias supply current to 500 μA, so overall power consumption of the system is further reduced.

Applications

- Adaptive chargers for cellular phones, cordless phones, tablets, PDAs, digital cameras, and power tools.

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6230AMPX	-40°C to +125°C	16-Lead, Molded Leadless Package, (MLP) QUAD. JEDEC MO-220, 3 x 3	Tape & Reel

Application Diagram

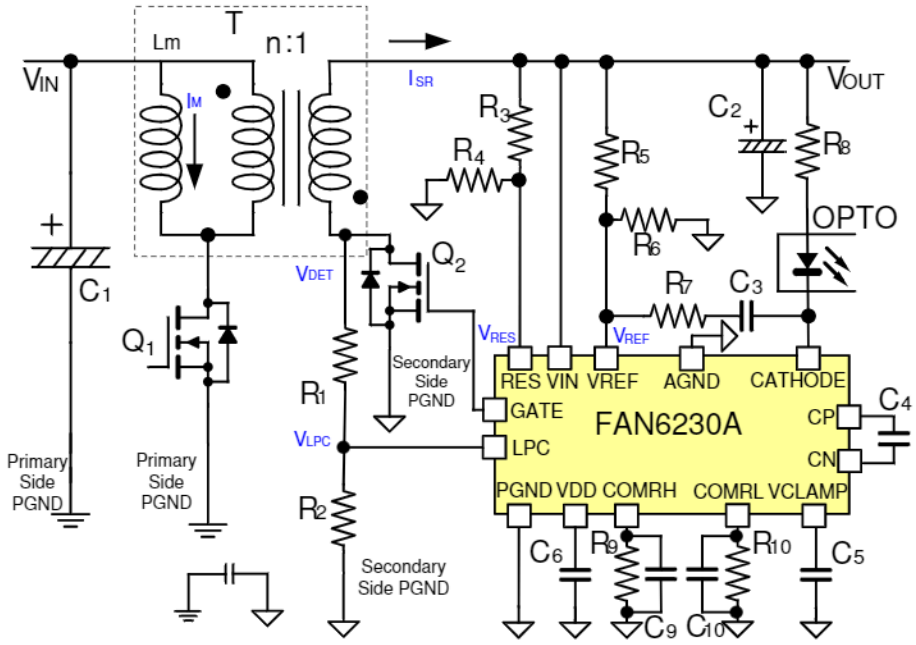


Figure 1. Typical Application Circuit

Internal Block Diagram

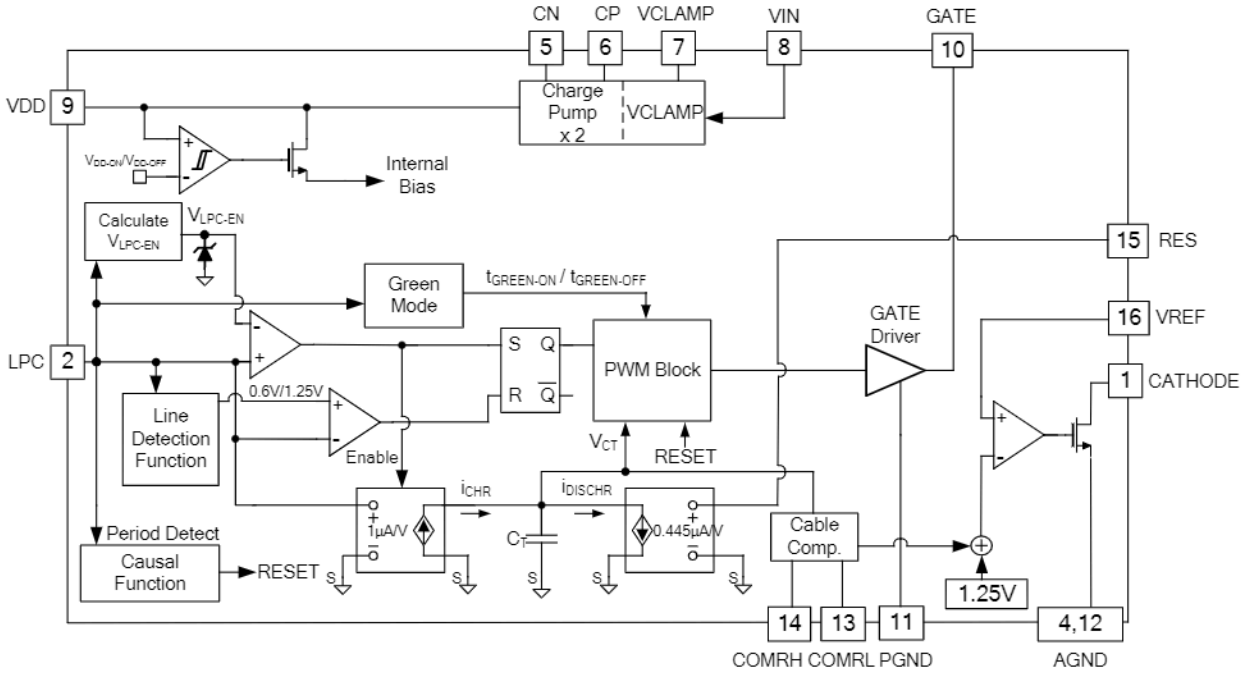
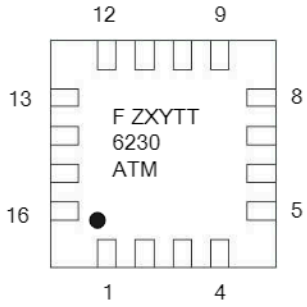


Figure 2. Functional Block Diagram

Marking Information



F: Fairchild Logo
Z: Plant Code
X: Year Code
Y: Week Code
TT: Die Run Code
T: Package Type (MP=MLP)
M: Manufacture Flow Code

Figure 3. Top Marking Information

Pin Configuration

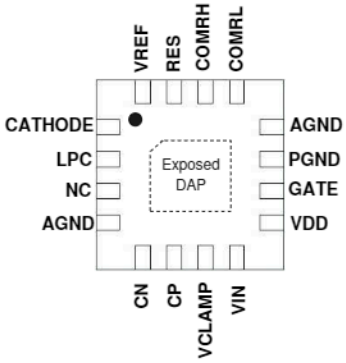


Figure 4. Pin Assignments

Pin Definitions

Pin #	Name	Description
1	CATHODE	Cathode of internal shunt regulator (open drain)
2	LPC	SR MOSFET Drain Voltage Detection. This pin is used to detect the voltage on the secondary winding during the on time period of the primary FET
3	NC	Not Connected. It is recommended to solder to PCB
4	AGND	Analog Ground
5	CN	Charge Pump CN
6	CP	Charge Pump CP
7	VCLAMP	Clamp Voltage on VIN Voltage. The clamped voltage is fed to the charge pump circuit. Need 1 µF ceramic bypass capacitor to PGND
8	VIN	Input voltage for the charge pump, typically connected to the output voltage of the power converter.
9	VDD	SR gate driver voltage source and bias supply for internal control circuitry.
10	GATE	Gate Driver Output. Totem-pole output to drive the external SR MOSFET.
11	PGND	Power Ground
12	AGND	Analog Ground
13	COMRL	Input for internal cable compensation circuit. Tie a resistor from this pin to AGND to program the cable compensation function for low line operation
14	COMRH	Input for internal cable compensation circuit. Tie a resistor from this pin to AGND to program cable compensation function for high line operation
15	RES	Reset Control of the Linear Predict circuit. An internal current source, IDISCHR is modulated by the voltage level on the RES pin.
16	VREF	Reference for the internal shunt regulator.
Exposed DAP	Analog Ground	Must be soldered to PCB ground plane

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	Charge Pump Supply Voltage			20	V
$V_{CATHODE}$	CATHODE Pin Input Voltage			20	V
V_{VDD}	VDD Pin Input Voltage		-0.3	6.5	V
V_{VREF}	VREF Pin Input Voltage		-0.3	7.0	V
V_{RES}	RES Pin Input Voltage		-0.3	7.0	V
V_{LPC}	LPC Pin Input Voltage		-0.3	7.0	V
V_{COMRH}	COMRH Pin Input Voltage		-0.3	6.5	V
V_{COMRL}	COMRL Pin Input Voltage		-0.3	6.5	V
V_{GATE}	GATE Pin Input Voltage		-0.3	6.5	V
V_{CP}	CP Pin Input Voltage		-0.3	6.5	V
V_{CN}	CN Pin Input Voltage		-0.3	6.5	V
V_{VCLAMP}	VCLAMP Pin Input Voltage		-0.3	6.5	V
P_D	Power Dissipation (T_A=25°C)			0.85	W
Θ_{JA}	Thermal Resistance (Junction-to-Ambient Thermal)			147	°C/W
Ψ_{Jt}	Thermal Resistance (Junction-to-Top Thermal)			12	°C/W
T_J	Operating Junction Temperature		-40	150	°C
T_{STG}	Storage Temperature Range		-40	150	°C
T_L	Lead Temperature (Soldering) 10 Seconds			260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI / ESDA / JEDEC JS-001-2012		2.5	kV
		Charged Device Model, JESD22-C101		1.5	

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
2. All voltage values, except differential voltages, are given with respect to AGND pin, (AGND=PGND).

Electrical Characteristics

V_{IN}=5 V~12 V, LPC=1.5 V, LPC width=2 μs, RES=1.5 V, T_J=-40°C to 105°C, f_{LPC}=100 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VIN Section (Charge Pump)						
V_{IN}	V_{IN} Continuously Operating Voltage		1.9		16	V
I_{IN-OP}	Operating Current at 5 V_{IN}	V_{IN}=5 V, C_{VCLAMP}=C_{PN}=C_{VDD}=1 μF, f_{LPC}=140 kHz,C_L=3300 pF (Including Charge Pump)		12	16	mA
$I_{IN-OP-12V}$	Operating Current at 12 V_{IN}	V_{IN}=12 V, C_{VCLAMP}=C_{PN}=C_{VDD}=1 μF, f_{LPC}=140 kHz,C_L=3300 pF (No Charge Pump)		6	8	mA
$I_{IN-GREEN}$	Operating Current in Green Mode	V_{IN}=5 V, C_{VCLAMP}=C_{PN}=C_{VDD}=1 μF		500	700	μA
V_{OD}	Output Voltage for Internal V_{DD} Supply	C_{VCLAMP}=C_{PN}=C_{VDD}=1 μF, V_{IN}>2.5 V, f_{LPC}=140 kHz, C_L=3300 pF, 1.9<V_{IN}<2.5, f_{LPC}=60 kHz, C_L=3300 pF	3.2	5.0	6.2	V
f_S	Switching Frequency of Charge Pump		164	174	184	kHz
V_{IN-CC}	Threshold Voltage of V_{IN} to Enter CC Region		3.8	4.0	4.2	V
V_{IN-CV}	Threshold Voltage of V_{IN} to Enter CV Region		4.2	4.4	4.6	V
VDD Section						
V_{DD-ON}	Turn-On Threshold Voltage[3]	V_{IN}=V_{DD}=2.5 V, C_{VCLAMP}=C_{PN}=C_{VDD}=1 μF, V_{DD} from 2.5 V to 4 V	3.20	3.35	3.50	V
V_{DD-OFF}	Turn-Off Threshold Voltage	V_{IN}=V_{DD}=2.5 V, C_{VCLAMP}=C_{PN}=C_{VDD}=1 μF, V_{DD} from 4 V to 2.5 V	2.85	3.00	3.15	V
V_{DD-HYS}	Hysteresis Voltage for Turn-On / Turn-Off Threshold	V_{DD-HYS}=V_{DD-ON} - V_{DD-OFF}	0.20	0.35	0.50	V
Causal Function Section						
$t_{DEAD-CAUSAL1}$	SR Turn-Off Dead Time by Causal Function at High Line	f_{LPC}=85 kHz, LPC=3 V, LPC Width=5 μs, RES=1.5 V	640	790	940	ns
$t_{DEAD-CAUSAL2}$	SR Turn-Off Dead Time by Causal Function at Low Line	f_{LPC}=140 kHz, LPC=1.5 V, LPC Width=3 μs, RES=1.5 V	420	570	720	ns
$t_{DEAD-CAUSAL3}$	SR Turn-Off Dead Time by Causal Function at CC range	f_{LPC}=140 kHz, LPC=1.5 V, LPC Width=3 μs, RES=1.5 V, V_{IN}=3.5V	650	850	1050	ns
$t_{DEAD-CFR}$	CFR Start to Shrink Timing (The Last Time from SR Gate Falling to LPC Rising)[4]	Causal Function Regulator (CFR)		70	200	ns
$t_{CAUSAL-LINEAR}$	Linear Operation Range of Causal Function		5		30	μs
$K_{CAUSAL-PERIOD}$	Causal Protection Ratio with Two Cycles[4]		120	150	180	%
Output Driver Section						
V_{OL}	Output Voltage Low	V_{IN}=5 V, I_{GATE}=100 mA		0.16	0.25	V
V_{OH}	Output Voltage High	V_{IN}=5 V, I_{GATE}=-100 mA	4.5	4.8		V

Continued on the following page…

Electrical Characteristics

V_{IN}=5 V~12 V, LPC=1.5 V, LPC width=2 μs, RES=1.5 V, T_J=-40°C to 105°C, f_{LPC}=100 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_R	Rise Time[4]	V_{IN}=5 V, C_L=3300 pF, GATE=1 V~4 V		14		ns
t_F	Fall Time[4]	V_{IN}=5 V, C_L=3300 pF, GATE=4 V~1 V		9		ns
$t_{PD-HIGH-LPC}$	Propagation Delay to OUT HIGH (LPC Trigger)[4]	V_{IN}=5 V, GATE=1 V		44	70	ns
$t_{PD-LOW-LPC}$	Propagation Delay to OUT LOW (LPC Trigger)[4]	V_{IN}=5 V, GATE=4 V		16		ns
$t_{INHIBIT}$	Gate Inhibit Time[4]			1.4		μs
$t_{MAX-PERIOD}$	Limitation between LPC Rising Edge to Gate Falling Edge Max. Period		42	47	52	μs
V_{REF} Section (Shunt Regulator)						
V_{REF}	Reference Voltage	$I_{CATHODE}$=5 mA, $V_{CATHODE}$=V_{REF}	1.24	1.25	1.26	V
$V_{REF-CLAMP-H}$	High Clamp Voltage		5.4	6.2	7.0	V
$V_{CATHODE}$	Shunt Regulator Output	V_{REF} > V_{REF-CV} (1.1 V) to Enable CATHODE	V_{DD-OFF}		15	V
$V_{DEV,I}$	Deviation of V_{REF} Over Cathode Current	$I_{CATHODE}$=0.5 mA to 5 mA, V_{REF}=$V_{CATHODE}$	0	10	20	mV
$V_{DEV,T}$	Deviation of V_{REF} Over-Temperature	$I_{CATHODE}$=0.5 mA, V_{REF}=$V_{CATHODE}$	0	15	30	mV
$R_{EGLI-FB}$	Line Regulation	4 < $V_{CATHODE}$ < 14	0	2	4	mV/V
$I_{L-CATHODE}$	Leakage Current	V_{REF}=0 V, $V_{CATHODE}$=6 V	0	1	10	μA
RES Section						
V_{RES-EN}	Threshold Voltage of V_{RES} to Enable SR Gate		0.1	0.2	0.3	V
V_{RES}	Linear Operation Range of RES Pin Voltage[4]	V_{DD-OFF} < V_{DD} ≤ 5 V	0.4		V_{DD}-1.0	V
$V_{RES-CLAMP-H}$	Higher Clamp Voltage		5.4	6.2	7.0	V
$I_{RES-SINK}$	RES Sink Current	V_{RES}=1 V	50	150	250	nA
$K_{RES-DROP}$	RES Dropping Protection Ratio with Two Cycles	LPC width=5 μs, RES=1 V to 0.7 V	70		90	%
LPC Section						
V_{LPC}	Linear Operation Range of LPC Pin Voltage[4]	V_{DD-OFF} < V_{DD} ≤ 5 V	0.5		V_{DD} - 1.0	V
$I_{LPC-SINK}$	LPC Sink Current	V_{LPC}=1 V	50	150	250	nA
$V_{LPC-HIGH-H}$	SR Enabled Threshold Voltage at High-Line[4]		1.4		1.6	V
$V_{LPC-TH-H}$	Threshold Voltage on LPC Rising Edge at High-Line[4]	$V_{LPC-HIGH-H}$ • 0.875=$V_{LPC-TH-H}$		1.25		V
$V_{LPC-HIGH-L-5V}$	SR Enabled Threshold Voltage at Low-Line, V_{IN}= 5 V	$V_{LPC-HIGH-L-5V}$ =$V_{LPC-TH-L-5V}$ / 0.875	0.62	0.68	0.74	V
$V_{LPC-TH-L-5V}$	Threshold Voltage on LPC Rising Edge at Low-Line, V_{IN}= 5 V[4]	Spec.=0.45+0.03 • V_{IN}, V_{IN}=5 V	0.55	0.60	0.65	V

Continued on the following page…

Electrical Characteristics

V_{IN}=5 V~12 V, LPC=1.5 V, LPC width=2 μs, RES=1.5 V, T_J=-40°C to 105°C, f_{LPC}=100 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{LPC-HIGH-L-9V}$	SR Enabled Threshold Voltage at Low-Line, V_{IN}= 9 V	$V_{LPC-HIGH-L-9V}$ =$V_{LPC-TH-L-9V}$ / 0.875	0.81	0.88	0.95	V
$V_{LPC-TH-L-9V}$	Threshold Voltage on LPC Rising Edge at Low-Line, V_{IN}= 9 V (4)	Spec.=0.45+0.03 • V_{IN}, V_{IN}=9 V	0.72	0.77	0.82	V
$V_{LPC-HIGH-L-12V}$	SR Enabled Threshold Voltage at Low-Line, V_{IN}= 12 V	$V_{LPC-HIGH-L-12V}$ =$V_{LPC-TH-L-12V}$ / 0.875	0.95	1.02	1.09	V
$V_{LPC-TH-L-12V}$	Threshold Voltage on LPC Rising Edge at Low-Line, V_{IN}=12 V (4)	Spec.=0.45+0.03 • V_{IN}, V_{IN}=12 V	0.85	0.90	0.95	V
$V_{LPC-TH-TRIG}$	Threshold Voltage on LPC falling Edge at trigger		40	70	100	mV
$V_{LINE-H-5V}$	Low-to High-Line Threshold Voltage on LPC Pin, V_{IN}= 5 V	Spec.=[0.80+0.023 • V_{IN}]*2; V_{IN}=5 V	1.7	1.8	1.9	V
$V_{LINE-L-5V}$	High-to Low-Line Threshold Voltage on LPC Pin, V_{IN}=5 V	Spec.=[0.75+0.023 • V_{IN}]*2; V_{IN} = 5 V	1.6	1.7	1.8	V
$V_{LINE-H-9V}$	Low-to High-Line Threshold Voltage on LPC Pin, V_{IN}=9 V	Spec.=[0.80+0.023 • V_{IN}]*2; V_{IN} = 9 V	1.87	1.97	2.07	V
$V_{LINE-L-9V}$	High-to Low-Line Threshold Voltage on LPC Pin, V_{IN}=9 V	Spec.=[0.75+0.023 • V_{IN}]*2; V_{IN}= 9 V	1.77	1.87	1.97	V
$V_{LINE-H-12V}$	Low-to High-Line Threshold Voltage on LPC Pin, V_{IN}=12 V	Spec.=[0.80+0.023 • V_{IN}]*2; V_I =12 V	1.99	2.09	2.19	V
$V_{LINE-L-12V}$	High-to Low-Line Threshold Voltage on LPC Pin, V_{IN}=12 V	Spec.=[0.75+0.023 • V_{IN}]*2; V_{IN}=12 V	1.89	1.99	2.09	V
$V_{LPC-CLAMP-H}$	Higher Clamp Voltage		5.4	6.2	7.0	V
$V_{LPC-DIS}$	LPC Threshold Voltage to Disable SR Gate Switching	V_{DD}=5 V, LPC=3 V↑	4.50	4.75	5.00	V
$t_{LPC-LH-debounce}$	Line Change Debounce from Low-Line to High-Line		12	18	24	ms
$t_{LPC-HL-debounce}$	Line Change Debounce from High-Line to Low-Line(4)			15		μs
Internal Timing Section						
$Ratio_{LPC}$	LPC Transfer Ratio to I_{LPC}(4)			1		μA/V
$Ratio_{RES}$	V_{RES} Transfer Ratio to I_{RES}(4)			0.445		μA/V
$Ratio_{LPC-RES}$	Ratio between V_{LPC} and V_{RES}	V_{LPC}=1.5 V, V_{RES}=1.5 V, LPC Width=4 μs	2.05	2.25	2.45	
$t_{LPC-EN-H}$	Minimum LPC Time to Enable the SR Gate at High-Line, $V_{LPC-HIGH}$>$V_{LPC-HIGH-H}$	V_{DD} ≥ 5 V, V_{LPC}=3 V, V_{RES}=1.5 V	80	180	280	ns
$t_{LPC-EN-L}$	Minimum LPC Time to Enable the SR Gate at Low-Line, $V_{LPC-HIGH}$>$V_{LPC-HIGH-L}$	V_{DD} ≥ 5 V, V_{LPC}=1.5 V, V_{RES}=1.5 V	600	700	800	ns
t_{MIN}	Minimum Gate Width(4)	V_{LPC}=1.5 V, V_{RES}=1.5 V	0.35	0.50	0.65	μs
$t_{gate-limit}$	$t_{on-SR}(n+1)$- $t_{on-SR}(n)$ < $t_{gate-limit}$			500		ns
GREEN Section						
$t_{GREEN-ON}$	Minimum LPC Non-Switching Period to Enter Green Mode	Each LPC Cluster to Cluster	260	330	400	μs

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Electrical Characteristics

V_{IN}=5 V~12 V, LPC=1.5 V, LPC width=2 μs, RES=1.5 V, T_J=-40°C to 105°C, f_{LPC}=100 kHz; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$t_{GREEN-OFF}$	Maximum LPC Non-Switching Period to Exit Green Mode	Each LPC Cluster to Cluster	100	150	200	μs
$n_{GREEN-OFF}$	Continuous LPC Switching Cycles to Exit Green Mode			256		Cycles
COMR Section						
$V_{DIS-COMR-H}$	Threshold Voltage of COMRH to Disable Cable Compensation	V_{DD}>3.5 V	2.0	2.5	3.0	V
$V_{DIS-COMR-L}$	Threshold Voltage of COMRL to Disable Cable Compensation	V_{DD}>3.5 V	2.0	2.5	3.0	V
$V_{REF-COMRH}$	Cable Compensation at High-Line	R_{COMRH}=100 kΩ, C_{COMRH}=100 nF, V_{DD}=5 V, RES=1.5 V, LPC HIGH=3 V, Gate Width=5 μs, (V_{REF}=$V_{CATHODE}$, $I_{CATHODE}$=5 mA)	1.37	1.40	1.43	V
$V_{REF-COMRL}$	Cable Compensation at Low-Line	R_{COMRL}=100 kΩ, C_{COMRL}=100 nF, V_{DD}=5 V, RES=1.5 V, LPC HIGH=1.5 V, Gate Width=5 μs (V_{REF}=$V_{CATHODE}$ $I_{CATHODE}$=5 mA)	1.37	1.40	1.43	V

Notes:

3. V_{DD}>V_{DD_ON} : enable cathode pin (disable to pull HIGH cathode pin).
4. Guarantee by Design

Typical Performance Characteristics

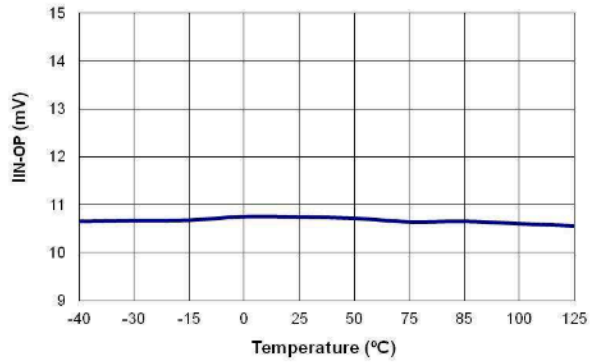


Figure 5. Operating Current (I_{IN-OP}) vs. Temperature

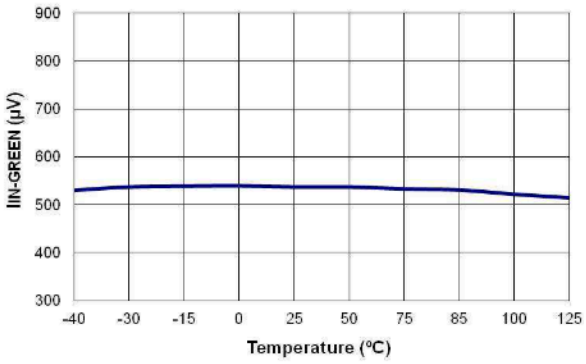


Figure 6. Operation Current in Green Mode ($I_{IN-GREEN}$) vs. Temperature

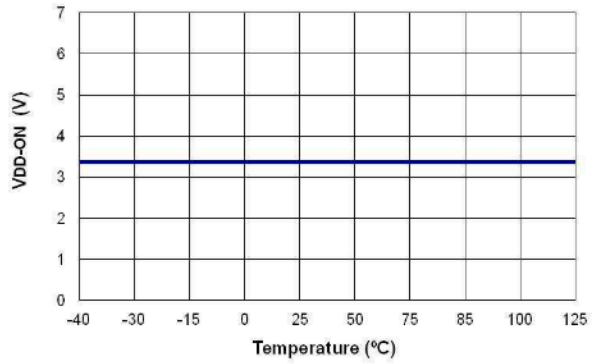


Figure 7. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

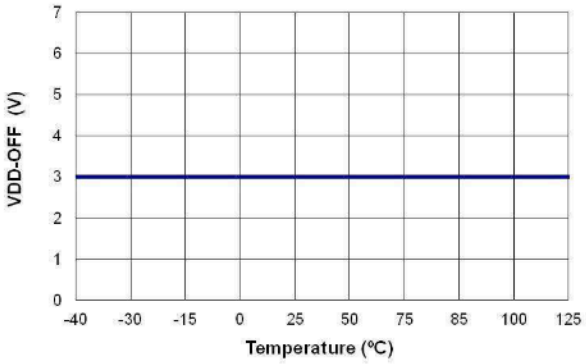


Figure 8. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

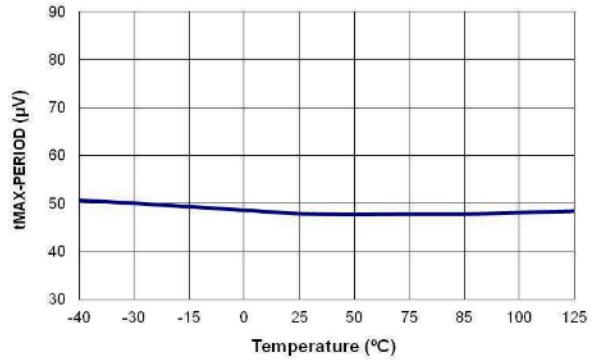


Figure 9. Maximum Period ($t_{MAX-PERIOD}$) vs. Temperature

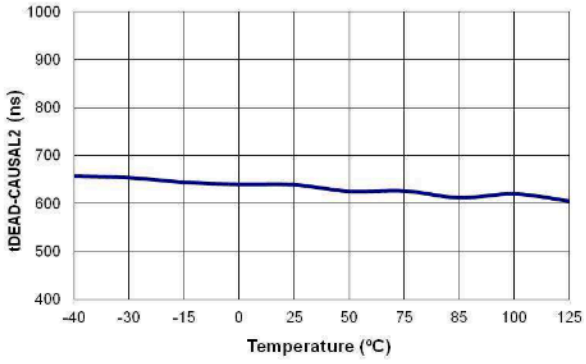


Figure 10. SR Turn-Off Dead Time by Causal Function at Low Line ($t_{DEAD-CAUSAL2}$) vs. Temperature

Typical Performance Characteristics

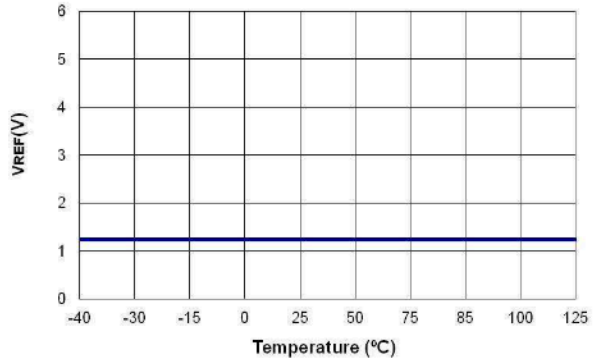


Figure 11. Reference Voltage (V_{REF}) vs. Temperature

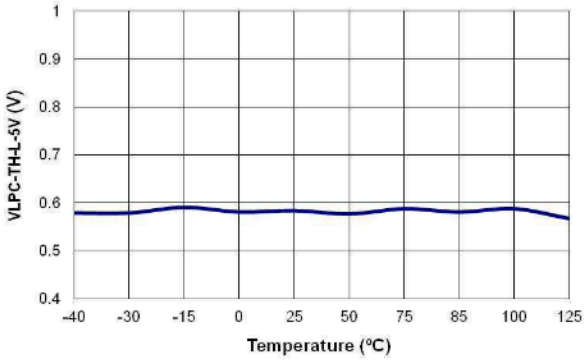


Figure 12. Threshold Voltage on LPC Rising Edge at Low-Line ($V_{LPC-TH-L-5V}$) vs. Temperature

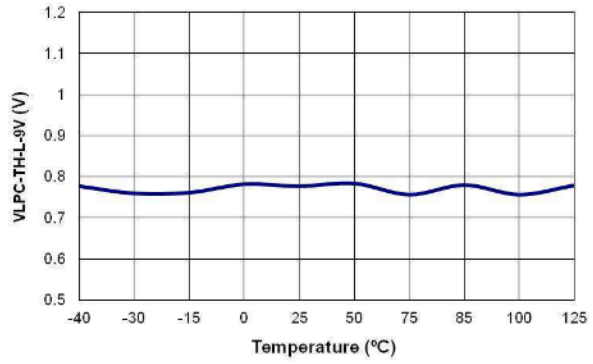


Figure 13. Threshold Voltage on LPC Rising Edge at Low-Line ($V_{LPC-TH-L-9V}$) vs. Temperature

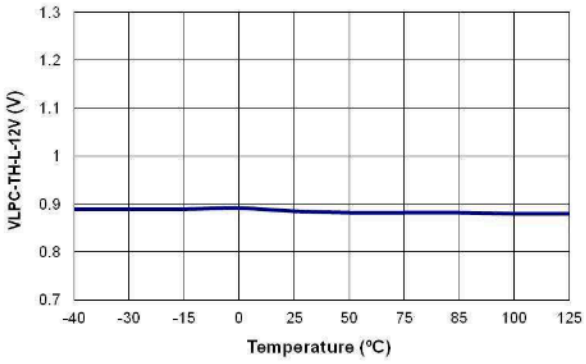


Figure 14. Threshold Voltage on LPC Rising Edge at Low-Line ($V_{LPC-TH-L-12V}$) vs. Temperature

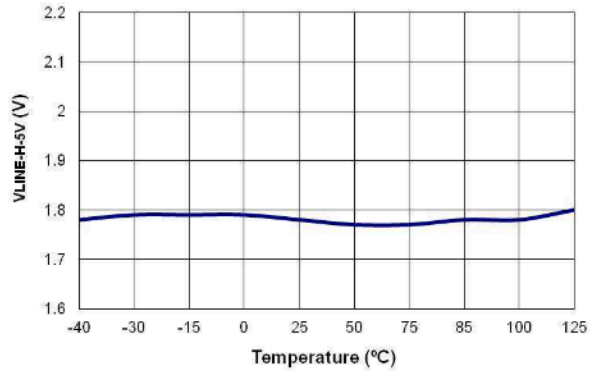


Figure 15. Low-to High-Line Threshold Voltage on LPC Pin ($V_{LINE-H-5V}$) vs. Temperature

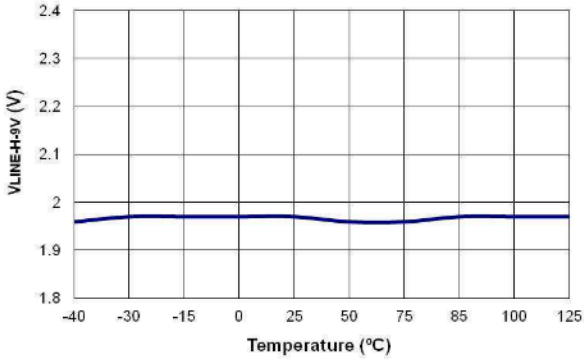


Figure 16. Low-to High-Line Threshold Voltage on LPC Pin ($V_{LINE-H-9V}$) vs. Temperature

Typical Performance Characteristics

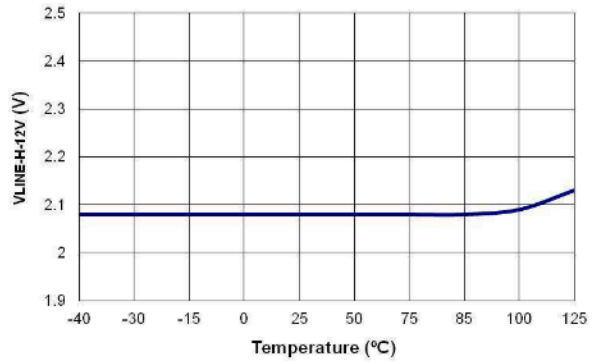


Figure 17. Low-to High-Line Threshold Voltage on LPC Pin ($V_{LINE-H-12V}$)vs. Temperature

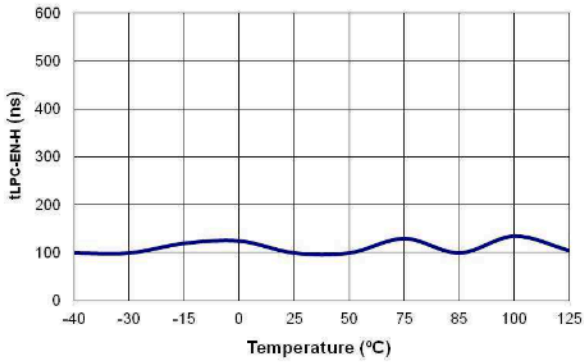


Figure 18. Minimum LPC Time to Enable SR Gate at High-Line ($t_{LPC-EN-H}$) vs. Temperature

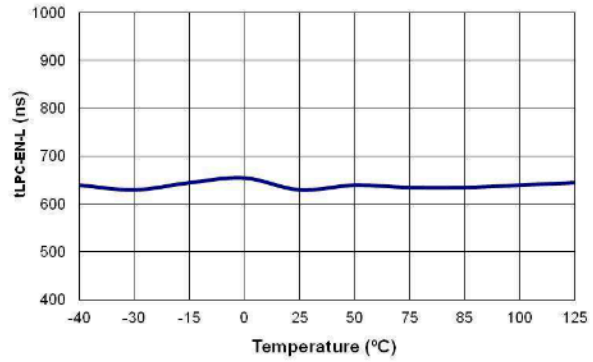


Figure 19. Minimum LPC Time to Enable SR Gate at Low-Line ($t_{LPC-EN-L}$) vs. Temperature

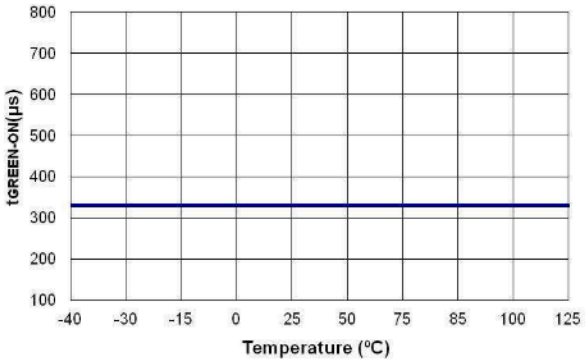


Figure 20. Minimum LPC Non-Switching Period to Enter Green Mode ($t_{GREEN-ON}$) vs. Temperature

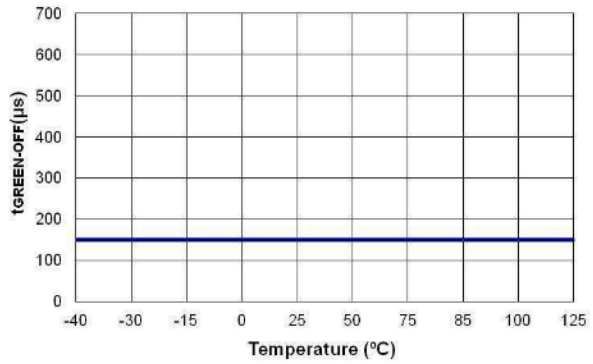


Figure 21. Minimum LPC Non-switching Period to Exit Green Mode ($t_{GREEN-OFF}$) vs. Temperature

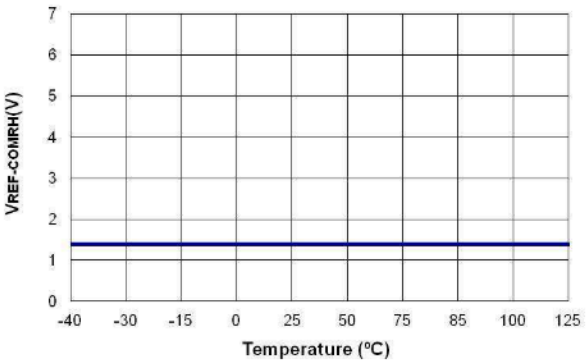


Figure 22. Cable Compensation at High-Line ($V_{REF-COMRH}$) vs. Temperature

Theory of Operation of SR Control

Synchronous rectification is widely used for low-voltage and high-current power converter applications to maximize efficiency. By replacing the rectifier diode with a MOSFET operating as a synchronous rectifier (SR), the equivalent forward-voltage drop can be lowered and consequently the conduction loss can be reduced. Unlike buck-derived topologies, the control of synchronous rectification of a flyback converter is challenging since it is a current-fed capacitor-loaded circuit structure. For this kind of circuit, the polarity of the voltage on the transformer secondary winding can change only after the synchronous rectifier (SR) is turned off. This is because the voltage on the secondary winding is clamped to the output voltage while the SR is conducting. Thus, the SR current zero crossing instant should be predicted to properly turn off the SR gate before the SR current reaches zero, which allows the SR body diode to naturally turn off blocking reverse current flow.

Figure 23 shows a simplified flyback converter with a synchronous rectification and its key waveforms. When the switch Qp is turned on, the input voltage is applied to the primary side magnetizing inductor of the transformer and the magnetizing inductor current ramps up. When the Qp is turned off, the reflected output voltage is applied across the primary side magnetizing inductor and the magnetizing inductor current ramps down. Depending on whether the converter operates in continuous conduction mode (CCM) or discontinuous conduction mode (DCM), the SR current zero crossing instant is determined differently. When operating in DCM, the SR current zero crossing instant changes according to the duty cycle of the primary side gate drive signal. Whereas, the SR current zero crossing instant in CCM operation is when the primary side switch is turned on. Thus, two different methods (linear predict and causal predict) are used in FAN6230A to anticipate the SR current zero crossing instant for both CCM and DCM operation.

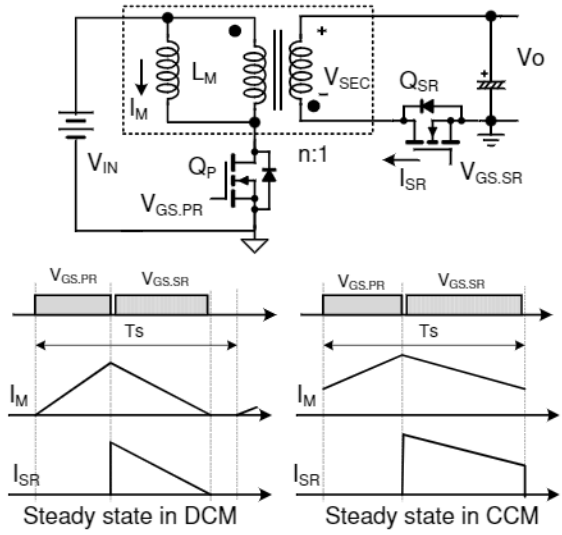


Figure 23. Flyback Converter and Key Waveforms for Each Operating Mode

1. Linear Predict Control (LPC)

Figure 24 shows the conceptual circuit of linear predict control and its related waveforms. In DCM operation, the transformer current (magnetizing inductor current) always ramps up from zero when a new switching cycle starts. This current ramps down to zero before the next switching cycle starts. Since the slope of the magnetizing current is determined by the voltage applied across the magnetizing inductor, the voltage second balance equation shows when the magnetizing current returns to its initial value after one switching cycle.

$$\frac{V_{IN}}{L_m} t_{ON} = \frac{nV_{OUT}}{L_m} t_{DIS} \quad (1)$$

Even in CCM operation, the voltage-second balance equation (1) is satisfied as long as the converter operates in steady state.

The basic idea of the linear predict method is to predict the instant when the magnetizing current of the transformer goes back to its initial condition after completing one switching cycle by emulating the operation of the magnetizing inductor current. Inductor current can be emulated by taking the transformer winding voltage which is converted to a current and then injected into a timing capacitor. The timing capacitor voltage emulates the inductor current and therefore the SR current zero crossing instant can be predicted for proper SR gate drive.

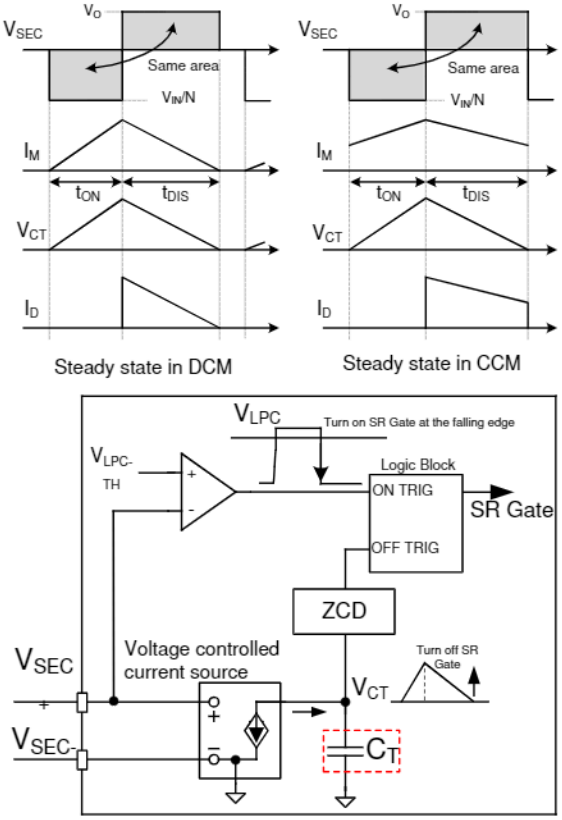


Figure 24. Conceptual Circuit of Linear Predict Control

2. Causal Predict Control (CPC)

Even though the linear predict method anticipates the SR current zero crossing instant very effectively in DCM operation, it has limitations for CCM operation. This is because the magnetizing current does not go back to its initial condition at the end of the switching cycle when the converter goes through a transient in CCM as illustrated in Figure 25. Thus, the linear predict method results in late termination of the SR gate, which can cause shoot-through since both primary side and secondary side switches are on at the same. To guarantee reliable SR control over all operating modes, another SR control method - causal predict control is also employed in the FAN6230A.

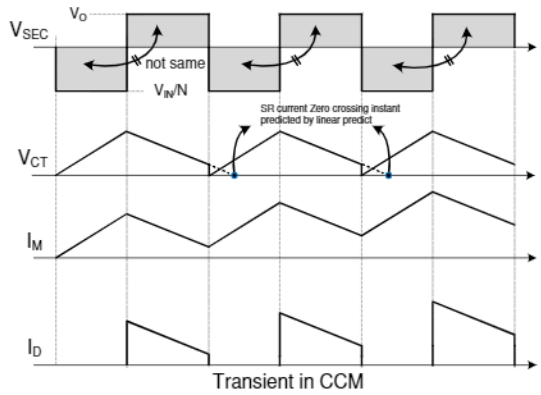


Figure 25. Magnetizing Current Waveform during Transient in CCM

Causal predict control anticipates the SR current zero crossing instant based on the switching period of the previous switching cycle as illustrated in Figure 26. Basically the causal predictive SR control is based on the assumption that the switching frequency does not change much between two consecutive switching cycles. Thus, this method predicts the switching instant of the current switching cycle according to the switching pattern of the previous switching cycle.

As can be seen in Figure 26, CPC anticipates the SR current to cross zero later than the actual zero crossing in DCM. However, LPC predicts the SR current zero crossing instant properly in DCM. For CCM operation, LPC anticipates the SR current to cross zero later than the actual zero crossing. Whereas, CPC predicts the SR current zero crossing instant properly in CCM.

FAN6230A uses the zero crossing anticipation signals from LPC and CPC and among the two signals, the signal introduced first triggers the turn-off of the SR switch.

One limitation of CPC is that it requires a relatively large dead time when the primary side PWM controller has variable frequency operation for output regulation or frequency modulation for EMI reduction. This is to cover the possible switching period variation between two consecutive switching cycles determined by the primary side PWM controller.

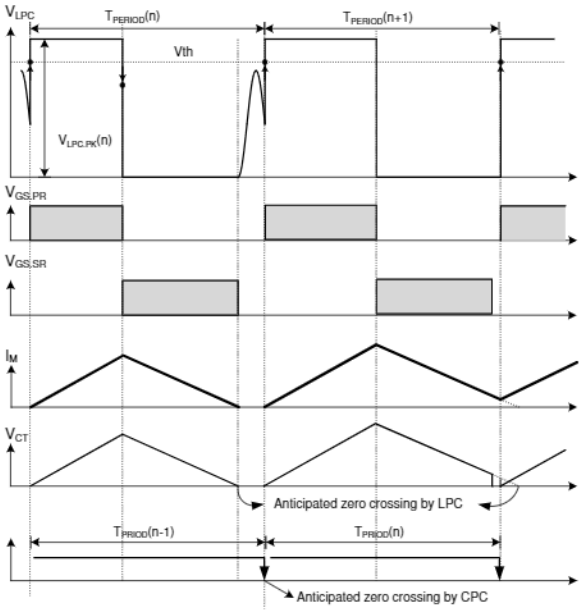


Figure 26. Operation of Causal Predict Control

Functional Description

Circuit Operations

3. SR Turn-on Trigger by LPC Pin Voltage

The most important signal that FAN6230A uses for SR control is the LPC pin voltage since it is used to detect the turn-on and turn-off instants of the primary side switch. Figure 28 shows the typical operation together with the LPC voltage waveforms for DCM and CCM operation. The issue is that oscillation occurs on the LPC signal when both the primary side MOSFET and the SR MOSFET are off in DCM operation. To maintain proper SR control, it is essential to distinguish the oscillation from the actual PWM switching. The LPC voltage must meet two conditions in order to be recognized as a valid LPC voltage generated by PWM switching.

- The LPC voltage should rise above 90% of sampled LPC voltage of the previous switching cycle. The 90% of the LPC sampling voltage should be also higher than V_{LPC-TH}. In other words, the LPC voltage sampling voltage should be higher than V_{LPC-TH} /0.9 ($V_{LPC-HIGH}$).
- In addition, LPC voltage should remain above the threshold longer than the LPC enable time (t_{LPC-EN}). The LPC enable time is adaptively changed according to the operating condition as $t_{LPC-EN-H}$=180 ns for high line and $t_{LPC-EN-L}$=700 ns for low line, respectively.

Once the LPC voltage is recognized as valid, the LPC voltage sampling takes place when t_{LPC-EN} expires. The sampled LPC voltage is used to generate the threshold to validate LPC voltage next time and also utilized to drive the voltage controlled current source for linear predict control.

When the LPC voltage that is recognized as valid LPC signal drops below V_{LPC-TH}, the SR MOSFET is turned on.

For several V_{IN} voltage applications, modulations of $V_{LPC-TH-L}$ as a function of V_{IN} voltage are necessary, shows in Figure 27, and Table 1 shows detailed $V_{LPC-TH-L}$ and $V_{LPC-TH-H}$ for low line and high line condition, respectively.

To prevent miss-trigger of SR in DCM operation, FAN6230A has an LPC falling detect protection, the LPC voltage should drop fast passing two detect thresholds within trigger time.

Even when the LPC voltage drops fast satisfying the conditions listed above, it is ignored when it happens within $t_{INHIBIT}$ (1.4 µs) inhibit time after the SR turn-off instant.

Table 1. Detailed Parameter by LPC Pin with Low Line and High Line Condition

Parameter	Condition	Value (Typ.)	Unit
$t_{LPC-EN-H}$	High Line	180	ns
$t_{LPC-EN-L}$	Low Line	700	ns
$V_{LPC-HIGH-H}$	High Line	1.5	V
$V_{LPC-HIGH-L-5V}$	Low Line, 5 V Output	0.68	V
$V_{LPC-HIGH-L-9V}$	Low Line, 9 V Output	0.88	V
$V_{LPC-HIGH-L-12V}$	Low Line, 12 V Output	1.02	V
$V_{LPC-TH-H}$	High Line	1.25	V
$V_{LPC-TH-L-5V}$	Low Line, 5 V Output	0.60	V
$V_{LPC-TH-L-9V}$	Low Line, 9 V Output	0.77	V
$V_{LPC-TH-L-12V}$	Low Line, 12 V Output	0.90	V
$V_{LPC-TH-TRIG}$		70	mV

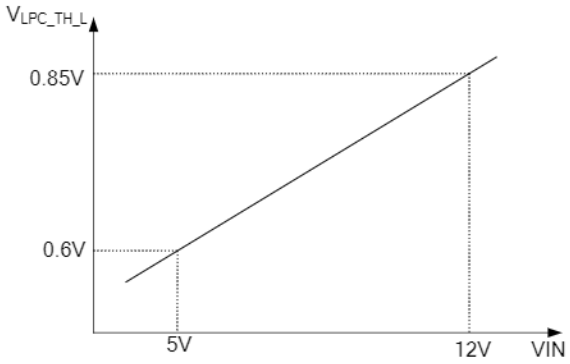


Figure 27. Modulation of $V_{LPC-TH-L}$ as a Function of V_{IN} Pin Voltage

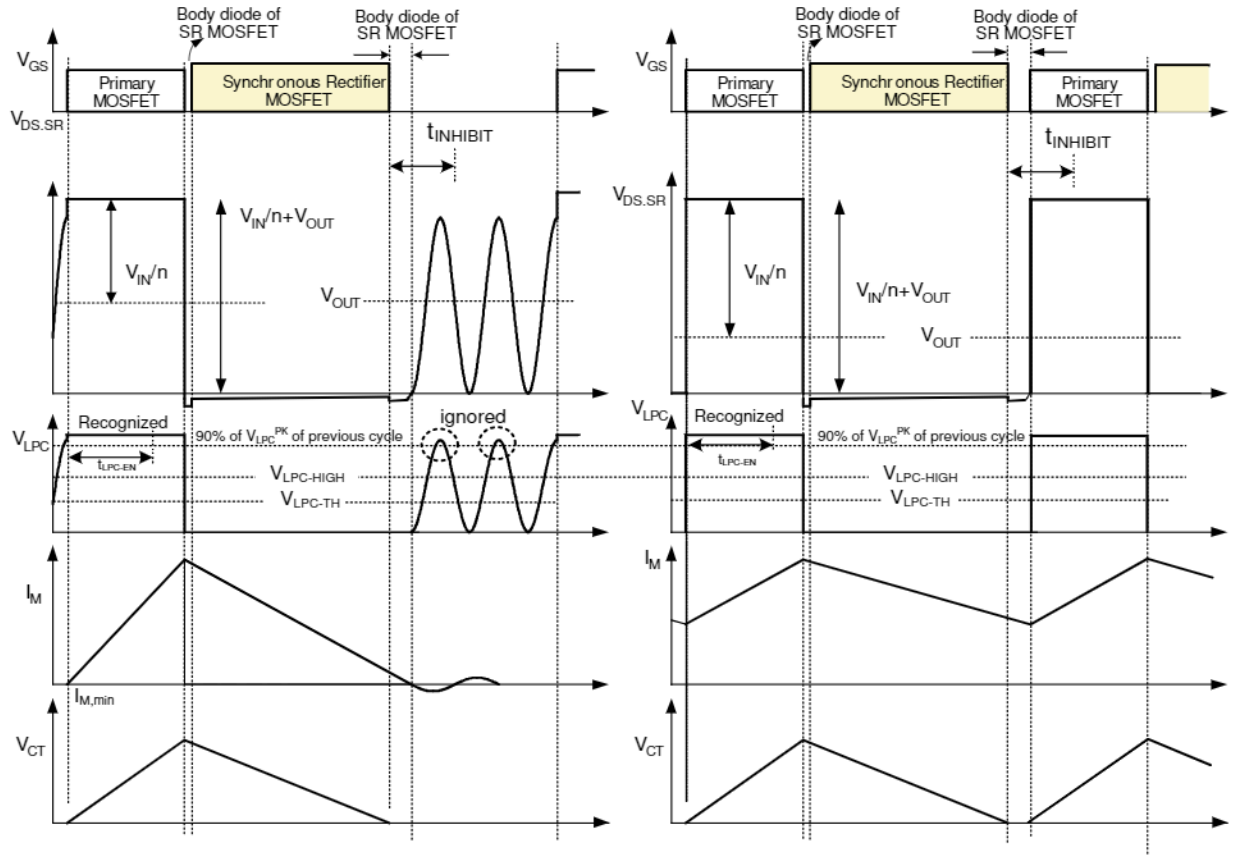


Figure 28. Typical Waveforms of Linear-Predict Timing Control in DCM and CCM Operation

4. Low / High Line Detection with LPC Voltage

According to the LPC sampling voltage, the low line and high line conditions are detected, which adjusts several key parameters according to the line voltage. The threshold voltages for line voltage detection are listed below.

Table 2. Threshold Voltages for Line Voltage Detection

Parameter	Condition	Value (Typ.)	Unit
$V_{LINE-H-5V}$	High Line Detect	1.80	V
$V_{LINE-L-5V}$	Low Line Detect	1.70	V
$V_{LINE-H-9V}$	High Line Detect	1.97	V
$V_{LINE-L-9V}$	Low Line Detect	1.87	V
$V_{LINE-H-12V}$	High Line Detect	2.27	V
$V_{LINE-L-12V}$	Low Line Detect	2.09	V
$t_{LPC-LH-debounce}$	From Low to High Line	18	ms
$t_{LPC-HL-debounce}$	From High to Low Line	15	µs

5. SR Turn-Off Trigger by Linear Predict

Figure 29 shows the linear predict control block diagram. The basic idea of the linear predict method is to estimate the instant when the magnetizing current of the transformer goes back to its initial condition after completing one switching cycle by emulating the operation of the magnetizing inductor current. Two voltage controlled current sources and an internal timing capacitor are used to emulate the charging and discharging of the magnetizing inductor.

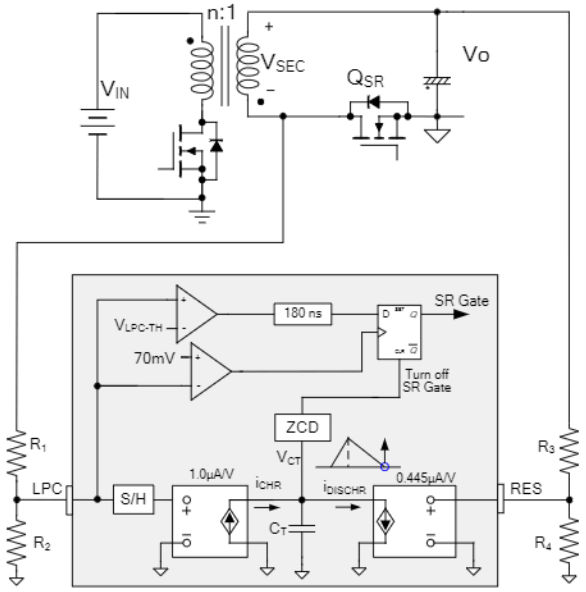


Figure 29. Linear-Predict Control Block

The current which charges the internal capacitor CT while LPC voltage is high is given as:

$$i_{CT1} = \frac{(\frac{V_{IN}}{N} + V_O)R_2}{R_1 + R_2} \cdot 1 \times 10^{-6} - \frac{V_O R_4}{R_3 + R_4} \cdot 0.445 \times 10^{-6} \quad (2)$$

Whereas, the current discharging the internal capacitor CT while LPC voltage is low is given as

$$i_{CT2} = V_O \frac{R_4}{R_3 + R_4} \cdot 0.445 \times 10^{-6} \quad (3)$$

The current-second balance of the capacitor which is equivalent to voltage second balance of the inductor is given as:

$$\begin{aligned} &[(\frac{V_{IN}}{N} + V_O)\frac{R_2 \cdot 1.0}{R_1 + R_2} - V_O \frac{R_4 \cdot 0.445}{R_3 + R_4}] \cdot T_{ON.PWM} \\ &= [V_O \frac{R_4 \cdot 0.445}{R_3 + R_4}] \cdot T_{ON.SR} \end{aligned} \quad (4)$$

By introducing a voltage divider ratio which is defined as $k = \frac{R_4}{R_3 + R_4} \cdot \frac{R_1 + R_2}{R_2}$, equation (4) can be simplified as:

$$[\frac{2.25}{k} \cdot (\frac{V_{IN}}{n} + V_{OUT}) - V_{OUT}] \cdot t_{ON.PWM} = V_{OUT} \cdot t_{ON.SR} \quad (5)$$

By setting k=2.25, the voltage-second balance equation is obtained from (4) as:

$$\frac{V_{IN}}{N} \cdot t_{ON.PWM} = V_O \cdot t_{ON.SR} \quad (6)$$

As shown in equation (6), the CT voltage zero crossing occurs when the SR current crosses zero. Considering the tolerance of the resistor dividers and internal circuit, the coefficient K should be slightly larger than 2.25 to guarantee that the SR gate is turned off before the SR current reaches zero.

Due to the allowable voltage ranges of the internal circuitry of the LPC and RES pins, there are several requirements for the LPC and RES voltage dividers.

- Since the minimum LPC sampling voltage allowing SR gate drive operation is $V_{LPC-HIGH}$, the minimum LPC sampling voltage should be higher than $V_{LPC-HIGH}$ as:

$$V_{LPC-HIGH-L} < \frac{R_2}{R_1 + R_2}(\frac{V_{IN.MIN}}{n} + V_{OUT}) \quad (7)$$

- To ensure the linear operation range of voltage controlled current source for LPC, the LPC voltage should be between 0.5 V and 4 V as:

$$0.5V < \frac{R_2}{R_1 + R_2}(\frac{V_{IN.MIN}}{n} + V_{OUT}) \quad (8)$$

$$\frac{R_2}{R_1 + R_2}(\frac{V_{IN.MAX}}{n} + V_{OUT}) < 4V \quad (9)$$

- To ensure the linear operation range of voltage controlled current source for RES pin, the RES voltage should be between 0.4 V and 4.2 V as:

$$0.4V < \frac{R_4}{R_3 + R_4} V_{OUT} < 4.2V \quad (10)$$

6. SR Turn-Off Trigger by Causal Predict

To ensure the proper operation of secondary side synchronous rectification, it is critical to turn off the SR MOSFET just before the turn on of next switching of primary side switch so that the two switches are not turned on at the same time. Table 3 shows the dead time introduced to the causal predict control.

Table 3. Dead Time Introduced to the Causal Predict Control

Parameter	Condition	Value (Typ.)	Unit
$t_{DEAD-CAUSAL1}$	CV Regulation, High Line	790	ns
$t_{DEAD-CAUSAL2}$	CV Regulation, Low Line	570	ns
$t_{DEAD-CAUSAL3}$	CC Regulation, Low Line	850	ns

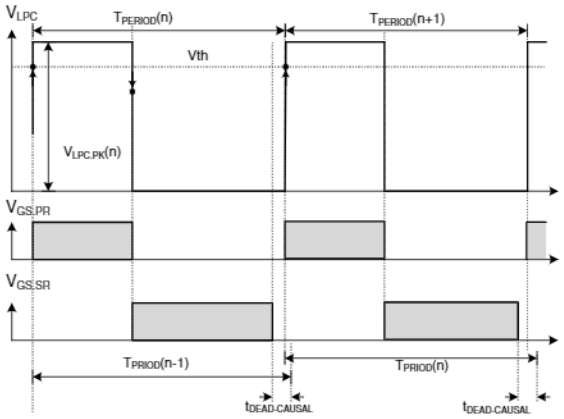


Figure 30. Operation of Causal Predict Control

7. SR Gate Expansion Limit Protection

Gate expansion limit protection controls the on-time expansion of the SR MOSFET. Once the discharge time of the internal timing capacitor ($t_{DIS.CT}$) is longer than 500ns plus previous on-time of the SR MOSFET ($t_{on-SR}(n-1)$); $t_{on-SR}(n)$ is limited to 500ns plus $t_{on-SR}(n-1)$ as shown in Figure 31. When output load changes rapidly from light load to heavy load, voltage-second balance theorem may not be applied. In this transient state, gate expand limit protection is activated to prevent overlap between the SR Gate and the PWM gate.

When the FAN6230A detects through the LPC pin voltage that the operating condition has changed between high line and low line, SR gate is reduced to its minimum (500 ns) and then recovers with SR gate limit function.

When the FAN6230A starts up or exits green mode, SR gate limit function is also incorporated resulting in soft-start of SR gate.

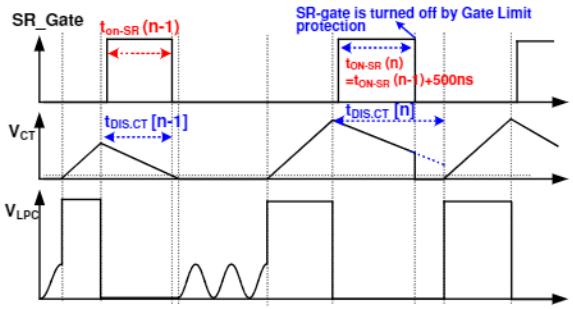


Figure 31. Operation of Gate Limit Function

8. RES Pin Operation

The output voltage of the flyback converter is sensed on the RES pin using a voltage divider. The output voltage information is used for the following functions.

- Linear Predict Control: The RES voltage is used to drive the voltage controlled current source for linear predict control.
- Output Short Protection: When the RES voltage drops below 0.2 V, SR is disabled. When RES voltage drops more than 10% compared to the RES voltage of the previous switching cycle, SR switching is also disabled (entering green mode).

Table 4. Parameters related to RES Pin

Parameter	Condition	Value (Typ.)	Unit
V_{RES-EN}		0.2	V
$K_{RES-DROP}$		90	%

9. Green Mode Operation

To improve the system efficiency of the power supply under light load conditions the FAN6230A provides green mode operation. Once the FAN6230A enters green mode, the major control functions including SR gate drive are disabled and the operating current is reduced from 12 mA to 500 µA. The conditions to enter and exit green mode are as follows.

- Enter Green Mode when the non-switching duration in burst mode (Non-switching time between two burst switching bundles) is longer than 330 µs.
- Exit Green Mode when the non-switching duration in burst mode is shorter than 150 µs or normal switching continues for longer than 256 consecutive switching cycles.

Table 5. Green Mode Definition

Parameter	Value (Typ.)	Unit
$t_{GREEN-ON}$	330	μs
$t_{GREEN-OFF}$	150	μs
$n_{GREEN-OFF}$	256	Cycle

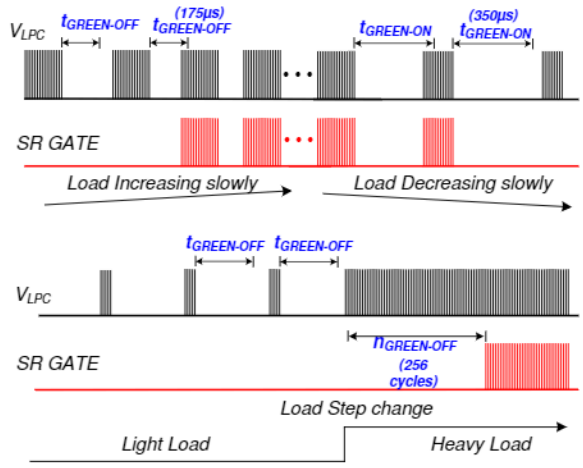


Figure 32. Entering and Exiting Green Mode

Additionally, there are three more transient conditions that force FAN6230A into green mode to prevent any abnormal condition. After the FAN6230A enters green mode during the following transient, the switching will resume after 256 switching cycles.

- The LPC voltage should rise above 90% of sampled LPC voltage of the previous switching cycle. If the 90% of the LPC sampling voltage less than V_{LPC_TH} , the FAN6230A enters into Green mode instant.
- When the RES voltage drops more than 10% compared to the RES voltage of the previous switching cycle, the FAN6230A enters into green mode.

10. Charge Pump Operation

To ensure its normal operation even with low supply voltage in CC operation in charger application, the FAN6230A has an integrated charge pump circuit. The internal charge pump circuits can be divided into two main stages. The front is the voltage clamping stage which is an LDO which provides power for the charge pump circuit. The charge pump stage has a voltage doubling mode and bypass mode, the selection of which is determined by to the voltage on the VIN pin as shown in Figure 33. When the VIN pin voltage is below 8 V, the charge pump is in voltage doubling mode. Then, the voltage clamping stage regulates its output around 2.6 V so that the charge pump can provide 5.2 V at the VDD pin. When the charge pump stage is in bypass mode, the voltage clamping circuit regulates V_{CLAMP} at 5.5 V, which is directly connected to VDD bypassing the charge pump.

For 5 V output charger applications, the charge pump stage is in voltage doubling mode most of the time to maintain a stable 5.2 V VDD supply voltage. To reduce the power consumption of the FAN6230A, the charge pump stage is in bypass mode in green mode with constant voltage regulation.

To stabilize the operation of the clamping stage, a 1 μF ceramic capacitor is typically used for V_{CLAMP} and CPN, respectively. For the VDD capacitor, 1-2 μF is recommended since too large of a capacitor can slow down the startup of the FAN6230A.

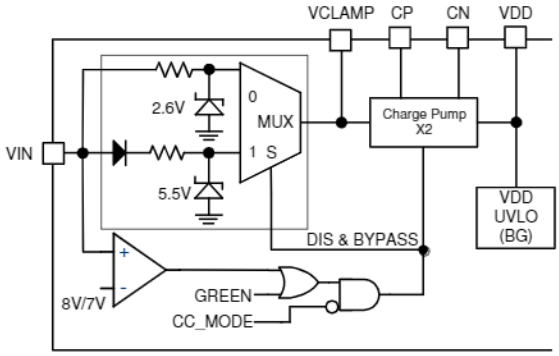


Figure 33. Internal Charge Pump Control Circuit

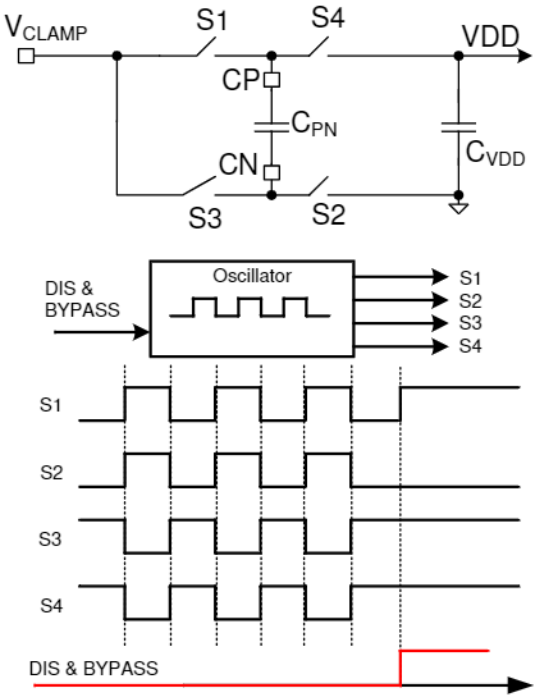


Figure 34. Charge Pump Circuit and Timing Diagram

Figure 35 shows the circuit for the power on sequence and the internal signals that connect to the reset pin of D flip flop disabling the SR gate drive signal. Detailed description of each signal is summarized in Table 6.

Table 6. Detailed Description of Each Signal

Signals to Disable SR	Description
GREEN	Green Mode
RES_SHORT	RES pin voltage is below 0.2 V
VDD_OVP	VDD pin voltage is higher than 7 V
MAX_PERIOD	LPC voltage rising above V_{LPC_TH} is not detected longer than 24 µs and 50 µs for CV mode and CC mode, respectively.
POW_ON	VDD is higher than 3.35 V
EN_32MS	32 ms after VDD rises above 3.35 V
LPC_RDY	LPC pin voltage is higher than V_{LPCTH}. 500 µs power up delay is also incorporated.

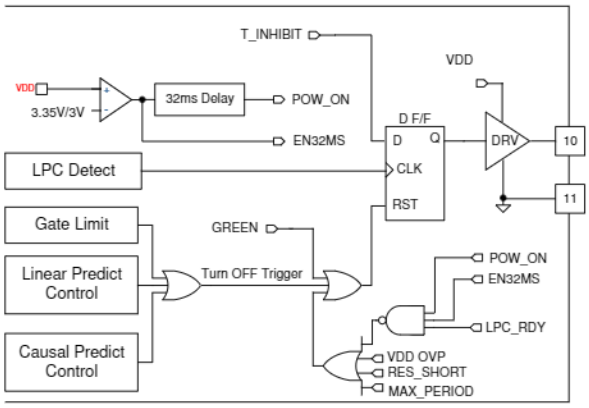


Figure 35. Conditions to Disables SR Switching

Figure 36 shows the corresponding startup and shutdown waveforms.

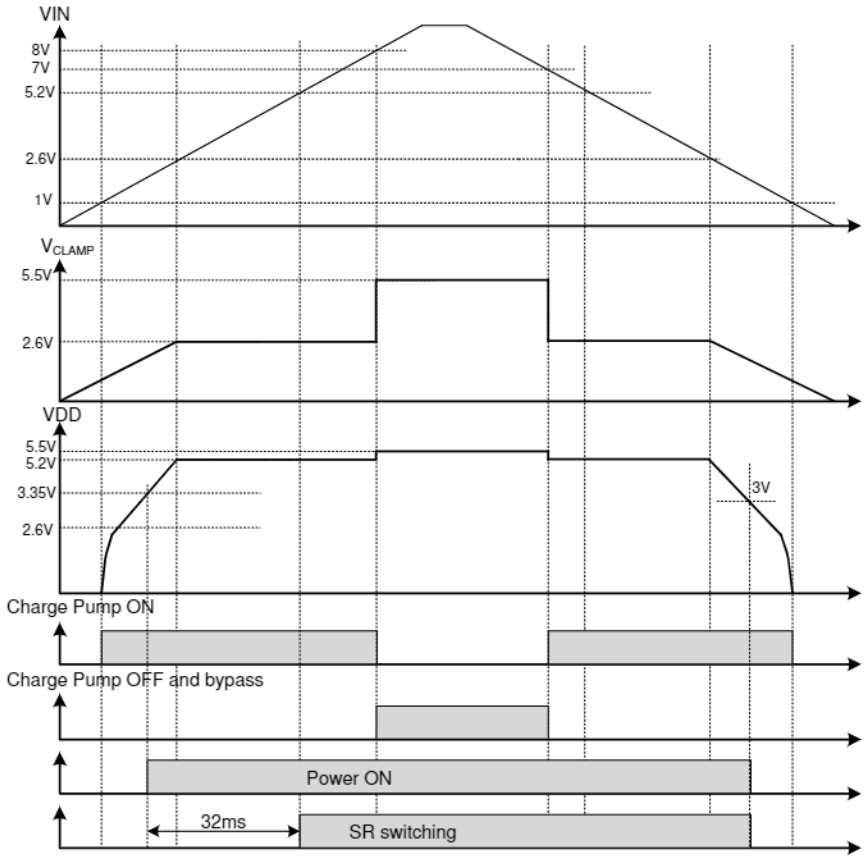


Figure 36. Power On Sequence Waveform

11. Cable Compensation

The FAN6230A has a built-in cable compensation circuit to provide regulated constant voltage at the end of the cable over the entire load range in CV Mode. The voltage drop across the load cable is compensated by adjusting the reference voltage of the internal shunt regulator as shown in Figure 37.

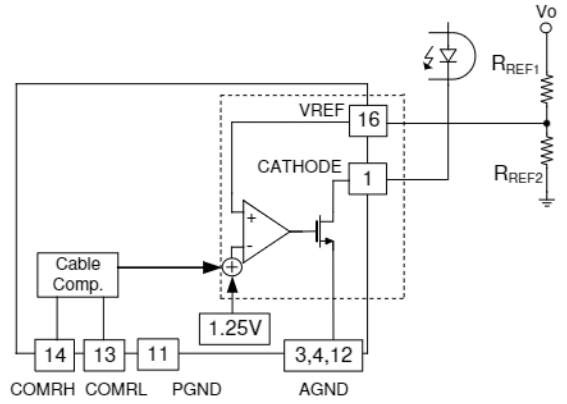


Figure 37. Cable Compensation

The CATHODE pin of the FAN6230A is typically connected to an opto-coupler to implement feedback to the primary side controller. Based on the control mechanism as addressed above, the setup of the cable compensation circuit can be described as follows:

$$V_{OUT} = \left[\frac{R_{REF1}+R_{REF2}}{R_{REF2}}\right] \cdot \left(1.25V + 0.8 \cdot \frac{t_{SR\_ON}^{2}}{T_{PERIOD}} \cdot R_{COMR}\right) \quad (11)$$

It is typical to connect a 1 nF bypass capacitor in parallel with the resistors for COMRH/L when the cable compensation function is used. Since the output current is estimated based on the conduction time of SR MOSFET, the cable compensation gain should be adjusted if the operation mode (CCM or DCM) changes with line voltage. Thus, FAN6230A has two pins for cable compensation gain setting (COMRH and COMRL) for high line and low line, respectively. When the compensation gain doesn't have to be adjusted with line voltage, connect COMRL pin to VDD. Then, the cable compensation gain for low line and high line is solely determined by the resistor on COMRH pin. The COMRH and COMRL pin can be also shorted to ground if no cable compensation is required; the COMR pin application is expressed in the table below:

Table 7. COMR Controller Method

COMRH	COMRL	Pins of Cable Compensation
VCOMRH	VCOMRL	VCOMRH & VCOMRL Program H/L Line Cable Compensation
VCOMRH	V_{DD}	VCOMRH Program H/L line Cable Compensation
V_{DD}	10 nF	Default Cable Compensation
0	0	No Cable Compensation

12. RES Dropping Protection

RES voltage is sampled and held as a reference voltage, V_{RES}, during the rising edge of the V_{LPC} and through t_{LPC-EN}. Once V_{RES} drops below 90% of the previous sampled and held, the green mode function could be trigger. Then SR gate drive signal is turned off immediately, as shown in Figure 38. When the output voltage drops rapidly, voltage-second balance on the primary-side magnetizing inductor, L_m, may not be satisfied. The RES-dropping protection activates to prevent driving signals overlapping.

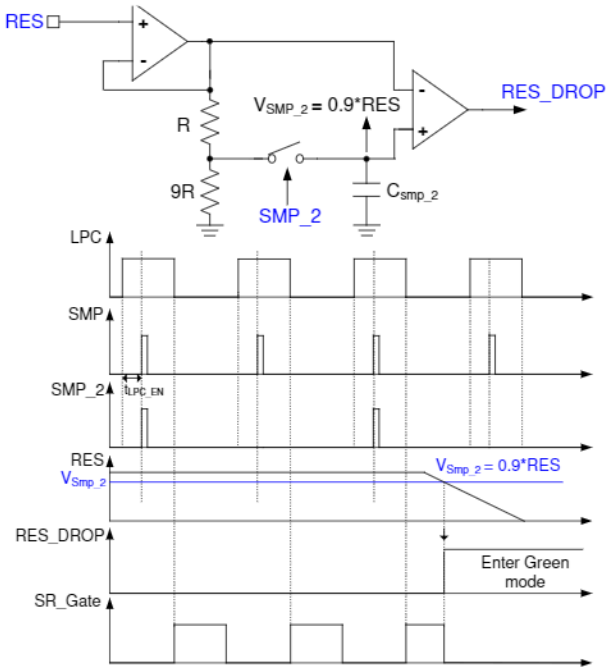


Figure 38. V_{RES} Dropping Protection

13. Under-Voltage Lockout (UVLO)

V_{DD} can serve as UVLO protection. The ON and OFF thresholds of V_{DD} are 3.35 V and 3 V, respectively. With ultra-low V_{DD} thresholds, the FAN6230A can be used in low output voltage applications.

14. Causal Period Protection (CPP)

When the causal function fails in CCM operation, such as the first period is longer than next period of switching cycle, the SR will have an overlap issue. To prevent the SR gate from faulty triggering until next PWM rising, an internal Causal Period Protection is integrated. If the second period ($t_{PERIOD}(n+1)$) is more than first period ($t_{PERIOD}(n)$) of 150%, meaning $t_{PERIOD}(n+1) > t_{PERIOD}(n) \times 150\%$, SR Gate pulse is disabled in the next period of switching cycle, shown in Figure 39.

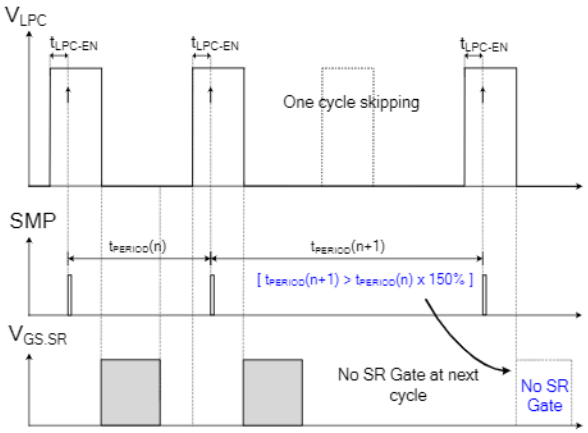


Figure 39. Causal Period Protection

Layout Guidelines

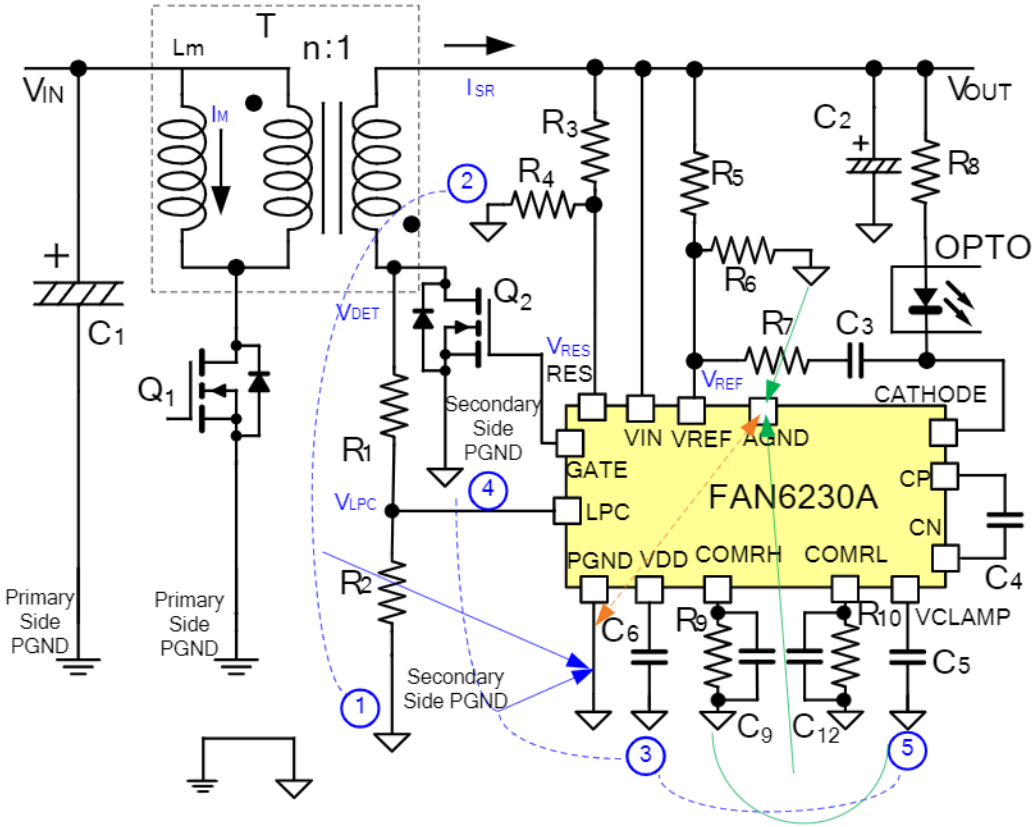


Figure 40. Simplified Typical Application Circuit

Layout plays a critical role to ensure normal operation of the FAN6230A. Using a simplified application circuit as an example illustrates the issues to consider while laying out the PCB.

As shown in Figure 40, C_1 and C_2 are the input and output capacitor, respectively. T is the flyback transformer. Q_1 is the primary side main switch. Q_2 is the secondary side SR MOSFET controlled by the FAN6230A. The main current flows through the transformer secondary side winding, C_2 and Q_2. So, the loop formed by the transformer secondary side winding, C_2 and Q_2 should be kept as small as possible. The power ground 1 should be connected to power ground 2 first and then to the PGND pin. Since the charge pump output provides the supply voltage to drive the MOSFET gate, the loop from the GATE pin to the gate of Q_2 and from Q_2 source to the ground of C_6 should be kept as small as possible. Therefore, connect the power ground 3, 4 and 5 together first and then to the PGND pin of the FAN6230A.

The resistors R_5 and R_6 sense the output voltage. So the ground of R_6 can be connected to the converter output capacitors or at the load side after the cable to get good voltage regulation. And the ground of R_6 should return to AGND of the IC directly to minimize noise. Resistor R_9 and R_{10} are used for cable compensation. The grounds of both resistors should be connected together first and then tied to the AGND of the IC. Finally, the AGND and PGND of the IC should be connected together with a single trace on the PCB as shown by the orange arrow.

It is important to make the ground traces width as larger as possible for better noise immunity.

Quick Setup Example for LPC and RES Voltage Dividers

Design Specifications

- Maximum Input Voltage: 375 V_{DC} (265 V_{AC})
- Minimum Input Voltage: 80 V_{DC} (90 V_{AC} with 10 V_{DC} ripple)
- Output Voltage: 5 V
- Cable drop compensation: 0.4 V
- Transformer Turns Ratio: n=13 (Np/Ns)
- Maximum SR Drain Voltage: 375/13+(5+0.4)=34.24 V
- Minimum SR Drain Voltage: 80/13+(5+0.4)=11.55 V

$$\frac{R_2}{R_1+R_2}\left(\frac{V_{IN,MIN}}{n}+V_{OUT}\right)>V_{LPC-HIGH-L-5V(Max.)}\Rightarrow\frac{R_2}{R_1+R_2}\cdot(11.55V)>0.74V\Rightarrow\frac{R_2}{R_1+R_2}>\frac{1}{15.61}$$

$$\frac{R_2}{R_1+R_2}\left(\frac{V_{IN,MAX}}{n}+V_{OUT}\right)<V_{DD}-1\Rightarrow\frac{R_2}{R_1+R_2}\cdot(34.24V)<4.2V\Rightarrow\frac{R_2}{R_1+R_2}<\frac{1}{8.15}$$

$$\therefore 8.15<\frac{R_1+R_2}{R_2}<15.61$$

$$\frac{R_4}{R_3+R_4}(V_{OUT})>V_{RES(Min.)}\Rightarrow\frac{R_4}{R_3+R_4}\cdot(5.4V)>0.4V\Rightarrow\frac{R_4}{R_3+R_4}>\frac{1}{13.5}$$

$$\frac{R_4}{R_3+R_4}(V_{OUT})<V_{DD}-1\Rightarrow\frac{R_4}{R_3+R_4}\cdot(5.4V)>4.2V\Rightarrow\frac{R_4}{R_3+R_4}>\frac{1}{1.28}$$

$$\therefore 1.28<\frac{R_3+R_4}{R_4}<13.5$$

The scale-down ratio (LPC/RES ratio) should be larger than 2.25 to guarantee that SR gate is turned off before the secondary side diode current reaches zero.

Selecting $\frac{R_1+R_2}{R_2}=12.12$ and considering exceed 20% margin on LPC/RES ratio, $\frac{R_3+R_4}{R_4}=\frac{R_1+R_2}{R_2}/(2.25\times1.2)=4.4$

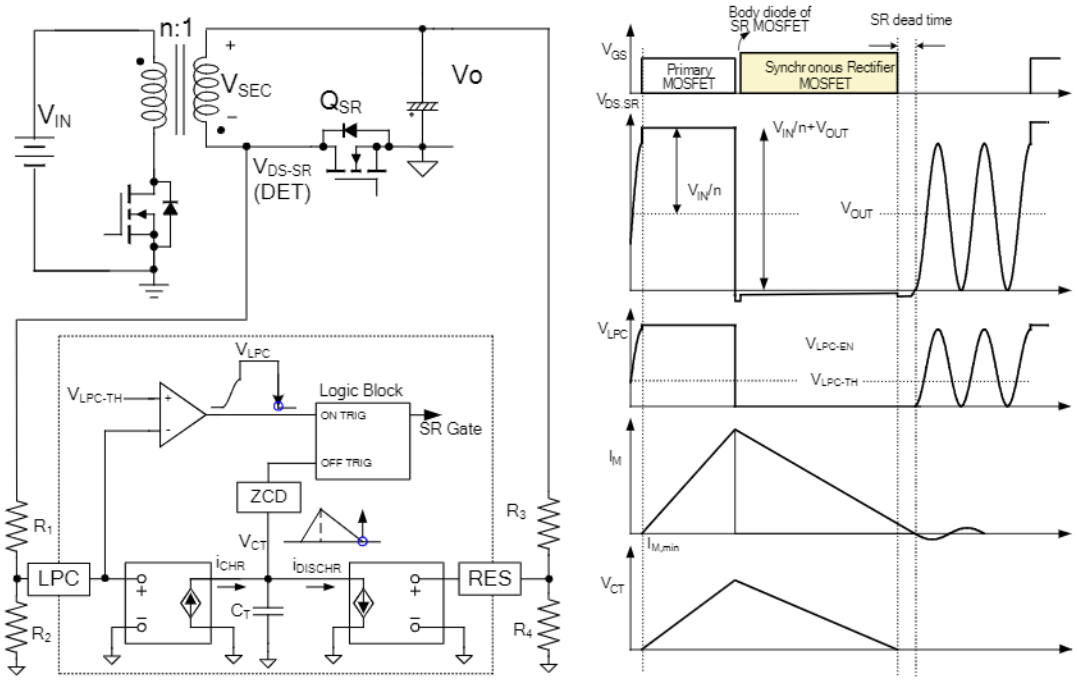


Figure 41. Simplified Linear-Predict Block

When flyback converter operates in DCM, the primary side MOSFET voltage ($V_{DS.PRI}$) oscillates when the secondary side diode current reaches zero, which is caused by the resonance between the effective output capacitor of the MOSFET and magnetizing inductance of the transformer. This also causes oscillation on the SR MOSFET voltage ($V_{DS.SR}$) as illustrated below where the peak to peak amplitude of the SR drain voltage is twice the output voltage. As input voltage drops causing the oscillation amplitude ($2V_O$) to be larger than the nominal SR drain voltage ($V_{IN}/n+V_O$), the oscillation on the LPC voltage can cause shrink of SR Gate in next cycle since the oscillation is clamped at the peak.

To avoid an abnormal condition, it is recommended to design the proper turn ratio of the transformer such that SR Gate voltage does not shrink if SR MOSFET voltage of 90% ($0.9\ V_{DS.SR.PK}$) is higher than $2V_O$ and V_{IN} is equal to the average of maximum DC voltage plus minimum DC voltage for consideration. Refer to the following calculation:

$$(\frac{V_{IN}}{N_{tr}}+Vo)\times 0.9 > V_{DET\_resonance} \Rightarrow N_{tr} < \frac{V_{IN}}{(V_{DET\_resonance}/0.9)-Vo}$$

$$when\ \ V_{IN}: V_{DC\_AVG} = 0.5\times(V_{DC\_MAX}+V_{DC\_MIN})$$

$$when\ \ V_{DET\_resonance} = 2\times V_O$$

With the design example, V_{AC}=90 V, V_O=12 V, I_O=1.56 A, C_{IN}=44 µF;

$$N_{tr} < \frac{112}{(24/0.9)-12} \quad \Rightarrow N_{tr} < 7.63$$

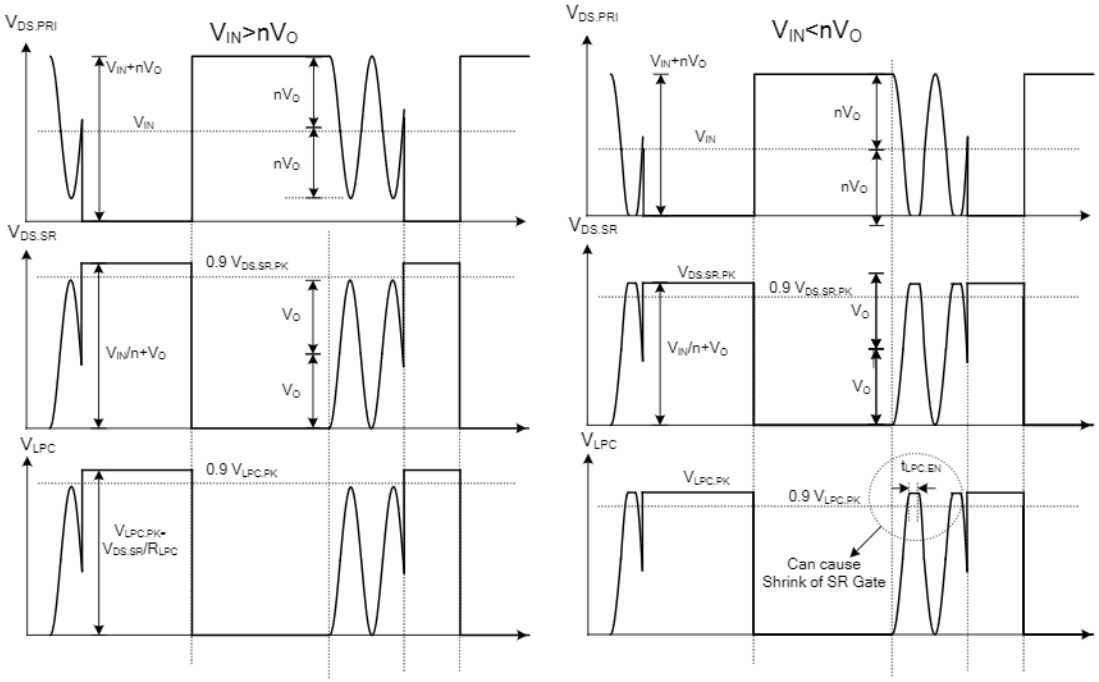


Figure 42. Condition that can cause SR Miss-Trigger by the Resonance of LPC Voltage

It is recommended that a series 20Ω resistor is added to the gate of FAN6230A to protect the Gate pin from big negative voltage spike that could happen in power supply application.

Typical Application Circuit (Flyback Charger)

Application	Fairchild Devices	Input Voltage Range	Output
Adaptive Charger	FAN501, FAN6230A	90~265 V_{AC}	5 V / 2.5 A

Features

- Ultra-Low Standby Power Consumption
- High Efficiency

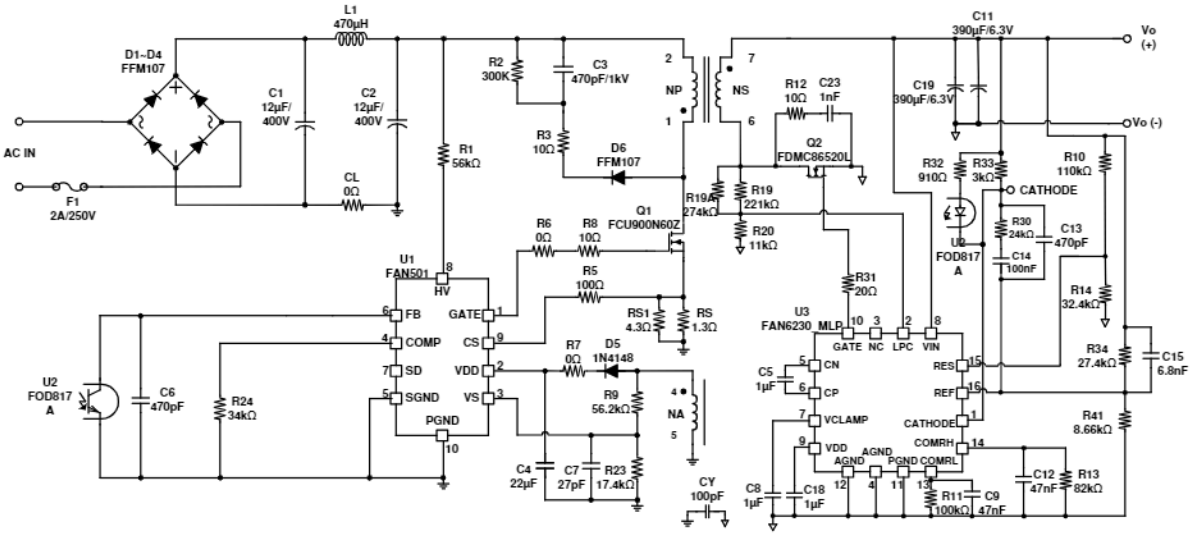


Figure 43. Schematic of Typical Application Circuit

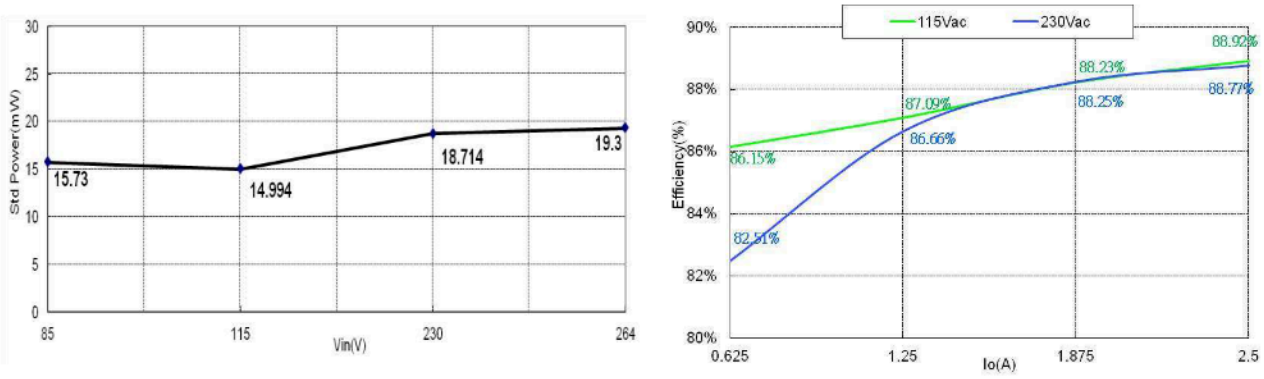


Figure 44. Standby Power and Measured Efficiency

Transformer Specification

- Core: EPC-1716 PC95
- Bobbin: EPC-1716

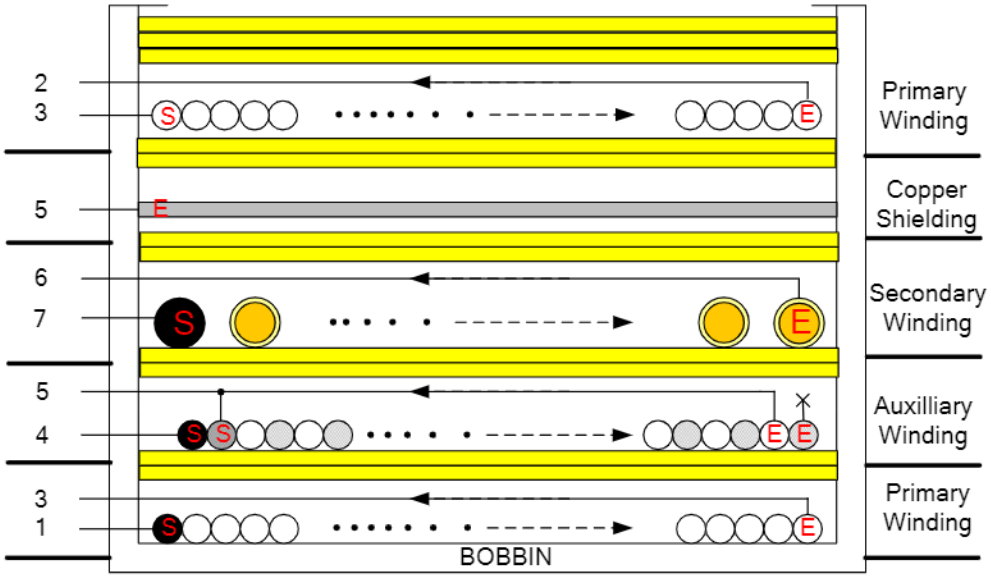
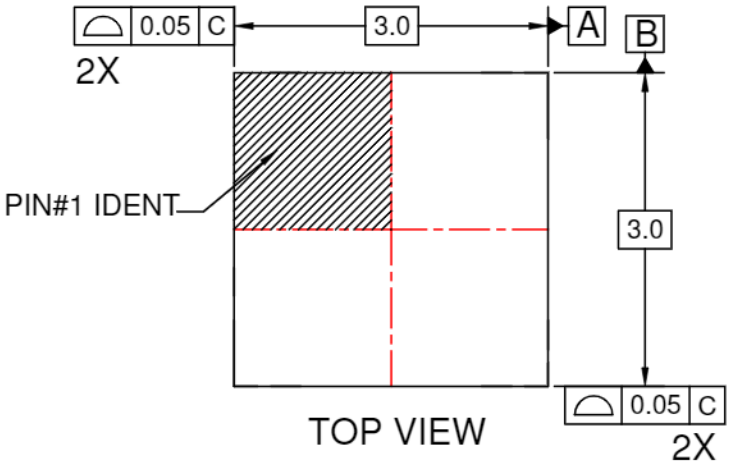


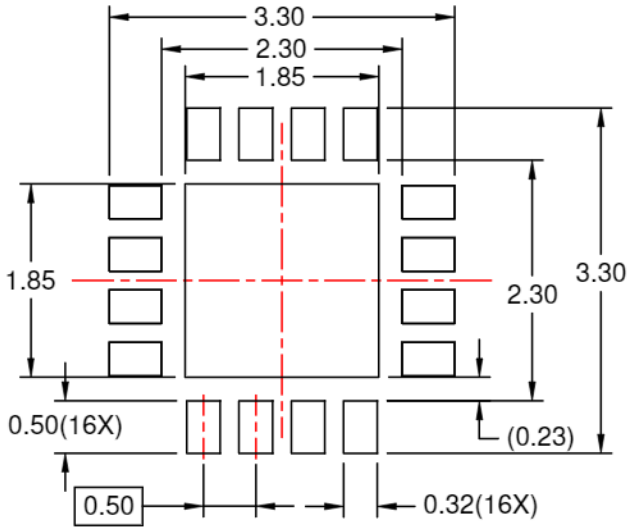
Figure 45. Transformer

Table 8. Transformer Winding Specifications

No.	Terminal		Wire	Turns	Isolation Layer Turns
	Start Pin	End Pin			
W1 (Pri. Winding)	1	3	2UEW 0.27*1	26	2
W2 (Aux. Winding)	4	5	2UEW 0.20*2	8	2
	5	X	2UEW 0.20*2	8	
W3 (Sec. Winding)	7	6	2UEW 0.60*2	4	2
W4 (Shielding)	5	X	Copper Shielding	1	2
W5 (Pri. Winding)	3	2	2UEW 0.27*1	26	3
Core Shielding	Copper	5	Copper Shielding	1	2

	Pin	Specification	Remark
Primary-Side Inductance	1-2	540 μH ± 5%	80 kHz, 1 V
Primary-Side Effective Leakage Inductance	1-2	30 μH ± 5%	80 kHz, 1 V, Short One Secondary Winding





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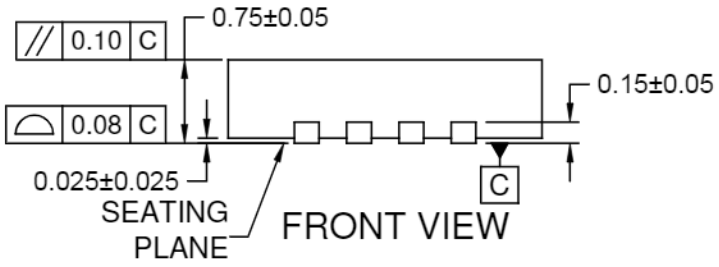

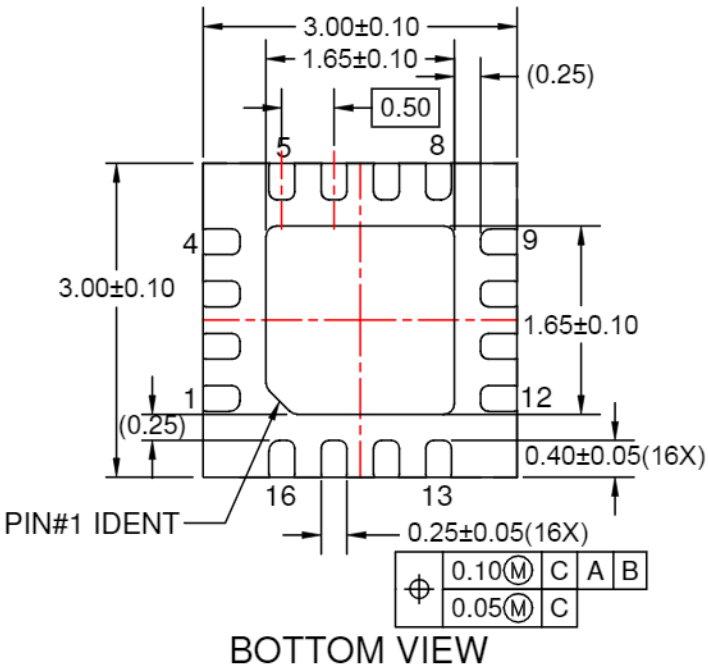

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