1. DESCRIPTION

The XD14538 is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an accurate output pulse over a wide range of widths, the duration and accuracy of which are determined by the external timing components, CX and RX. Output Pulse Width T = RX · CX (secs)

RX = Ω

CX = Farads

2. FEATURES

- Unlimited Rise and Fall Time Allowed on the A Trigger Input
- Pulse Width Range = 10 μs to 10 s
- Latched Trigger Inputs
- Separate Latched Reset Inputs
- 3.0 Vdc to 18 Vdc Operational Limits
- Triggerable from Positive (A Input) or Negative−Going Edge (B−Input)
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range

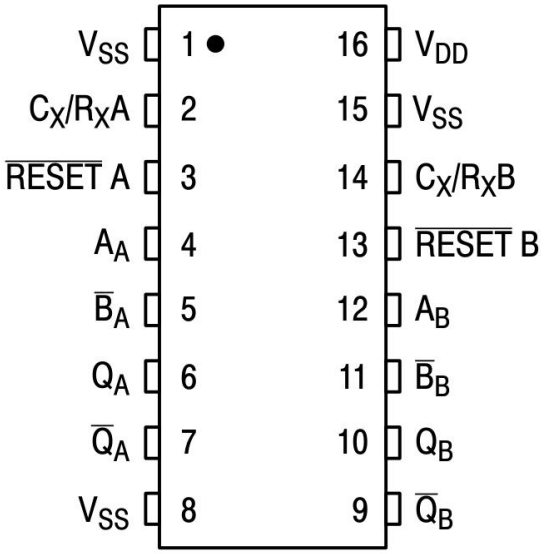
3. MAXIMUMRATINGS

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Operating Temperature Range	- 4 0 to +85	°C
T_{stg}	Storage Temperature Range	65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

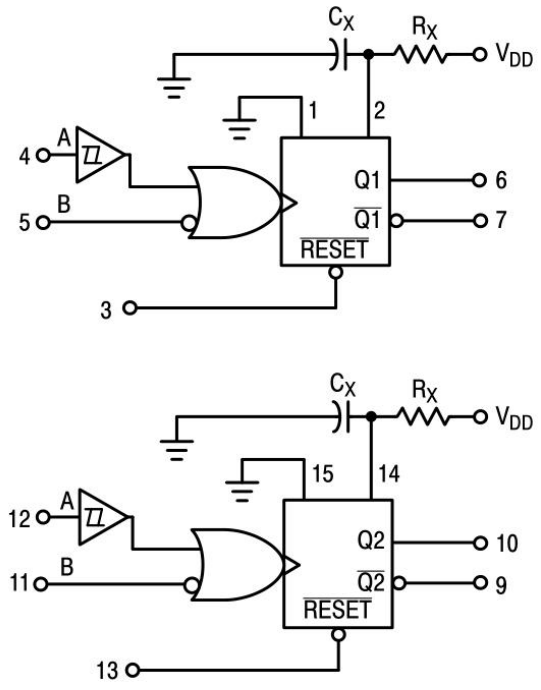
1. guard
   against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, Vin and Vout should be constrained to the range VSS ≤(Vin or Vout)≤VDD.
   Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

4. PIN ASSIGNMENT



(Top View)

5. BLOCK DIAGRAM



R_X AND C_X ARE EXTERNAL COMPONENTS.
V_{DD} = PIN 16
V_{SS} = PIN 8, PIN 1, PIN 15

6. ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	85°C Min	85°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V_O = 4.5 or 0.5 Vdc)	V_{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V_O = 0.5 or 4.5 Vdc)	V_{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11	–	11	8.25	–	11	–	
Output Drive Current (V_{OH} = 2.5 Vdc) Source	I_{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6 Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
(V_{OH} = 9.5 Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
(V_{OH} = 13.5 Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V_{OL} = 0.4 Vdc)	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current, Pin 2 or 14	I_{in}	15	–	±0.05	–	±0.00001	±0.05	–	±0.5	µAdc
Input Current, Other Inputs	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance, Pin 2 or 14	C_{in}	–	–	–	–	25	–	–	–	pF
Input Capacitance, Other Inputs (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package) Q = Low, $\overline{Q}$ = High	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current, Active State (Both) (Per Package) Q = High, $\overline{Q}$ = Low	I_{DD}	5.0	–	2.0	–	0.04	0.20	–	2.0	mAdc
		10	–	2.0	–	0.08	0.45	–	2.0	
		15	–	2.0	–	0.13	0.70	–	2.0	
Total Supply Current at an external load capacitance (C_L) and at external timing network (R_X, C_X) (Note 3)	I_T	5.0	$I_T = (3.5 \times 10^{-2})\ R_X C_X f + 4 C_X f + 1 \times 10^{-5}\ C_L f$							µAdc
		10	$I_T = (8.0 \times 10^{-2})\ R_X C_X f + 9 C_X f + 2 \times 10^{-5}\ C_L f$							
			$I_T = (1.25 \times 10^{-1})\ R_X C_X f + 12 C_X f + 3 \times 10^{-5}\ C_L f$							
			where: I_T in µA (one monostable switching only), C_X in µF, C_L in pF, R_X in k ohms, and f in Hz is the input frequency.							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
3. The formulas given are for the typical characteristics only at 25°C.

7. OPERATING CONDITIONS

External Timing Resistance	R_X	–	5.0	–	(Note 4)	kΩ
External Timing Capacitance	C_X	–	0	–	No Limit (Note 5)	μF

4. The maximum usable resistance RX is a function of the leakage of the capacitor CX, leakage of the XD14538, and leakage due to board layout and surface resistance. Susceptibility to externally induced noise signals may occur for RX > 1 MΩ..
5. If CX > 15 μF, use discharge protection diode per Fig. 11.

8. SWITCHING CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ (Note 7)	Max	
Output Rise Time t_{TLH} = (1.35 ns/pF) C_L + 33 ns t_{TLH} = (0.60 ns/pF) C_L + 20 ns t_{TLH} = (0.40 ns/pF) C_L + 20 ns	t_{TLH}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time t_{THL} = (1.35 ns/pF) C_L + 33 ns t_{THL} = (0.60 ns/pF) C_L + 20 ns t_{THL} = (0.40 ns/pF) C_L + 20 ns	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time A or B to Q or Q t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 255 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 132 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 87 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	300 150 100	600 300 220	ns
$\overline{\text{Reset}}$ to Q or Q t_{PLH}, t_{PHL} = (0.90 ns/pF) C_L + 205 ns t_{PLH}, t_{PHL} = (0.36 ns/pF) C_L + 107 ns t_{PLH}, t_{PHL} = (0.26 ns/pF) C_L + 82 ns		5.0 10 15	– – –	250 125 95	500 250 190	ns
Input Rise and Fall Times Reset	t_r, t_f	5 10 15	– – –	– – –	15 5 4	μs
B Input		5 10 15	– – –	300 1.2 0.4	1.0 0.1 0.05	ms
A Input		5 10 15	No Limit			–
Input Pulse Width A, B, or Reset	t_{WH}, t_{WL}	5.0 10 15	170 90 80	85 45 40	– – –	ns
Retrigger Time	t_{rr}	5.0 10 15	0 0 0	– – –	– – –	ns
Output Pulse Width — Q or Q Refer to Figures 8 and 9 C_X = 0.002 μF, R_X = 100 kΩ	T	5.0 10 15	198 200 202	210 212 214	230 232 234	μs

C_X = 0.1 µF, R_X = 100 kΩ		5.0 10 15	9.3 9.4 9.5	9.86 10 10.14	10.5 10.6 10.7	ms
C_X = 10 µF, R_X = 100 kΩ		5.0 10 15	0.91 0.92 0.93	0.965 0.98 0.99	1.03 1.04 1.06	s
Pulse Width Match between circuits in the same package. C_X = 0.1 µF, R_X = 100 kΩ	100 $[(T_1 - T_2)/T_1]$	5.0 10 15	– – –	±1.0 ±1.0 ±1.0	±5.0 ±5.0 ±5.0	%

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

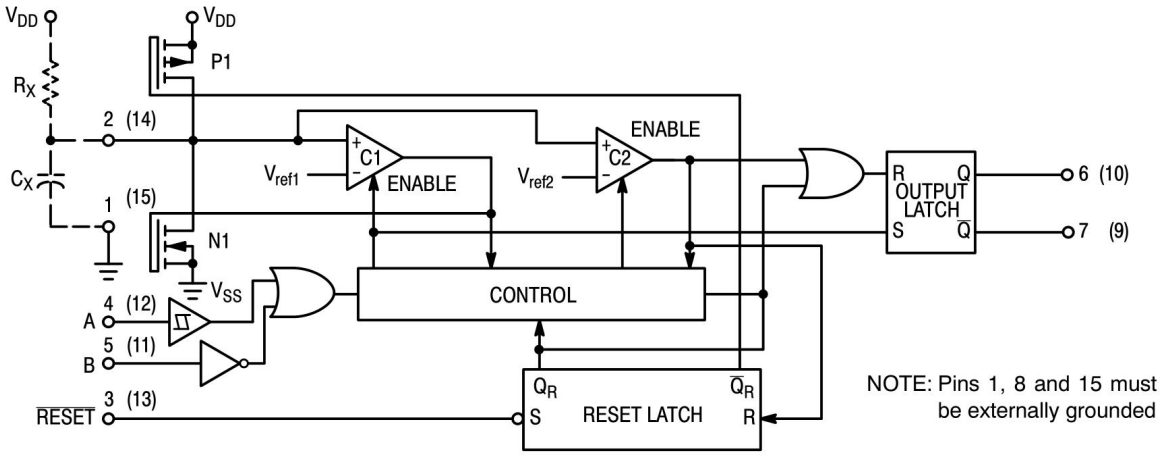


Figure 1. Logic Diagram (1/2 of Devlce Shown)

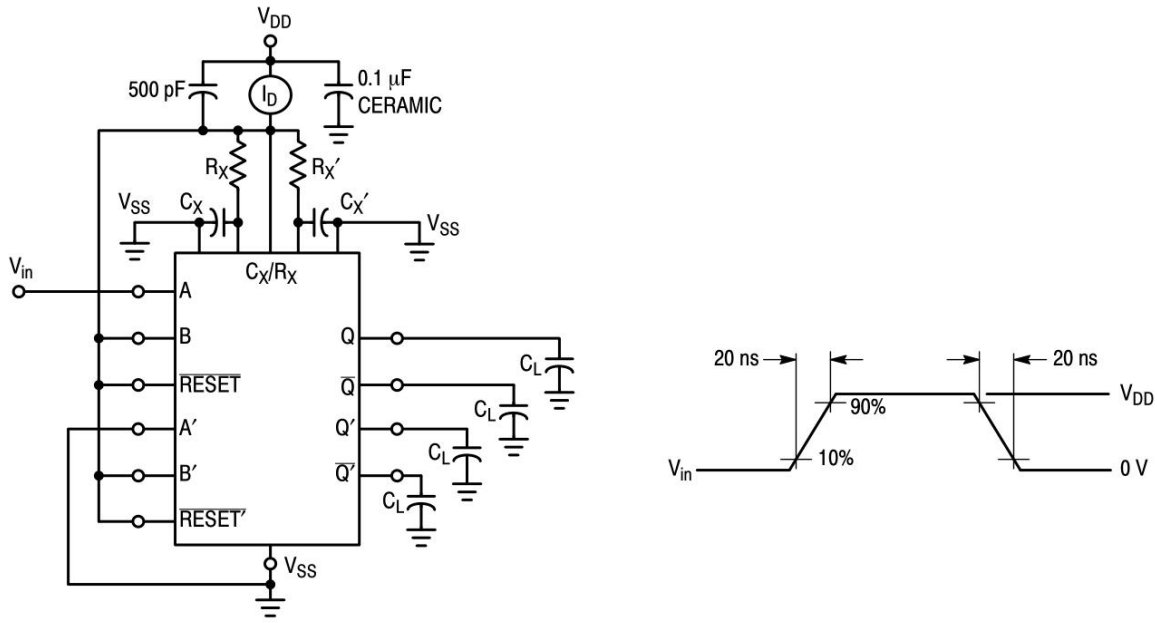
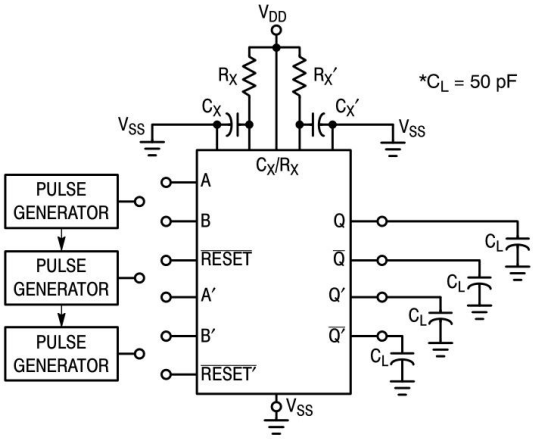


Figure 2. Power Dissipation Test Circuit and Waveforms



INPUT CONNECTIONS

Characteristics	$\overline{\text{Reset}}$	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, T, t_{WH}, t_{WL}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_{WH}, t_{WL}	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: Switching test waveforms for PG1, PG2, PG3 are shown In Figure 4.

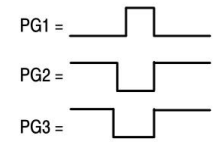


Figure 3. Switching Test Circuit

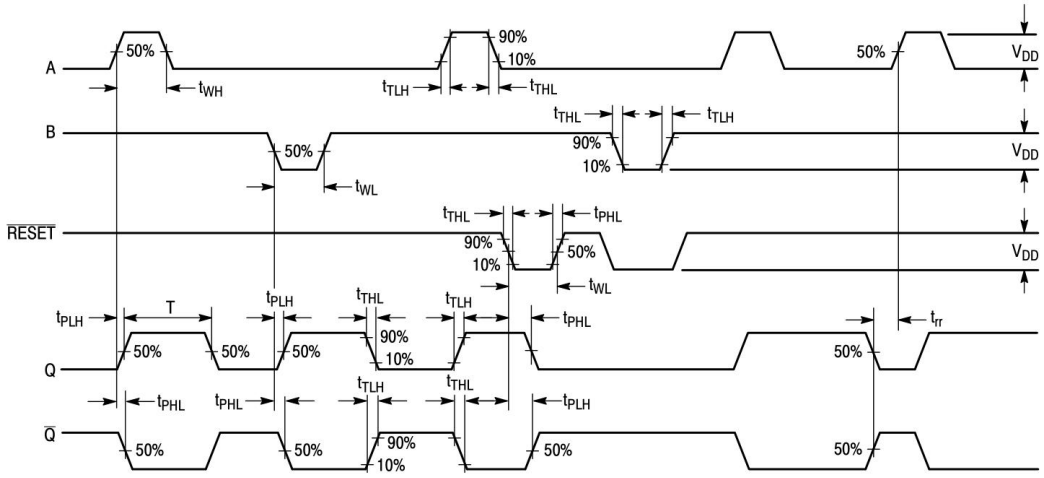


Figure 4. Switching Test Waveforms

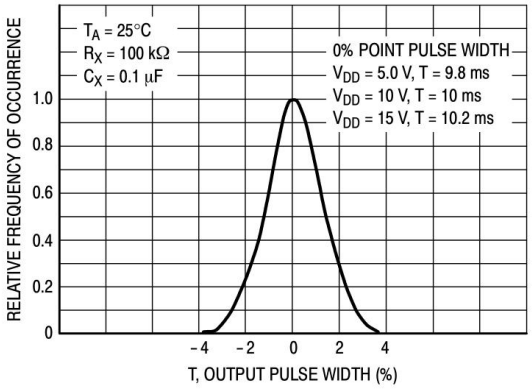


Figure 5. Typical Normalized Distribution of Units for Output Pulse Width

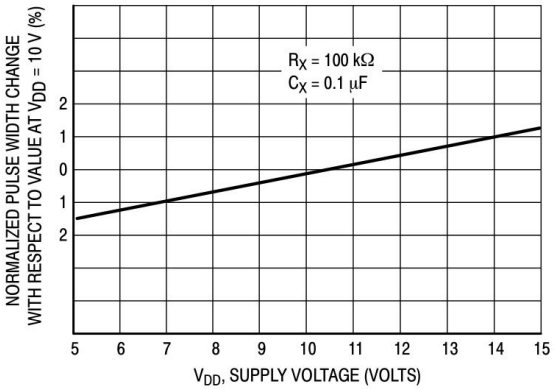


Figure 6. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

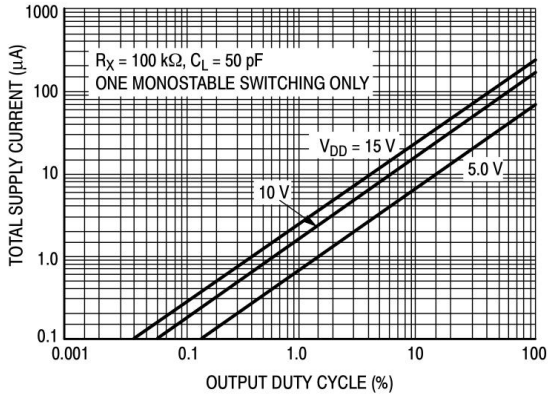


Figure 7. Typical Total Supply Current versus Output Duty Cycle

FUNCTION TABLE

Inputs			Outputs	
$\overline{\text{Reset}}$	A	B	Q	$\overline{\text{Q}}$
H	↑	H	⎍	⎓
H	L	↓	⎍	⎓
H	↑↓	L	Not Triggered	
H	H	↑↓	Not Triggered	
H	L, H, ↓	H	Not Triggered	
H	L	L, H, ↑	Not Triggered	
L	X	X	L	H
↓↑	X	X	Not Triggered	

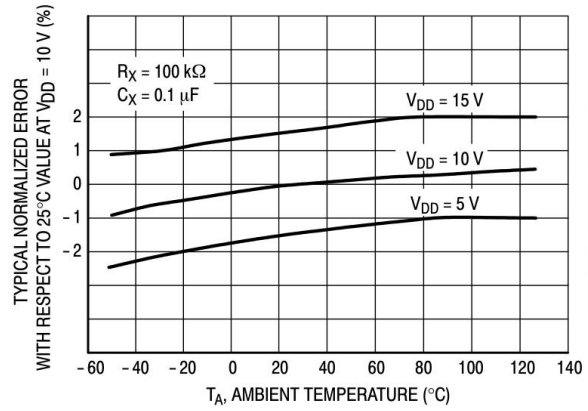


Figure 8. Typical Error of Pulse Width Equation versus Temperature

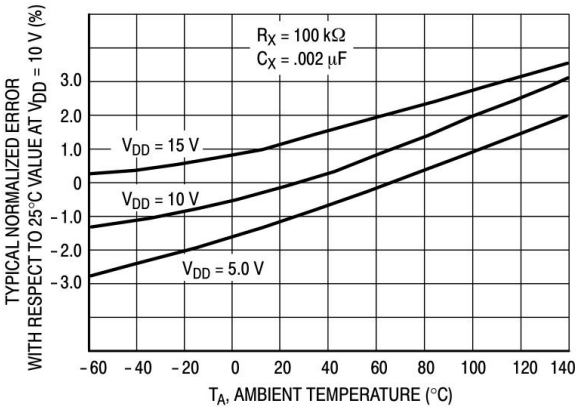


Figure 9. Typical Error of Pulse Width Equation versus Temperature

THEORY OF OPERATION

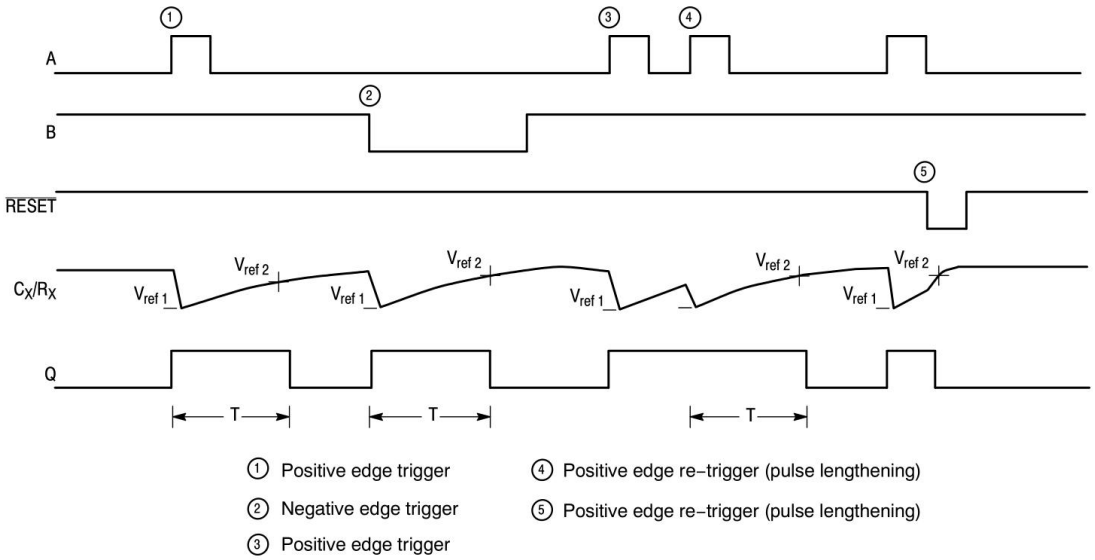


Figure 10. Timing Operation

TRIGGER OPERATION

The block diagram of the XD14538 is shown in Figure 1, with circuit operation following.

As shown in Figure 1 and 10, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and $\overline{Reset}$ are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N−channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{ref1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals $V_{ref\ 2}$, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2 ②. This ends at the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

In the quiescent state, CX is fully charged to VDD causing the current through resistor RX to be zero. Both comparators are “off” with total device current due only to reverse junction leakages. An added feature of the XD14538 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of CX, RX, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The XD14538 is retriggered if a valid trigger occurs ③ followed by another valid trigger ④before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref\ 1}$, but has not yet reached $V_{ref\ 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated
④, the voltage at C_X/R_X will again drop to $V_{ref\ 1}$ before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

RESET OPERATION

The XD14538 may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on $\overline{Reset}$ sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1 ⑤. When the voltage on the capacitor reaches $V_{ref\ 2}$, the reset latch will clear, and will then be ready to accept another pulse. It the $\overline{Reset}$ input is held low, any trigger inputs that occur will be inhibited and the Q and Q outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the $\overline{Reset}$ input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

POWER−DOWN CONSIDERATIONS

Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the XD14538 is powered down, the capacitor voltage may discharge from VDD through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the VDD supply must not be faster than (VDD). (C) / (10 mA). For example, if VDD = 10 V and CX = 10 μF, the VDD supply should discharge no faster than (10 V) x (10 μF) / (10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate. When a more rapid decrease of VDD to zero volts occurs, the XD14538 can sustain damage. To avoid this possibility use an external clamping diode, DX, connected as shown in Fig. 11.

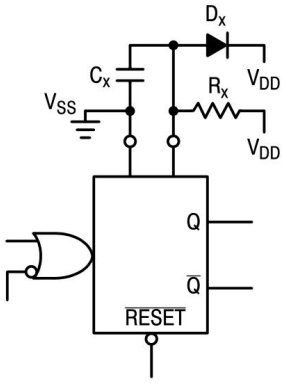


Figure 11. Use of a Diode to Limit Power Down Current Surge

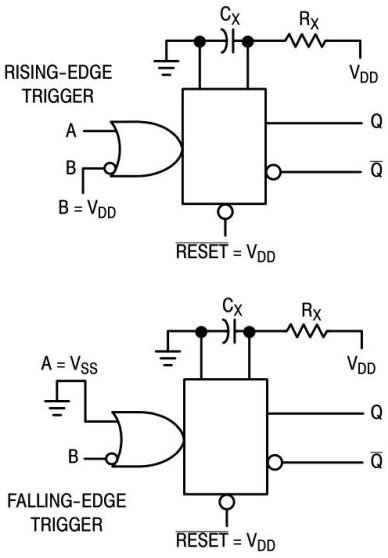


Figure 12. Retriggerable Monostables Circuitry

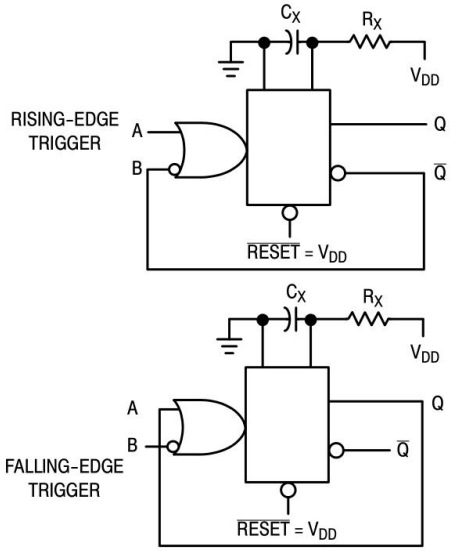


Figure 13. Non−Retriggerable Monostables Circuitry

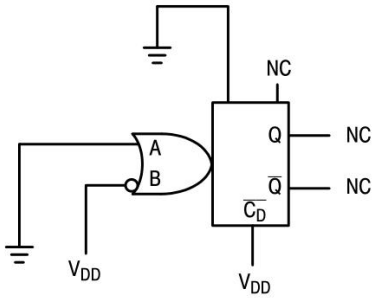


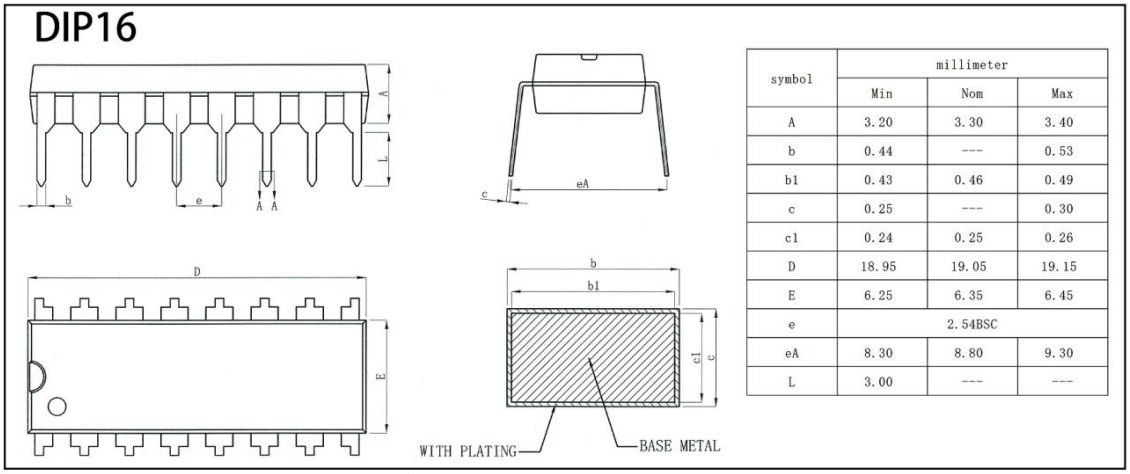
Figure 14. Connection of Unused Sections

9. ORDERING INFORMATION

Ordering Information

Part Number	Device Marking	Package Type	Body size (mm)	Temperature (°C)	MSL	Transport Media	Package Quantity
XD14538	XD14538	DIP16	19.05 * 6.35	- 40 to 85	MSL3	Tube 25	1000

10. DIMENSIONAL DRAWINGS



symbol	millimeter		
	Min	Nom	Max
A	3.20	3.30	3.40
b	0.44	---	0.53
b1	0.43	0.46	0.49
c	0.25	---	0.30
c1	0.24	0.25	0.26
D	18.95	19.05	19.15
E	6.25	6.35	6.45
e	2.54BSC		
eA	8.30	8.80	9.30
L	3.00	---	---