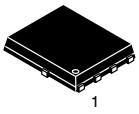
MOSFET – Power, Single N-Channel, DFN5/DFNW5

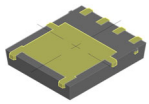
40 V, 130 A 2.5 mΩ

NVMFS5C442NL

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	2.5 mΩ @ 10 V	130 A
	3.7 mΩ @ 4.5 V	



DFN5 (SO−8FL)
CASE 488AA



DFNW5
(FULL−CUT SO8FL WF)
CASE 507BA

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C442NLWF − Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

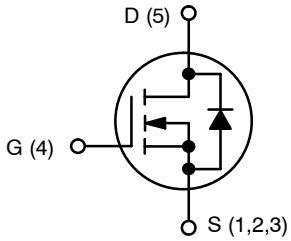
Symbol	Parameter			Value	Unit
V_{DSS}	Drain−to−Source Voltage			40	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	130	A
			T_C = 100°C	95	
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	83	W
			T_C = 100°C	42	
I_D	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	28	A
			T_A = 100°C	20	
P_D	Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	3.7	W
			T_A = 100°C	1.8	
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		900	A
T_J, T_{stg}	Operating Junction and Storage Temperature Range			−55 to +175	°C
I_S	Source Current (Body Diode)			81	A
E_{AS}	Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 10 A)			265	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

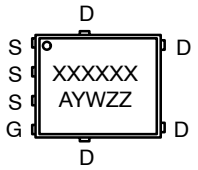
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction−to−Case − Steady State	1.8	°C/W
$R_{\theta JA}$	Junction−to−Ambient − Steady State (Note 2)	41	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



N−CHANNEL MOSFET

MARKING DIAGRAM



XXXXXX = 5C442L
(NVMFS5C442NL) or
442LWF
(NVMFS5C442NLWF)
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		40			V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient				24.8		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			10	μA
			T_J = 125°C			250	
		V_{GS} = 0 V, V_{DS} = 20 V, T_J = 125°C				20	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 90 μA		1.2		2.0	V
$V_{GS(TH)}/T_J$	Threshold Temperature Coefficient				−5.4		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V	I_D = 50 A		2.0	2.5	mΩ
		V_{GS} = 4.5 V	I_D = 50 A		2.9	3.7	
g_{FS}	Forward Transconductance	V_{DS} = 15 V, I_D = 50 A			116		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			3100		pF
C_{OSS}	Output Capacitance				1100		
C_{RSS}	Reverse Transfer Capacitance				37		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 4.5 V, V_{DS} = 32 V; I_D = 50 A			23		nC
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 32 V; I_D = 50 A			50		
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 4.5 V, V_{DS} = 32 V; I_D = 50 A			5.0		
Q_{GS}	Gate−to−Source Charge				9.8		
Q_{GD}	Gate−to−Drain Charge				6.7		
V_{GP}	Plateau Voltage				3.1		V
SWITCHING CHARACTERISTICS (Note 5)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = 4.5 V, V_{DS} = 32 V, I_D = 50 A, R_G = 1.0 Ω			12		ns
t_r	Rise Time				8.3		
$t_{d(OFF)}$	Turn−Off Delay Time				28		
t_f	Fall Time				9.4		
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.85	1.2	V
			T_J = 125°C		0.73		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 50 A			46		ns
t_a	Charge Time				23		
t_b	Discharge Time				23		
Q_{RR}	Reverse Recovery Charge				40		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

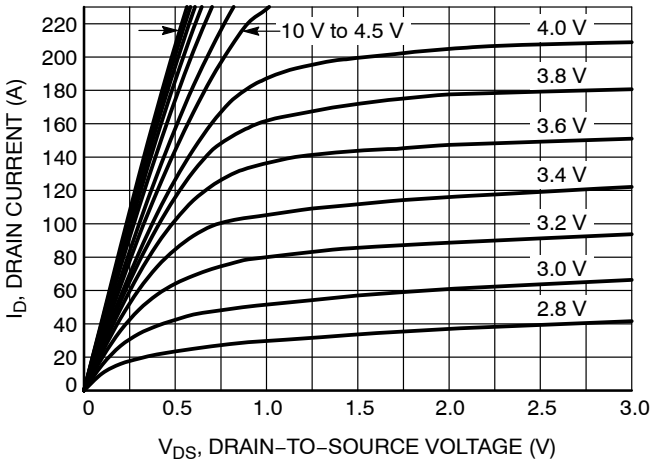


Figure 1. On−Region Characteristics

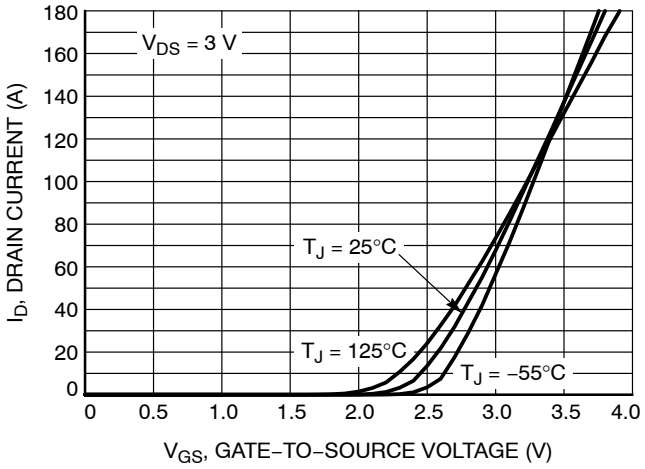


Figure 2. Transfer Characteristics

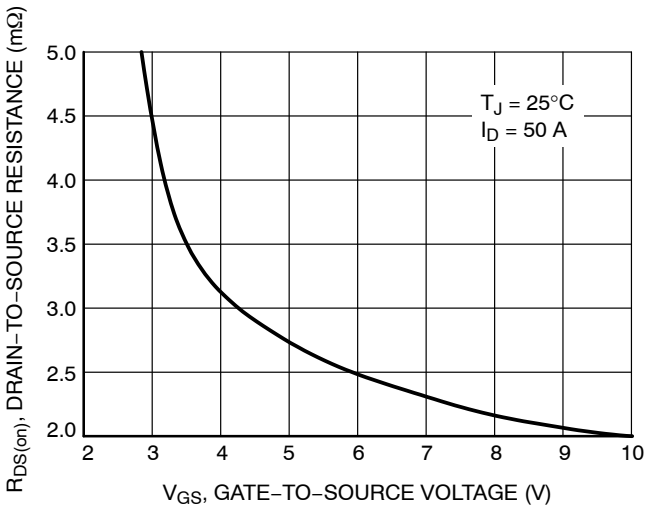


Figure 3. On−Resistance vs. Gate−to−Source Voltage

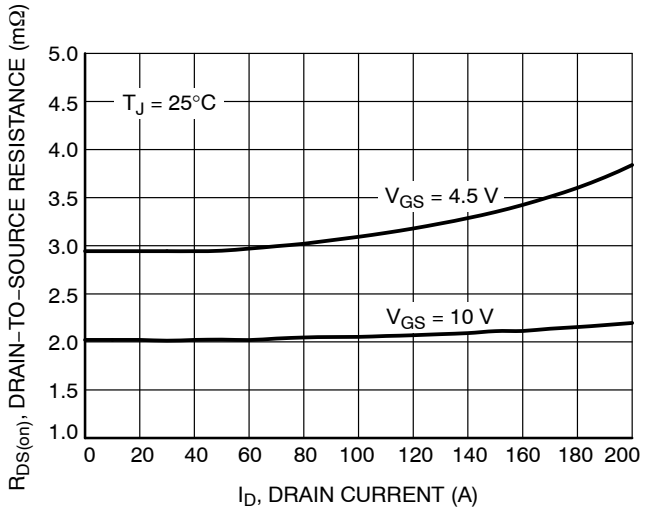


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

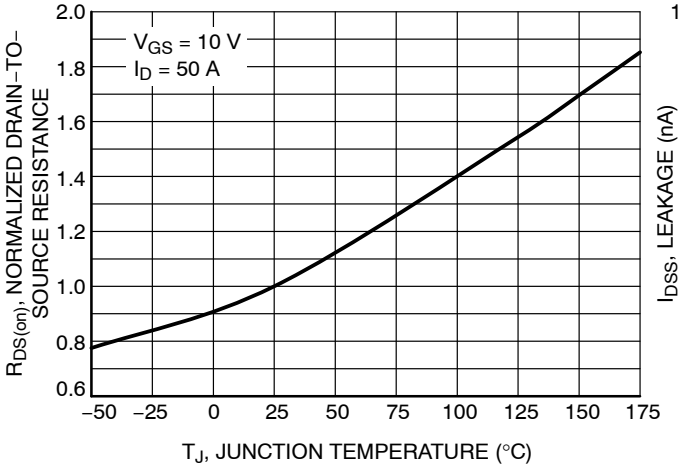


Figure 5. On−Resistance Variation with Temperature

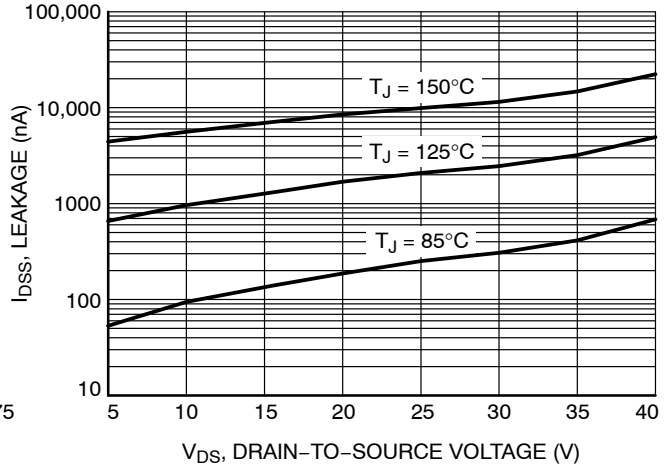


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

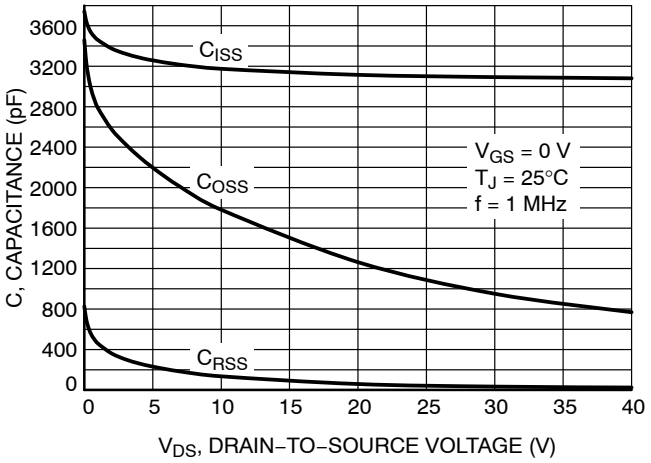


Figure 7. Capacitance Variation

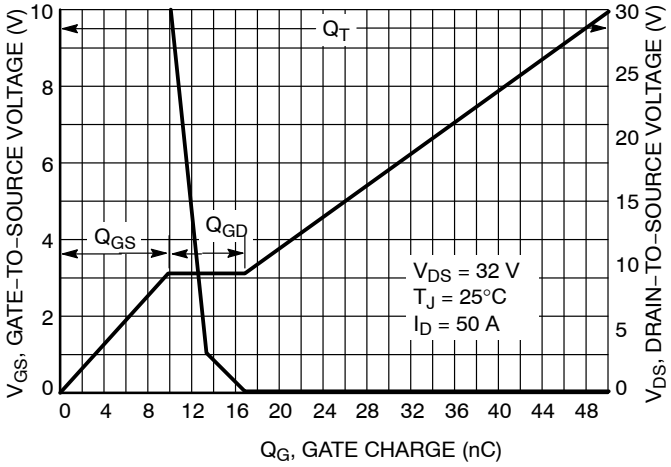


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

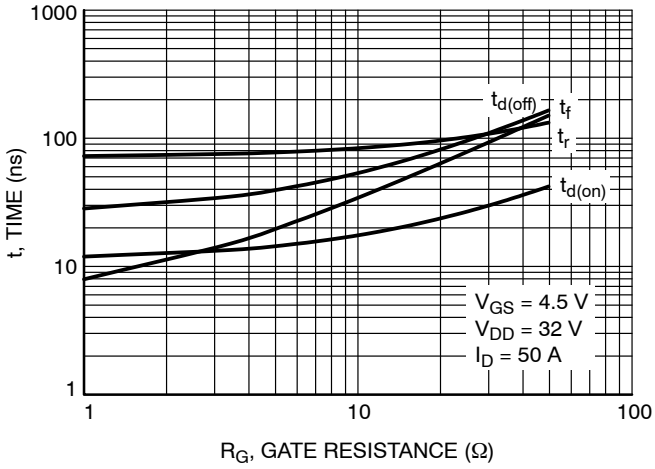


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

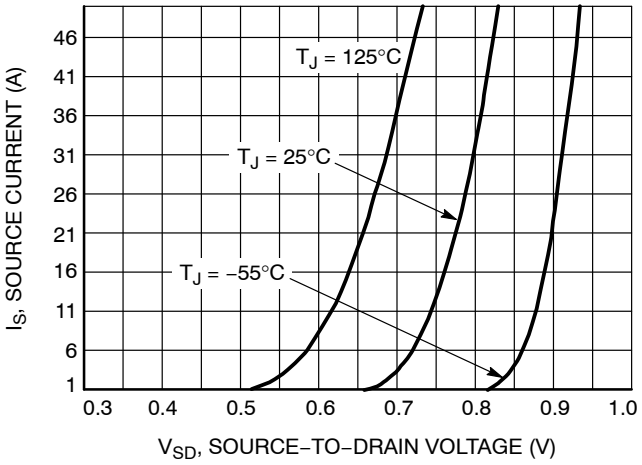


Figure 10. Diode Forward Voltage vs. Current

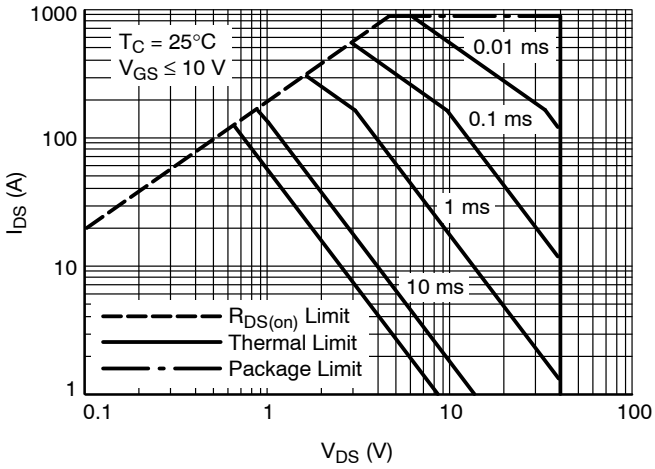


Figure 11. Safe Operating Area

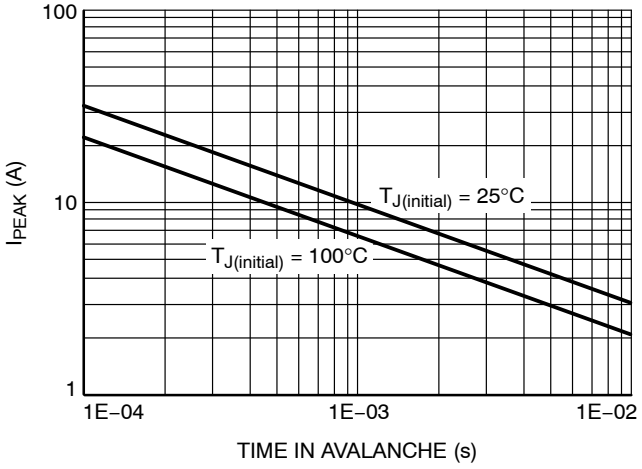


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

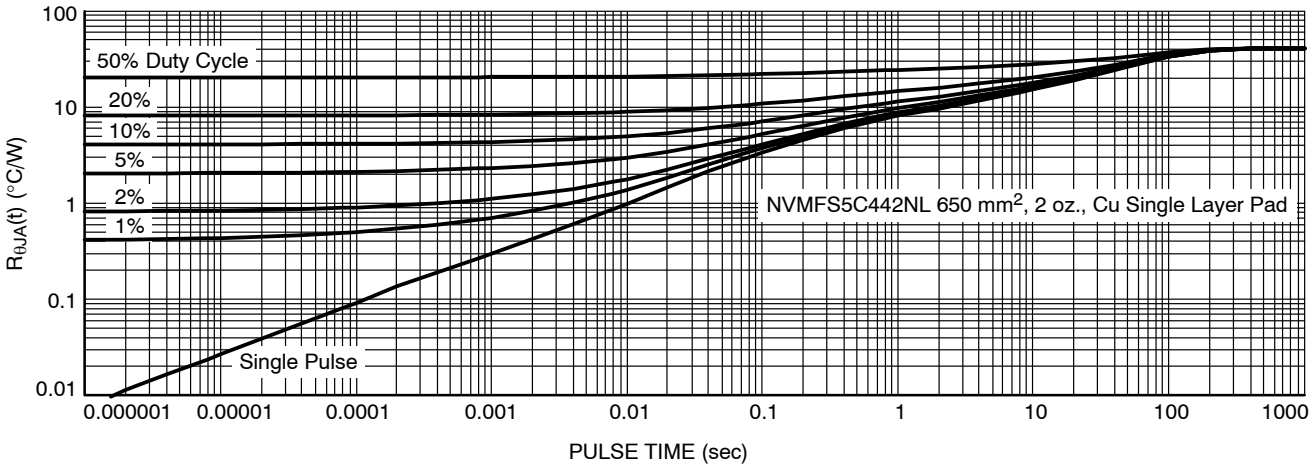


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NVMFS5C442NLWFT1G	442LWF	DFNW5 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C442NLT3G	5C442L	DFN5 (Pb−Free)	5000 / Tape & Reel
NVMFS5C442NLAFT1G	5C442L	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5C442NLAFT1G−YE	5C442L	DFN5 (Pb−Free)	1500 / Tape & Reel
NVMFS5C442NLWFAFT1G	442LWF	DFNW5 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C442NLWFET1G	442LWF	DFNW5 (Pb−Free, Wettable Flanks)	1500 / Tape & Reel
NVMFS5C442NLT1G	5C442L	DFN5 (Pb−Free)	1500 / Tape & Reel

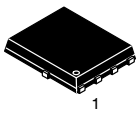
DISCONTINUED (Note 6)

NVMFS5C442NLWFT3G	442LWF	DFNW5 (Pb−Free, Wettable Flanks)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

6. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

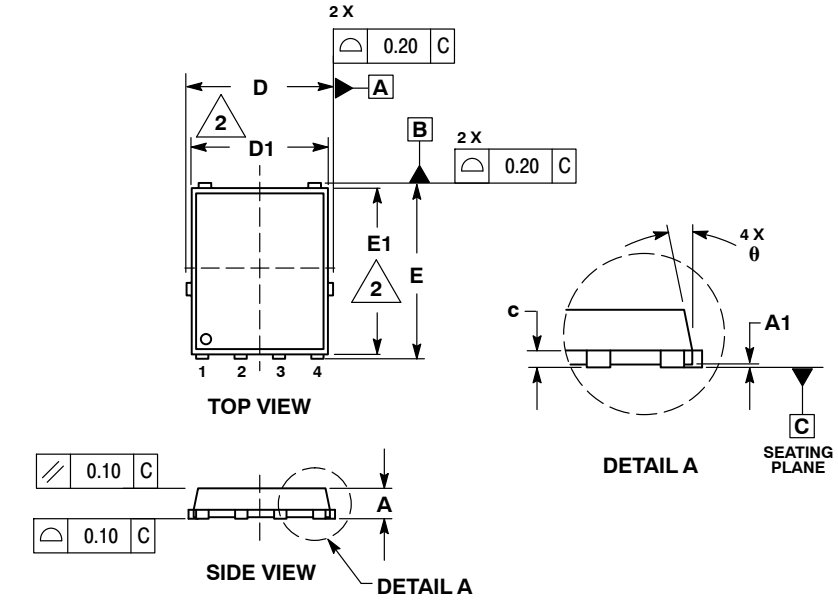
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 2:1

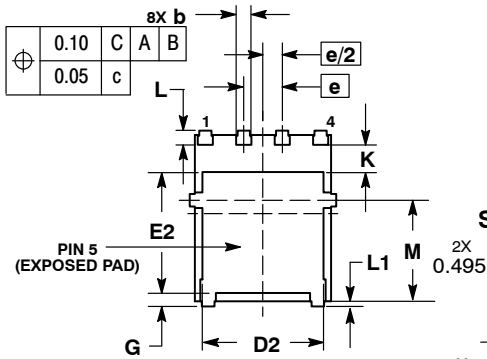
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

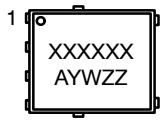


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °



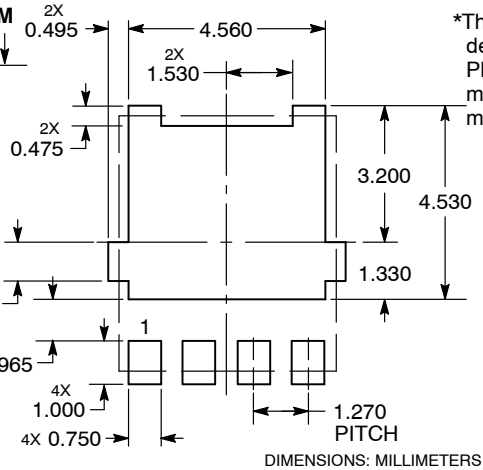
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



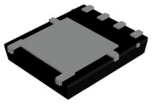
DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

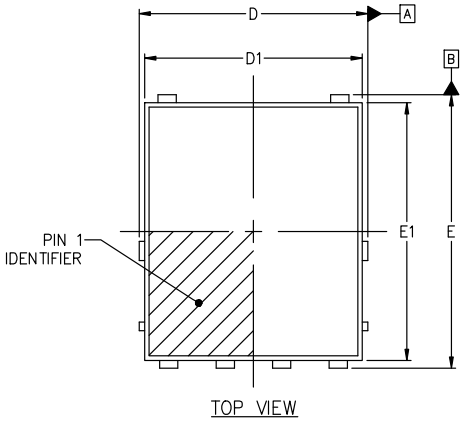
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

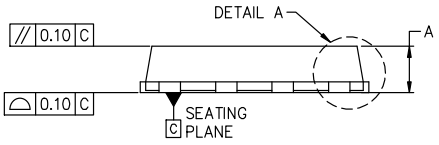
DOCUMENT NUMBER:	**98AON14036D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**	**PAGE 1 OF 1**

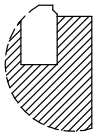


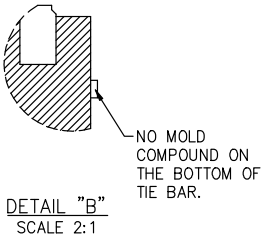
DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BE
ISSUE B

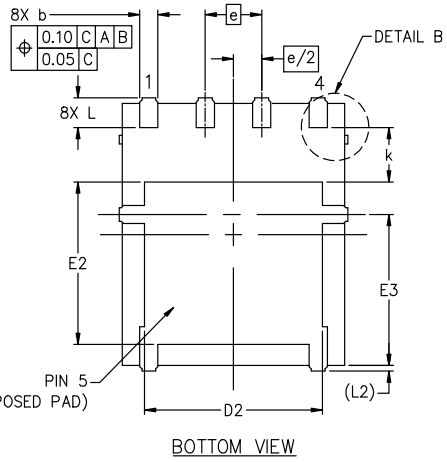
DATE 19 SEP 2024





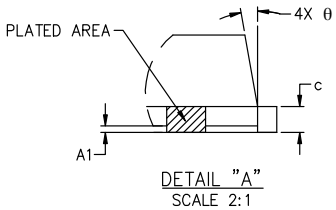




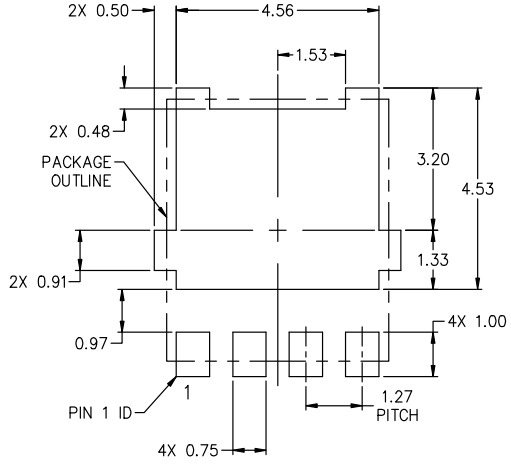


NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M−2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.

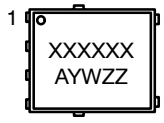


DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



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*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON33319H**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**DFNW5 4.90x5.90x1.00, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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