

PART NUMBER

SCAN18541T^MXA

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SCAN18541T Non-Inverting Line Driver with Tri-State Outputs

Check for Samples: [SCAN18541T](#)

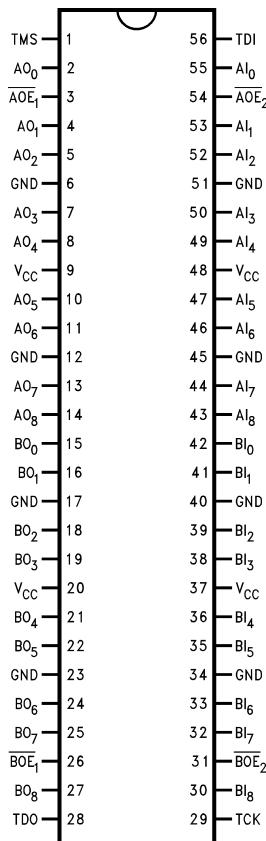
FEATURES

- IEEE 1149.1 (JTAG) Compliant
- Dual Output Enable Signals Per Byte
- Tri-State Outputs for Bus-Oriented Applications
- 9-bit Data Busses for Parity Applications
- Reduced-Swing Outputs Source 24 mA/Sink 48 mA (Mil)
- Ensured to Drive 50Ω Transmission Line to TTL Input Levels of 0.8V and 2.0V
- TTL Compatible Inputs
- 25 mil Pitch CLGA Packaging
- Includes CLAMP and HIGHZ Instructions
- Standard Microcircuit Drawing (SMD) 5962-9311601

DESCRIPTION

The SCAN18541T is a high speed, low-power line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented paired output enable control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Connection Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Pin Names

Pin Names	Description
AI ₍₀₋₈₎	Input Pins, A Side
BI ₍₀₋₈₎	Input Pins, B Side
AOE ₁ , AOE ₂	TRI-STATE Output Enable Input Pins, A Side
BOE ₁ , BOE ₂	TRI-STATE Output Enable Input Pins, B Side
AO ₍₀₋₈₎	Output Pins, A Side
AO ₍₀₋₈₎	Output Pins, B Side

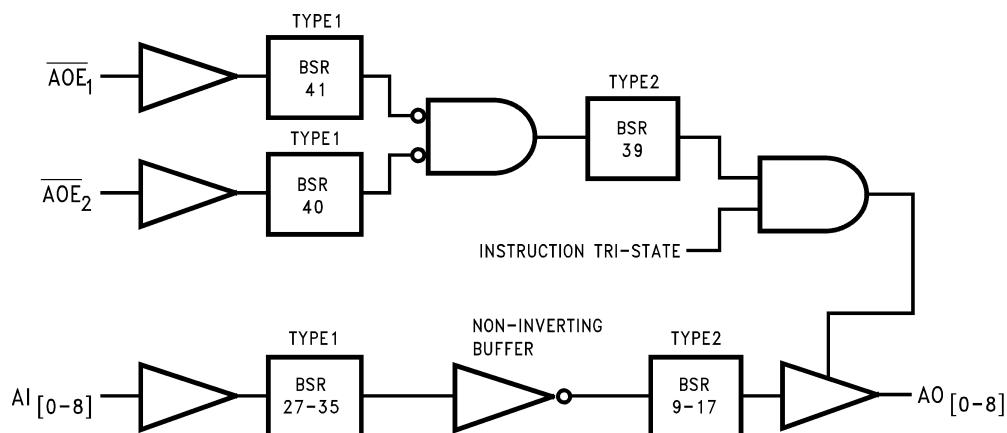
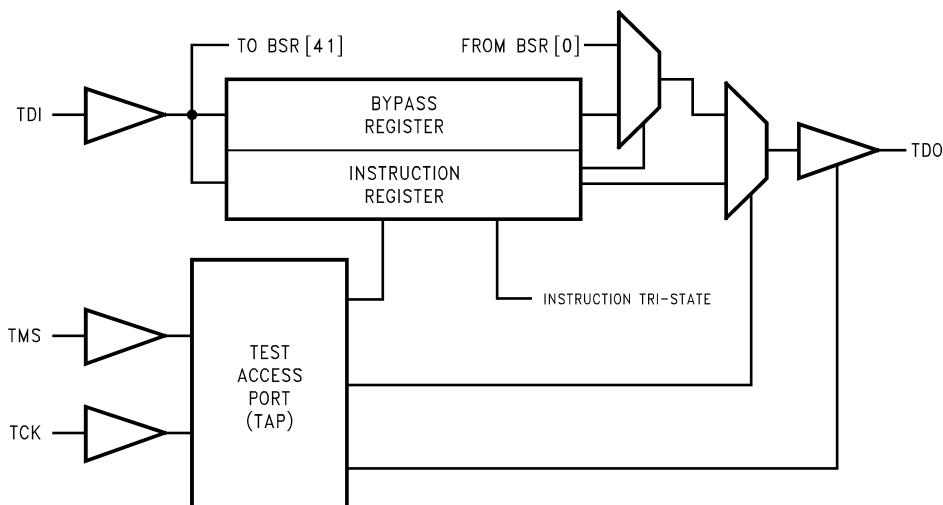
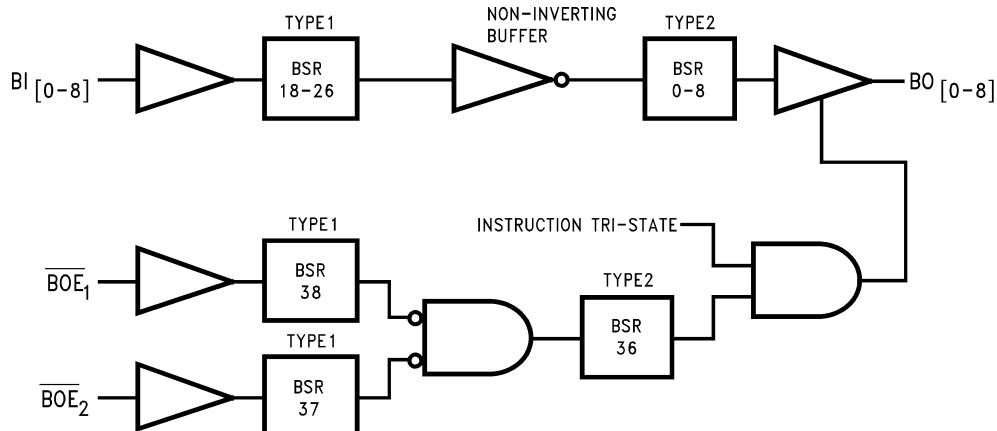
TRUTH TABLES

Inputs ⁽¹⁾			AO (0-8)
AOE ₁	AOE ₂	AI (0-8)	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

(1) H= HIGH Voltage Level
 L= LOW Voltage Level
 X= Immaterial
 Z= High Impedance

Inputs ⁽¹⁾			BO (0-8)
BOE ₁	BOE ₂	BI (0-8)	
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

(1) H= HIGH Voltage Level
 L= LOW Voltage Level
 X= Immaterial
 Z= High Impedance

BLOCK DIAGRAMS

Figure 1. Byte A

Figure 2. Tap Controller


Note: BSR stands for Boundary Scan Register.

Figure 3. Byte B

DESCRIPTION OF BOUNDARY-SCAN CIRCUITRY

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

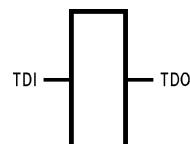


Figure 4. Bypass Register Scan Chain Definition Logic 0

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001. The two least significant bits of this captured value (01) are required by IEEE Std 1149.1. The upper six bits are unique to the SCAN18541T device. SCAN CMOS Test Access Logic devices do not include the IEEE 1149.1 optional identification register. Therefore, this unique captured value can be used as a “pseudo ID” code to confirm that the correct device is placed in the appropriate location in the boundary scan chain.

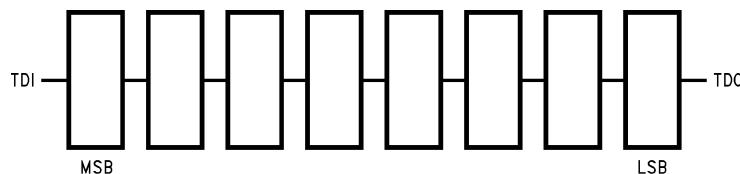


Figure 5. Instruction Register Scan Chain Definition

MSB→LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGH-Z
All Others	BYPASS

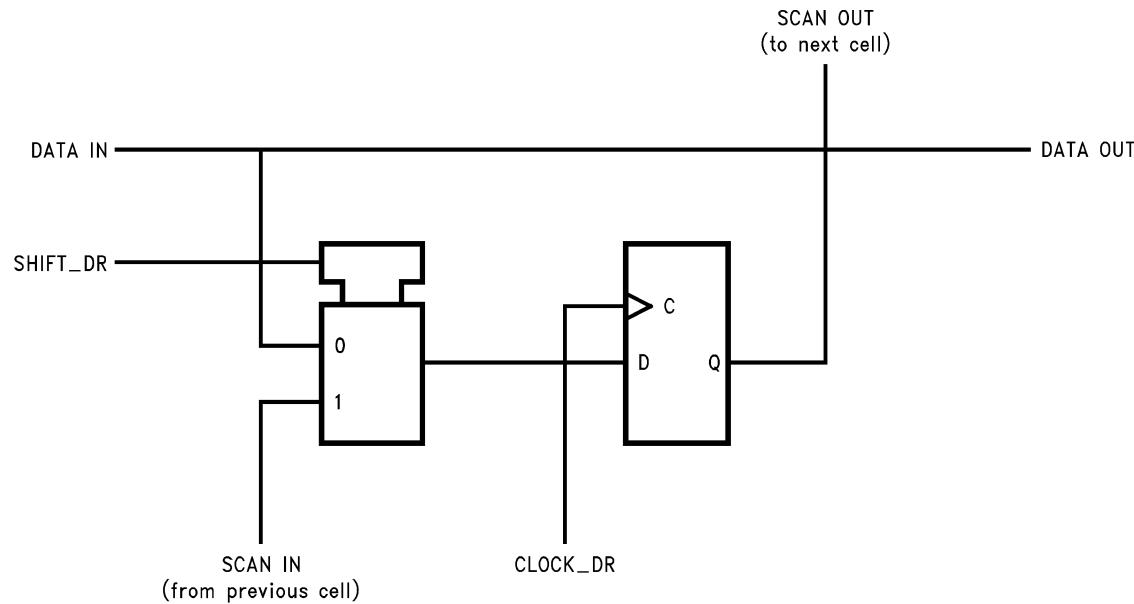


Figure 6. Scan Cell TYPE 1

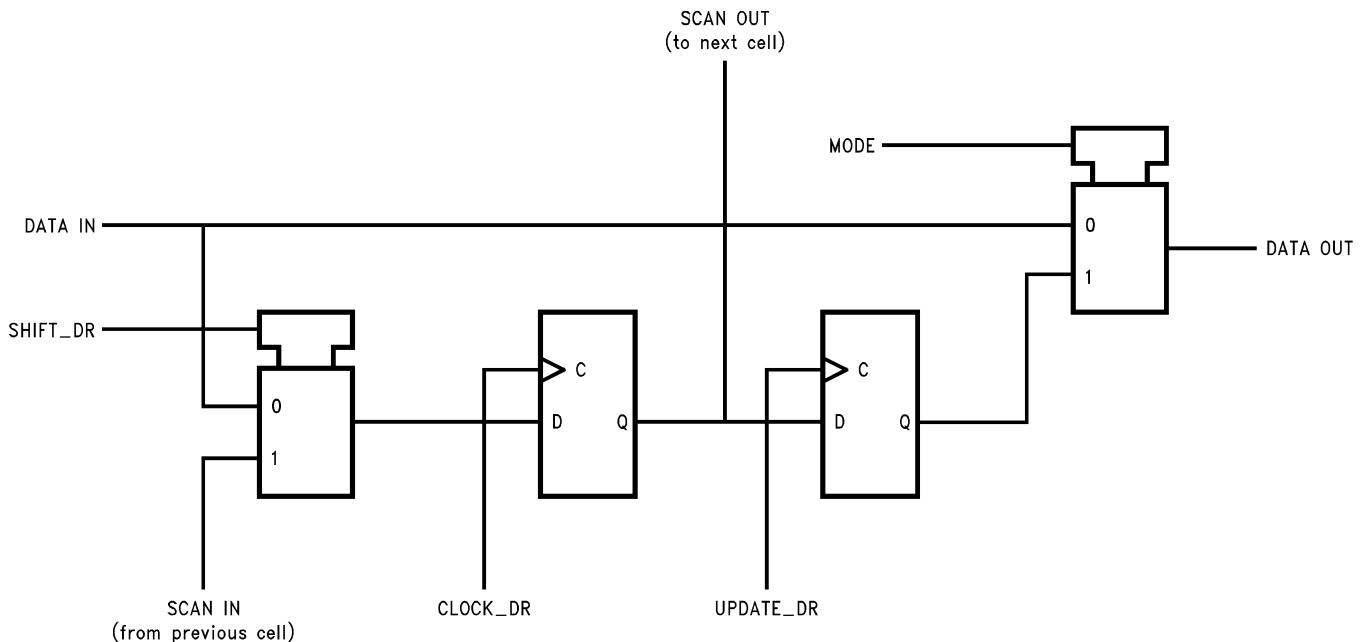


Figure 7. Scan Cell TYPE2

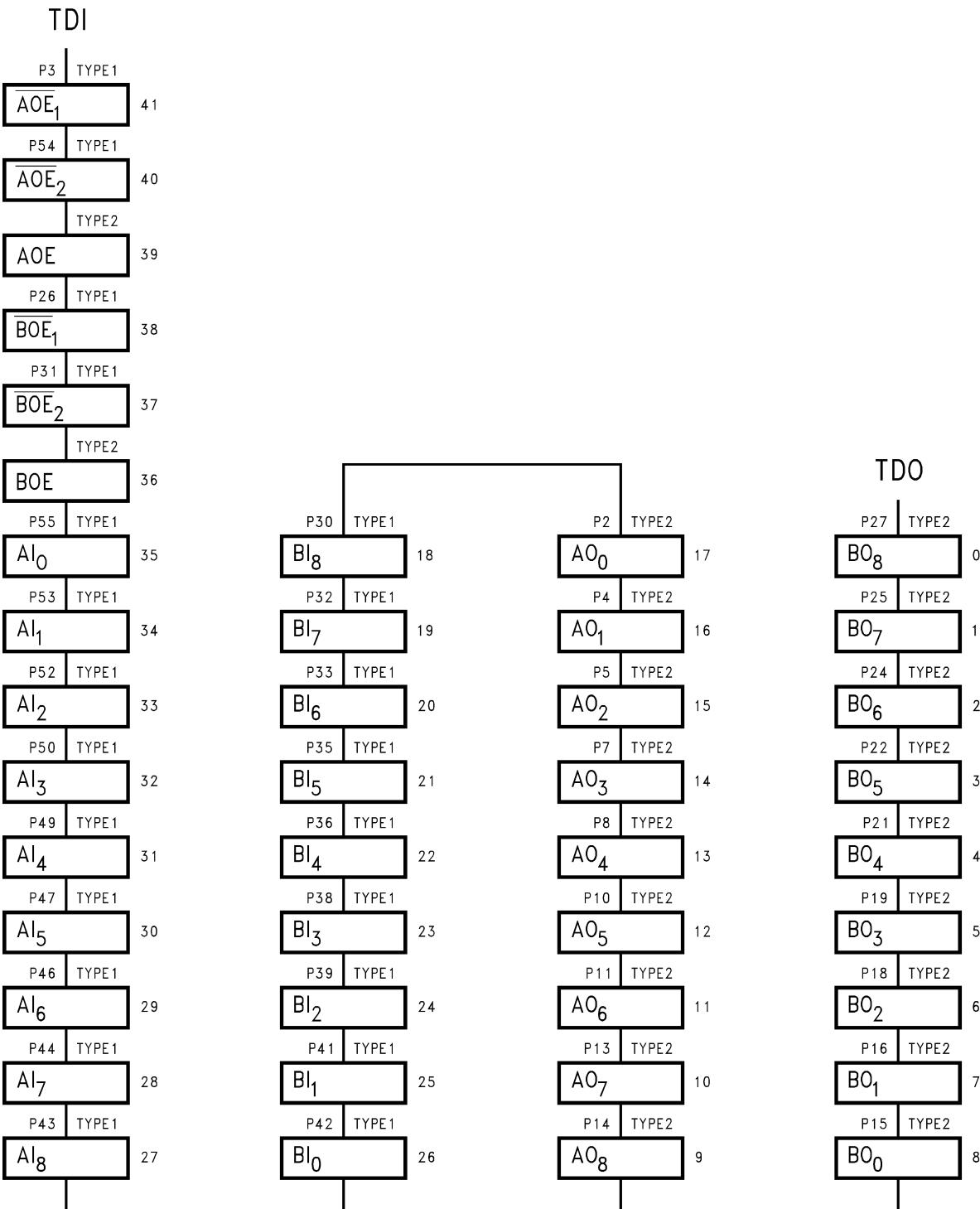


Figure 8. Boundary-Scan Register Scan Chain Definition (42 Bits in Length)

Boundary-Scan Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
41	\overline{AOE}_1	3	Input	TYPE1	Control Signals
40	\overline{AOE}_2	54	Input	TYPE1	
39	AOE		Internal	TYPE2	
38	\overline{BOE}_1	26	Input	TYPE1	
37	\overline{BOE}_2	31	Input	TYPE1	
36	BOE		Internal	TYPE2	
35	AI ₀	55	Input	TYPE1	A-in
34	AI ₁	53	Input	TYPE1	
33	AI ₂	52	Input	TYPE1	
32	AI ₃	50	Input	TYPE1	
31	AI ₄	49	Input	TYPE1	
30	AI ₅	47	Input	TYPE1	
29	AI ₆	46	Input	TYPE1	
28	AI ₇	44	Input	TYPE1	
27	AI ₈	43	Input	TYPE1	
26	BI ₀	42	Input	TYPE1	B-in
25	BI ₁	41	Input	TYPE1	
24	BI ₂	39	Input	TYPE1	
23	BI ₃	38	Input	TYPE1	
22	BI ₄	36	Input	TYPE1	
21	BI ₅	35	Input	TYPE1	
20	BI ₆	33	Input	TYPE1	
19	BI ₇	32	Input	TYPE1	
18	BI ₈	30	Input	TYPE1	
17	AO ₀	2	Output	TYPE2	A-out
16	AO ₁	4	Output	TYPE2	
15	AO ₂	5	Output	TYPE2	
14	AO ₃	7	Output	TYPE2	
13	AO ₄	8	Output	TYPE2	
12	AO ₅	10	Output	TYPE2	
11	AO ₆	11	Output	TYPE2	
10	AO ₇	13	Output	TYPE2	
9	AO ₈	14	Output	TYPE2	
8	BO ₀	15	Output	TYPE2	B-out
7	BO ₁	16	Output	TYPE2	
6	BO ₂	18	Output	TYPE2	
5	BO ₃	19	Output	TYPE2	
4	BO ₄	21	Output	TYPE2	
3	BO ₅	22	Output	TYPE2	
2	BO ₆	24	Output	TYPE2	
1	BO ₇	25	Output	TYPE2	
0	BO ₈	27	Output	TYPE2	



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS ⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		-0.5V to +7.0V
DC Input Diode Current (I_{IK})	$V_I = -0.5V$	-20 mA
	$V_I = V_{CC} + 0.5V$	+20 mA
DC Output Diode Current (I_{OK})	$V_O = -0.5V$	-20 mA
	$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)		-0.5V to $V_{CC} + 0.5V$
DC Output Source/Sink Current (I_O)		± 70 mA
DC V_{CC} or Ground Current	Per Output Pin	± 70 mA
Junction Temperature	CLGA	+175°C
Storage Temperature		-65°C to +150°C
ESD (Min)		2000V

(1) Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Texas Instruments does not recommend operation of SCAN circuits outside databook specifications.

(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

RECOMMENDED OPERATING CONDITIONS

Supply Voltage (V_{CC})	SCAN Products	4.5V to 5.5V
Input Voltage (V_I)		0V to V_{CC}
Output Voltage (V_O)		0V to V_{CC}
Operating Temperature (T_A)	Military	-55°C to +125°C
Minimum Input Edge Rate dV/dt	V_{IN} from 0.8V to 2.0V V_{CC} @ 4.5V, 5.5V	125 mV/ns

DC ELECTRICAL CHARACTERISTICS

All outputs loaded; thresholds associated with output under test.

Symbol	Parameter	V_{CC} (V)	Military	Units	Conditions
			$T_A = -55^\circ C$ to $+125^\circ C$		
			Specified Limits		
V_{IH}	Minimum High Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$
		5.5	2.0		or $V_{CC} - 0.1V$
V_{IL}	Maximum Low Input Voltage	4.5	0.8	V	$V_{OUT} = 0.1V$
		5.5	0.8		or $V_{CC} - 0.1V$
V_{OH}	Minimum High Output Voltage	4.5	3.15	V	$I_{OUT} = -50 \mu A$
		5.5	4.15		
		4.5	2.4		$V_{IN} = V_{IL}$ or V_{IH}
		5.5	2.4		$I_{OH} = -24 mA$
V_{OL}	Maximum Low Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.55		$V_{IN} = V_{IL}$ or V_{IH}
		5.5	0.55		$I_{OL} = 48 mA$
I_{IN}	Maximum Input Leakage Current	5.5	± 1.0	μA	$V_I = V_{CC}$, GND
I_{IN} TDI, TMS	Maximum Input Leakage	5.5	3.7	μA	$V_I = V_{CC}$
			-385		$V_I = GND$
	Minimum Input Leakage	5.5	-160	μA	$V_I = GND$

DC ELECTRICAL CHARACTERISTICS (continued)

All outputs loaded; thresholds associated with output under test.

Symbol	Parameter	V _{CC} (V)	Military		Units	Conditions		
			T _A = -55°C to +125°C					
			Specified Limits					
I _{OLD}	Minimum Dynamic ⁽¹⁾	5.5	63	mA	V _{OLD} = 0.8V Max			
I _{OHD}	Output Current		-27	mA	V _{OHD} = 2.0V Min			
I _{OZ}	Maximum Output Leakage Current	5.5	±10.0	µA	V _I (OE) = V _{IL} , V _{IH}			
I _{OS}	Output Short Circuit Current	5.5	-100	mA (min)	V _O = 0V			
I _{CC}	Maximum Quiescent Supply Current	5.5	168	µA	V _O = Open TDI, TMS = V _{CC}			
		5.5	930	µA	V _O = Open TDI, TMS = GND			
I _{CCt}	Maximum I _{CC} Per Input	5.5	2.0	mA	V _I = V _{CC} -2.1V			
		5.5	2.15	mA	V _I = V _{CC} -2.1V TDI/TMS Pin, Test One with the Other Floating			

(1) Maximum test duration 2.0 ms, one output loaded at a time.

NOISE SPECIFICATIONS

Symbol	Parameter	V _{CC} (V)	Military		Units	Fig. No.		
			T _A = -55°C to +125°C					
			Specified Limits					
V _{OLP}	Maximum High Output Noise ⁽¹⁾⁽²⁾	5.0	0.8		V			
V _{OLV}	Minimum Low Output Noise ⁽¹⁾⁽²⁾	5.0	-0.8		V			

(1) Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched LOW and one output held LOW.

(2) Maximum number of outputs that can switch simultaneously is n. (n-1) outputs are switched HIGH and one output held HIGH.

AC ELECTRICAL CHARACTERISTICS

Normal Operation

Symbol	Parameter	V _{CC} (V) ⁽¹⁾	Military		Units	Fig. No.		
			T _A = -55°C to +125°C C _L = 50 pF					
			Min	Max				
t _{PLH} , t _{PHL}	Propagation Delay Data to Q	5.0	2.5 2.5	10.5 10.5	ns			
t _{PZL} , t _{PHZ}	Disable Time	5.0	1.5 1.5	11.2 11.2	ns			
t _{PZL} , t _{PHZ}	Enable Time	5.0	2.0 2.0	14.0 12.0	ns			

(1) Voltage Range 5.0 is 5.0V ±0.5V.

AC ELECTRICAL CHARACTERISTICS

Scan Test Operation

All Propagation Delays involving TCK are measured from the falling edge of TCK.

Symbol	Parameter	V _{CC} (V) ⁽¹⁾	Military		Units	Fig. No.		
			T _A = -55°C to +125°C C _L = 50 pF					
			Min	Max				
t _{PLH} , t _{PHL}	Propagation Delay TCK to TDO	5.0	3.5 3.5	15.8 15.8	ns			
t _{PLZ} , t _{PHZ}	Disable Time TCK to TDO	5.0	2.5 2.5	13.2 13.2	ns			
t _{PZL} , t _{PZH}	Enable Time TCK to TDO	5.0	3.0 3.0	17.0 17.0	ns			
t _{PLH} , t _{PHL}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0	21.7 21.7	ns			
t _{PLH} , t _{PHL}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0	21.2 21.2	ns			
t _{PLH} , t _{PHL}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.5 5.5	23.0 23.0	ns			
t _{PLZ} , t _{PHZ}	Propagation Delay TCK to Data Out During Update-DR State	5.0	4.0 4.0	19.6 19.6	ns			
t _{PLZ} , t _{PHZ}	Propagation Delay TCK to Data Out During Update-IR State	5.0	5.0 5.0	22.4 22.4	ns			
t _{PLZ} , t _{PHZ}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	5.0 5.0	23.3 23.3	ns			
t _{PZL} , t _{PZH}	Propagation Delay TCK to Data Out During Update-DR State	5.0	5.0 5.0	22.6 22.6	ns			
t _{PZL} , t _{PZH}	Propagation Delay TCK to Data Out During Update-IR State	5.0	6.5 6.5	26.2 26.2	ns			
t _{PZL} , t _{PZH}	Propagation Delay TCK to Data Out During Test Logic Reset State	5.0	7.0 7.0	27.4 27.4	ns			

(1) Voltage Range 5.0 is 5.0V $\pm 0.5V$.

AC OPERATING REQUIREMENTS

Scan Test Operation

Symbol	Parameter	V _{CC} (V) ⁽¹⁾	Military		Units	Fig. No.		
			T _A = -55°C to +125°C C _L = 50 pF					
			Specified Minimum					
t _S	Setup Time, H or L Data to TCK ⁽²⁾	5.0	3.0		ns			
t _H	Hold Time, H or L TCK to Data ⁽²⁾	5.0	5.0		ns			
t _S	Setup Time, H or L AOE _n , BOE _n to TCK ⁽³⁾	5.0	3.0		ns			
t _H	Hold Time, H or L	5.0	4.5		ns			
	TCK to AOE _n ,							
	BOE _n ⁽³⁾							
t _S	Setup Time, H or L Internal AOE, BOE, to TCK ⁽⁴⁾	5.0	3.0		ns			
t _H	Hold Time, H or L TCK to Internal AOE, BOE ⁽⁴⁾	5.0	3.0		ns			
t _S	Setup Time, H or L TMS to TCK	5.0	8.0		ns			
t _H	Hold Time, H or L TCK to TMS	5.0	2.0		ns			
t _S	Setup Time, H or L TDI to TCK	5.0	4.0		ns			
t _H	Hold Time, H or L TCK to TDI	5.0	4.5		ns			
t _W	Pulse Width TCK	H L	5.0	12.0 5.0	ns			
f _{max}	Maximum TCK	5.0	25		MHz			
	Clock Frequency							
T _{PU}	Wait Time, Power Up to TCK	5.0	100		ns			
T _{DN}	Power Down Delay	0.0	100		ms			

(1) Voltage Range 5.0 is 5.0V $\pm 0.5V$. All Input Timing Delays involving TCK are measured from the rising edge of TCK.

(2) This delay represents the timing relationship between the data input and TCK at the associated scan cells numbered 0-8, 9-17, 18-26 and 27-35.

(3) Timing pertains to BSR 37, 38, 40 and 41 only.

(4) This delay represents the timing relationship between AOE/BOE and TCK for scan cells 36 and 39 only.

CAPACITANCE

Symbol	Parameter	Max	Units	Conditions
C _{IN}	Input Pin Capacitance	5.0	pF	V _{CC} = 5.0V
C _{OUT}	Output Pin Capacitance	15.0	pF	V _{CC} = 5.0V
C _{PD}	Power Dissipation Capacitance	35.0	pF	V _{CC} = 5.0V

REVISION HISTORY

Changes from Revision A (April 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	11

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