Rochester Electronics

Datasheet

PART NUMBER

MD8253^BJA

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R055-93. - JT	92-12-21	Monica L. Poelking
B	Changes in accordance with NOR 5962-R021-99. – LTG	00-10-05	Monica L. Poelking
C	Modify paragraphs 3.1 and 3.5.1 to allow product to be marked with “QD” certification mark. Update boilerplate. – TVN	00-10-05	Monica L. Poelking
D	Update boilerplate to MIL-PRF-38535 requirements. – CFS	05-09-07	Thomas M. Hess
E	Update boilerplate to MIL-PRF-38535 requirements. – PHN	19-07-26	Thomas M. Hess

THE ORIGINAL FIRST SHEET OF THIS SMD HAS BEEN REPLACED.

REV																			
SHEET																			
REV	E																		
SHEET	15																		

REV STATUS OF SHEETS																
REV	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E	E
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A	PREPARED BY Ray Monnin	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **https://www.dla.mil/landandmaritime**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Da Di Cenzo	
	APPROVED BY N. A. Hauck	MICROCIRCUIT, PROGRAMMABLE INTERVAL TIMER, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 87-06-22	
	REVISION LEVEL **E**	SIZE **A** / CAGE CODE **67268** / **5962-87520** SHEET 1 OF 15

1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-87520	01	J	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type 1/	Generic number	Circuit function
01	8253	Programmable interval timer
02	8253	Programmable interval timer
03	8253-5	Programmable interval timer

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage range ..... -0.5 V dc to +7.0 V dc
Input voltage range with respect to ground (any pin) ..... -0.5 V dc to +7.0 V dc
Maximum power dissipation (P_D) ..... 1.0 W
Storage temperature range ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds) ..... +270°C
Thermal resistance, junction-to-case (θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +150°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... 5.0 V dc
Minimum high level input voltage (V_{IH}) ..... 2.2 V dc
Minimum low level input voltage (V_{IL}) ..... -0.5 V dc
Maximum high level input voltage (V_{IH}) ..... V_{CC} + 0.5 V dc
Maximum low level input voltage (V_{IL}) ..... 0.7 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Device types 01 and 02 are equivalent.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at https://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used. This drawing has been modified to allow the manufacturer to use the alternate die/fabrication requirements of paragraph A.3.2.2 of MIL-PRF-38535 or other alternative approved by the Qualifying Activity.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figures 4 and 5.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.5.1 Certification/compliance mark. A compliance indicator “C” shall be marked on all non-JAN devices built in compliance to MIL-PRF-38535, appendix A. The compliance indicator “C” shall be replaced with a "Q" or "QML" certification mark in accordance with MIL-PRF-38535 to identify when the QML flow option is used. For product built in accordance with A.3.2.2 of MIL-PRF-38535, or as modified in the manufacturer’s QM plan, the “QD” certification mark shall be used in place of the "Q" or "QML" certification mark.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DLA Land and Maritime -VA shall be required for any change that affects this drawing.

3.9 Verification and review. DLA Land and Maritime, DLA Land and Maritime's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	V_{CC} = 5 V ±10%	All	1, 2, 3		0.7	V
Input high voltage	V_{IH}	V_{CC} = 5 V ±10%	All	1, 2, 3	2.2		V
Output low voltage	V_{OL}	V_{CC} = 5 V ±10%, I_{OL} = 1.6 mA	All	1, 2, 3		0.45	V
Output high voltage	V_{OH}	V_{CC} = 5 V ±10%, I_{OH} = -150 µA	All	1, 2, 3	2.4		V
Input load current	I_{IL}	V_{CC} = 5.5 V V_{IN} = V_{CC} to 0.0 V	All	1, 2, 3		±20	µA
Output float leakage	I_{OFL}	V_{CC} = 5.5 V V_{OUT} = V_{CC} to 0.0 V	All	1, 2, 3		±20	µA
V_{CC} supply current 1/	I_{CC}	V_{CC} = 5.5 V Outputs unloaded static	All	1, 2, 3		160	mA
Input capacitance	C_{IN}	f_C = 1 MHz, T_A = 25°C V_{CC} = GND = 0.0 V See 4.3.1d	All	4		10	pF
Input/Output capacitance	$C_{I/O}$	T_A = 25°C V_{CC} = GND = 0.0 V Unmeasured pins returned to V_{SS} See 4.3.1d	All	4		20	pF
Functional test		See 4.3.1c	All	7, 8			
Address stable before $\overline{RD}$	t_{AR}	See figures 4 and 5 2/	01, 02	9, 10, 11	50		ns
			03		30		
Address hold time for $\overline{RD}$	t_{RA}		All	9, 10, 11	5		ns
$\overline{RD}$ pulse width 3/	t_{RR}		01, 02	9, 10, 11	400		ns
			03		300		
Data delay from $\overline{RD}$ 4/	t_{RD}		01, 02	9, 10, 11		300	ns
			03			200	
$\overline{RD}$ to data floating 5/	t_{DF}		01, 02	9, 10, 11	25	125	ns
			03		25	100	
Recovery time between $\overline{RD}$ and any other control signal 5/	t_{RV}		All	9, 10, 11	1		µs

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Address stable before $\overline{WR}$	t_{AW}	See figures 4 and 5 2/	01, 02	9, 10, 11	50		ns
			03		30		
Address hold time for $\overline{WR}$	t_{WA}		All	9, 10, 11	30		ns
$\overline{WR}$ pulse width 3/	t_{WW}		01, 02	9, 10, 11	400		ns
			03		300		
Data setup time for $\overline{WR}$	t_{DW}		01, 02	9, 10, 11	300		ns
			03		250		
Data hold time for $\overline{WR}$	t_{WD}		01, 02	9, 10, 11	40		ns
			03		30		
Recovery time between $\overline{WR}$ and any other control signal 5/	t_{RV}		All	9, 10, 11	1		µs
Clock period	t_{CLK}		All	9, 10, 11	380	DC 5/	ns
High pulse width	t_{PWH}		All	9, 10, 11	230		ns
Low pulse width	t_{PWL}		All	9, 10, 11	150		ns
Gate width high	t_{GW}		All	9, 10, 11	150		ns
Gate width low 5/	t_{GL}		All	9, 10, 11	100		ns
Gate setup to CLK high	t_{GS}		All	9, 10, 11	100		ns
Gate hold after CLK high	t_{GH}		All	9, 10, 11	55		ns
Output delay from CLK low 4/	t_{OD}		All	9, 10, 11		400	ns
Output delay from gate low 4/	t_{ODG}		All	9, 10, 11		300	ns

1/ I_{CC} is measured in a static condition with no output loads applied.

2/ Test conditions: $V_{IL} = 0.45\ V$, $V_{IH} = 2.4\ V$
$V_{OL} = 0.8\ V$, $V_{OH} = 2.2\ V$

3/ If clock low occurs less than 100 ns after the rising edge of READ or WRITE, the counter selected during the READ or WRITE could be affected.

4/ Test condition: $C_L = 100\ pF$.

5/ Guaranteed if not tested.

Device type	All		
Case outline	J		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D7	13	OUT1
2	D6	14	GATE1
3	D5	15	CLK1
4	D4	16	GATE2
5	D3	17	OUT2
6	D2	18	CLK2
7	D1	19	A0
8	D0	20	A1
9	CLK0	21	$\overline{CS}$
10	OUT0	22	$\overline{RD}$
11	GATE0	23	$\overline{WR}$
12	GND	24	V_{CC}

FIGURE 1. Terminal connections.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A1	A0	
0	1	0	0	0	Load counter number 0
0	1	0	0	1	Load counter number 1
0	1	0	1	0	Load counter number 2
0	1	0	1	1	Write mode word
0	0	1	0	0	Read counter number 0
0	0	1	0	1	Read counter number 1
0	0	1	1	0	Read counter number 2
0	0	1	1	1	No-operation three-state
1	X	X	X	X	Disable three-state
0	1	1	X	X	No-operation three-state

Mode register for latching count

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1, SC0 - Specify counter to be latched.
D5, D4 - 00 designates counter latching operation.
X - Don’t care.

Control word format

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

FIGURE 2. Truth tables.

Definition of control

SC – Select counter

SC1	SC0	
0	0	Select counter 0
0	1	Select counter 1
1	0	Select counter 2
1	1	Illegal

RL – Read/Load

RL1	RL0	
0	0	Counter latching operation
1	0	Read/load most significant byte only
0	1	Read/load least significant byte only
1	1	Read/load least significant byte first, then most significant byte

M - Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

FIGURE 2. Truth tables - Continued.

BCD

0	Binary counter 16-bits
1	Binary code decimal (BCD) counter (4 decades)

Gate pin operations summary

Modes	Signal status		
	Low or going low	Rising	High
0	Disables counting	-	Enables counting
1	-	1. Initiates counting 2. Resets output after next clock	-
2	1. Disables counting 2. Sets output immediately high	1. Reloads counter 2. Initiates counting	Enables counting
3	1. Disables counting 2. Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	-	Enables counting
5	-	Initiates counting	-

FIGURE 2. Truth tables - Continued.

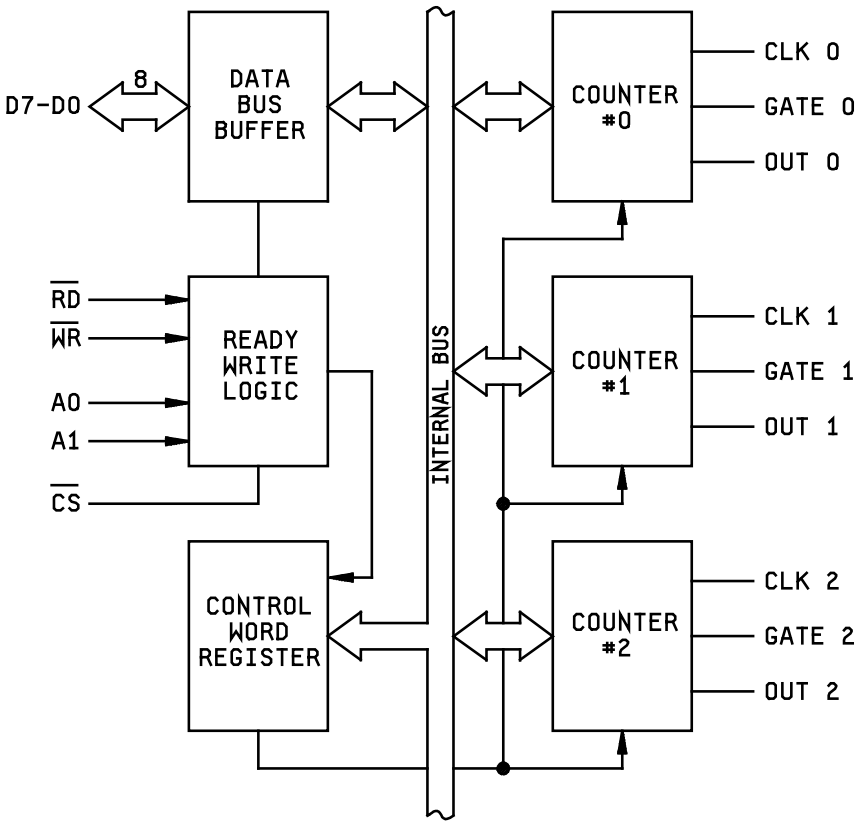


FIGURE 3. Block diagram.

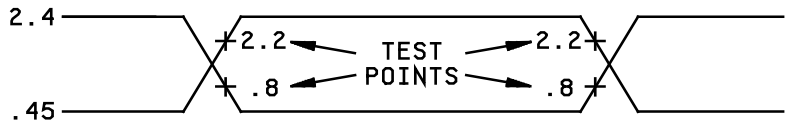
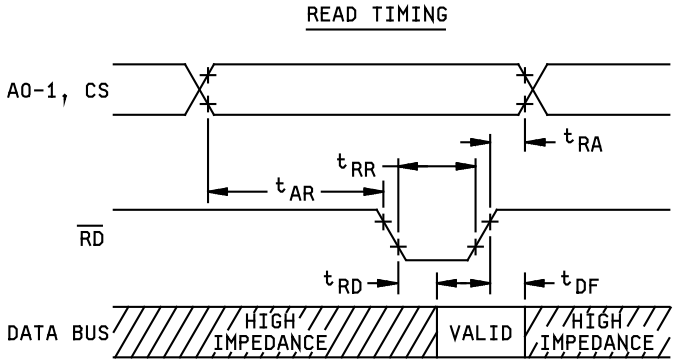
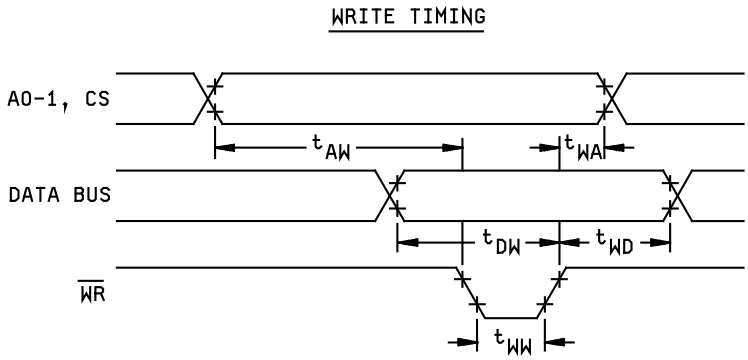


FIGURE 4. Switching test input waveform.





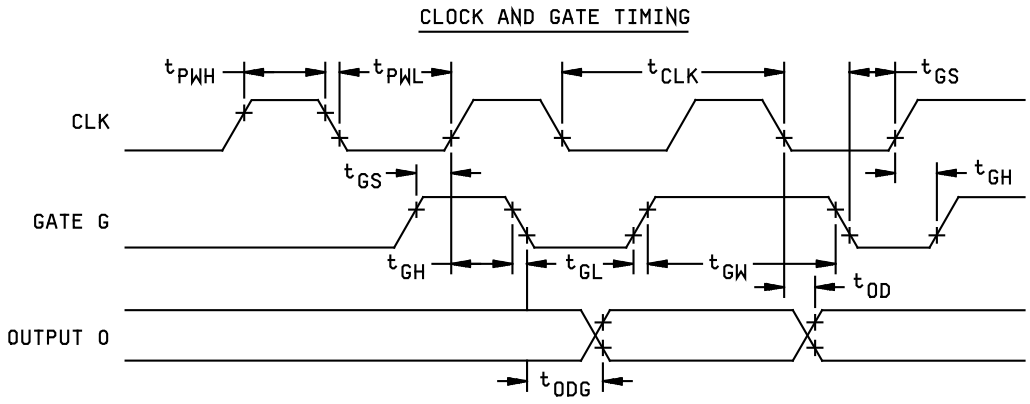


FIGURE 5. Timing waveforms.

4. VERIFICATION

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (method 5005)	1*, 2, 3, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3 or 2, 8A, 10
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroup 1.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 are verified by testing to the truth tables in figure 2.

d. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured initially and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform DLA Land and Maritime when a system application requires configuration control and the applicable SMD to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.5 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103 and QML-38535. The vendors listed in MIL-HDBK-103 and QML-38535 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DLA Land and Maritime-VA.

TABLE III. Pin description.

Pin number	Name	Input/Output	Description
1 – 8	D7 – D0	I/O	Data bus (8-bit)
9, 15, 18	CLK N	I	Counter clock inputs
11, 14, 16	GATE N	I	Counter gate inputs
10, 13, 17	OUT N	O	Counter outputs
22	$\overline{RD}$	I	Read counter
23	$\overline{WR}$	I	Write command or data
21	$\overline{CS}$	I	Chip select
19, 20	A0, A1	I	Counter select
24	V_{CC}		+5 volts
12	GND		Ground

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 19-07-26

Approved sources of supply for SMD 5962-87520 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at: https://landandmaritimeapps.dla.mil/programs/smcr/

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8752001JA	3/	8253
5962-8752002JA	3V146	MD8253/BJA
5962-8752003JA	3/	8253-5

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
3V146	Rochester Electronics 16 Malcolm Hoyt Drive Newburyport, MA 01950