

MOSFET – Power, Single N-Channel 40 V, 0.82 mΩ, 330 A

NVMFS5C410NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C410NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	40	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^\circ\text{C}$	I_D	330
		$T_C = 100^\circ\text{C}$		230
Power Dissipation $R_{\theta JC}$ (Note 1)		$T_C = 25^\circ\text{C}$	P_D	167
		$T_C = 100^\circ\text{C}$		83
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^\circ\text{C}$	I_D	50
		$T_A = 100^\circ\text{C}$		35
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^\circ\text{C}$	P_D	3.8
		$T_A = 100^\circ\text{C}$		1.9
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10\ \mu\text{s}$	I_{DM}	900	A
Operating Junction and Storage Temperature Range		T_J , T_{stg}	-55 to +175	°C
Source Current (Body Diode)		I_S	169	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{L(pk)} = 29\ \text{A}$)		E_{AS}	706	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	°C

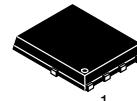
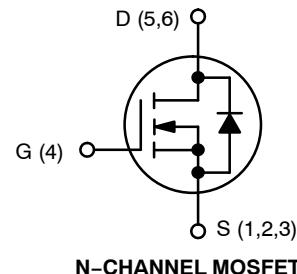
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	0.9	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	39	

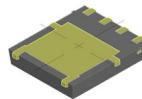
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(\text{BR})DSS}$	$R_{DS(\text{ON}) \text{ MAX}}$	$I_D \text{ MAX}$
40 V	0.82 mΩ @ 10 V	330 A
	1.2 mΩ @ 4.5 V	



**DFN5
(SO-8FL)
CASE 488AA
STYLE 1**

XXXXXX = 5C410L
(NVMFS5C410NL) or
410LWF
(NVMFS5C410NLWF)
D = Assembly Location
S = Year
W = Work Week
G = Lot Traceability



**DFNW5
(SO-8FL WF)
CASE 507BE**

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFS5C410NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA		40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J				21.2		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 40 V	T _J = 25°C		10	μA	
			T _J = 125°C		250		
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = 20 V			100	nA	

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA		1.2		2.0	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J				-5.75		mV/°C
Drain-to-Source On Resistance	R _{DSS(on)}	V _{GS} = 10 V	I _D = 50 A		0.65	0.82	mΩ
		V _{GS} = 4.5 V	I _D = 50 A		0.95	1.2	
Forward Transconductance	g _F	V _{DS} = 15 V, I _D = 50 A			190		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V		8862		pF
Output Capacitance	C _{OSS}			4156		
Reverse Transfer Capacitance	C _{rss}			116		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 20 V; I _D = 50 A	V _{GS} = 4.5 V, V _{DS} = 20 V; I _D = 50 A	66		nC
Total Gate Charge	Q _{G(TOT)}		V _{GS} = 10 V, V _{DS} = 20 V; I _D = 50 A	143		
Threshold Gate Charge	Q _{G(TH)}			6.75		
Gate-to-Source Charge	Q _{GS}			21.4		
Gate-to-Drain Charge	Q _{GD}			22		
Plateau Voltage	V _{GP}			2.7		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DS} = 20 V, I _D = 50 A, R _G = 1.0 Ω		20		ns
Rise Time	t _r			130		
Turn-Off Delay Time	t _{d(OFF)}			66		
Fall Time	t _f			177		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = 50 A	T _J = 25°C		0.73	1.2	V
			T _J = 125°C		0.6		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A			79.5		ns
Charge Time	t _a				39		
Discharge Time	t _b				40.5		
Reverse Recovery Charge	Q _{RR}				126		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

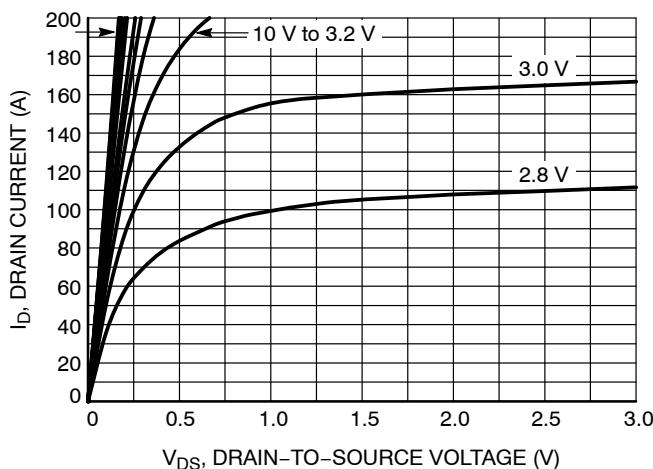


Figure 1. On-Region Characteristics

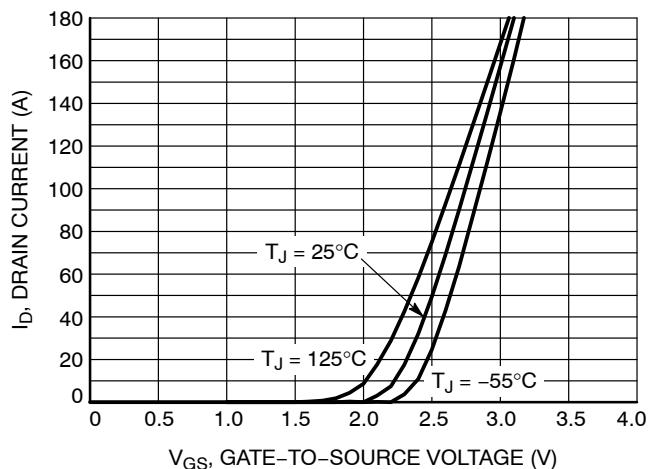


Figure 2. Transfer Characteristics

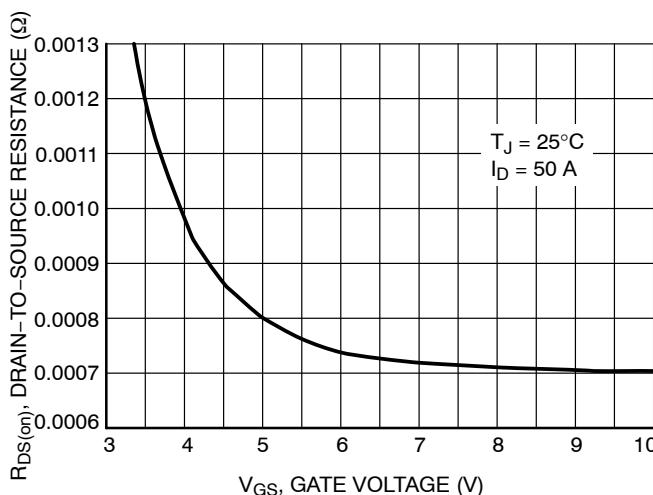


Figure 3. On-Resistance vs. Gate-to-Source Voltage

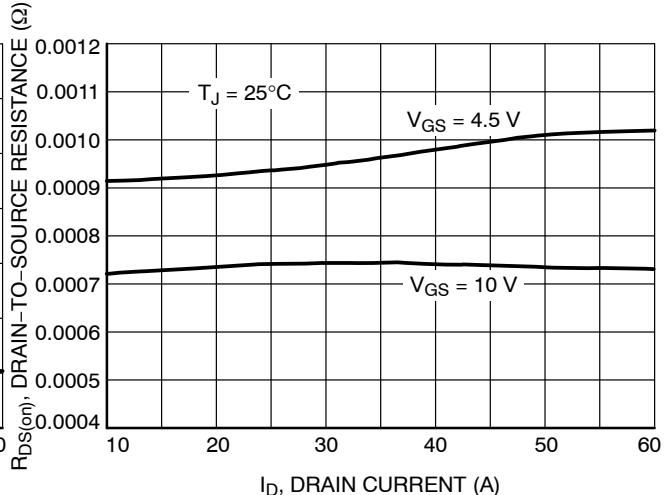


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

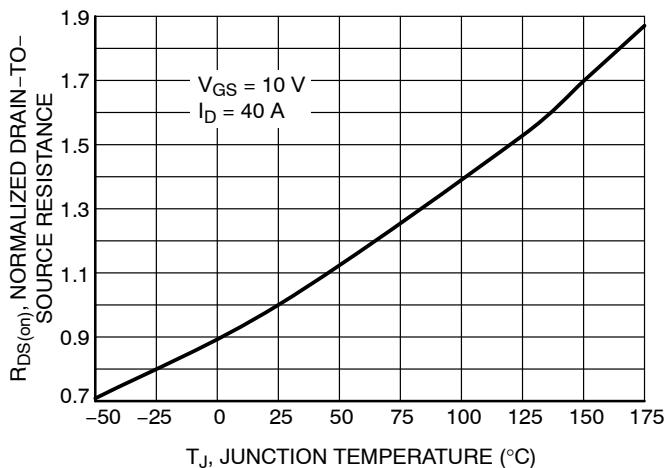


Figure 5. On-Resistance Variation with Temperature

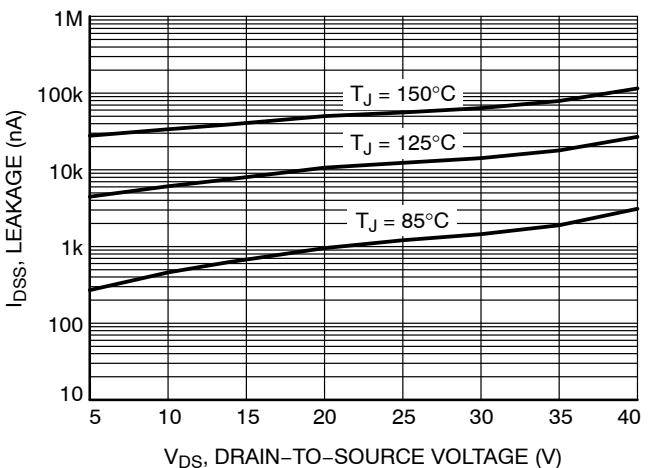


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

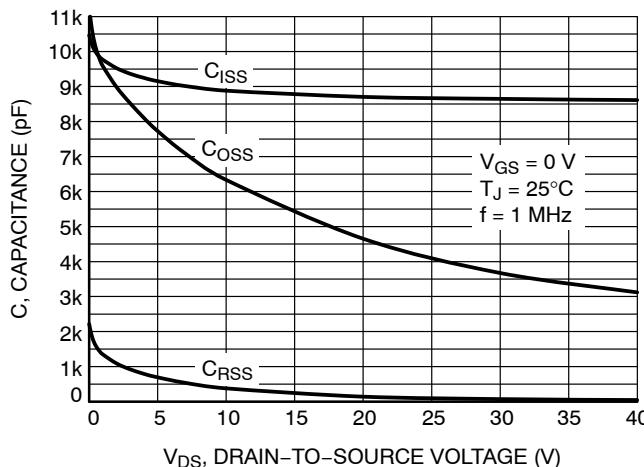


Figure 7. Capacitance Variation

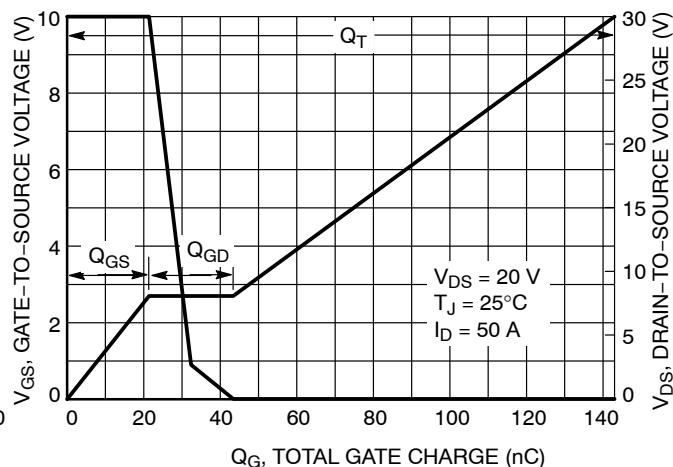


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

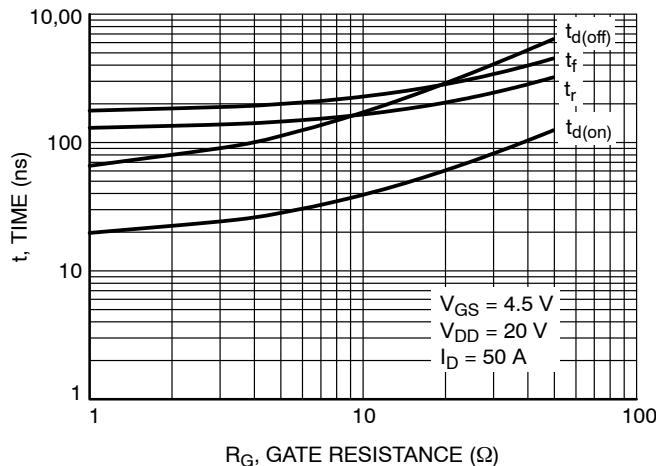


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

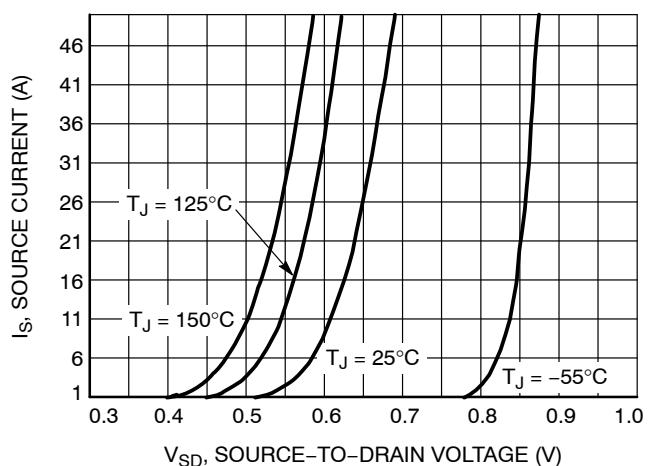


Figure 10. Diode Forward Voltage vs. Current

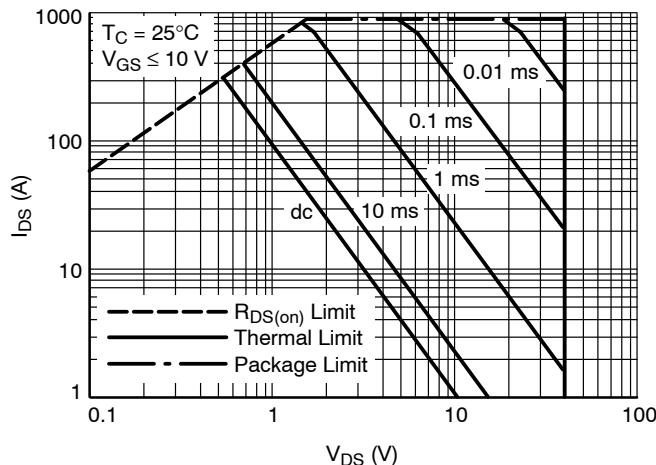


Figure 11. Safe Operating Area

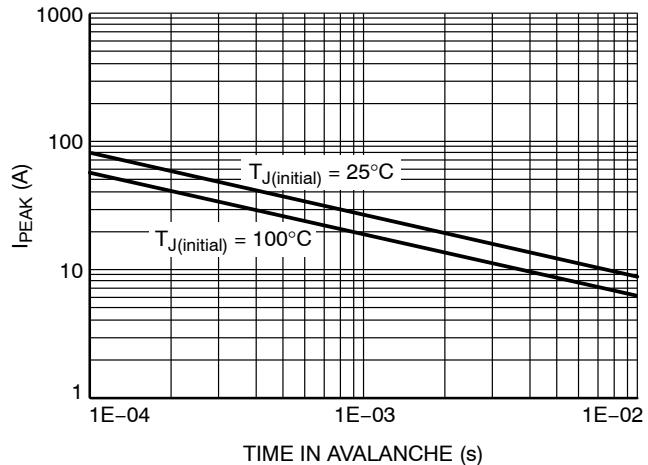


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFS5C410NL

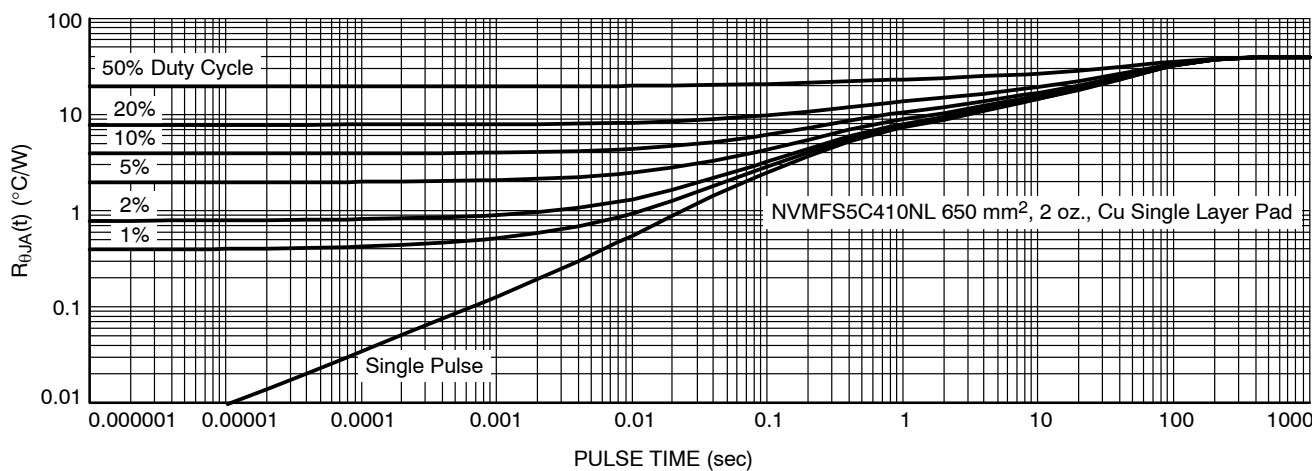


Figure 13. Thermal Characteristics

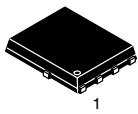
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
NVMFS5C410NLT1G	5C410L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C410NLWFT1G	410LWF	DFNW5 (Pb-Free, Wettable Flanks, Full-cut SO-8FL WF)	1500 / Tape & Reel
NVMFS5C410NLT3G	5C410L	DFN5 (Pb-Free)	5000 / Tape & Reel
NVMFS5C410NLWFT3G	410LWF	DFNW5 (Pb-Free, Wettable Flanks, Full-cut SO-8FL WF)	5000 / Tape & Reel
NVMFS5C410NLRAFT1G	5C410L	DFN5 (Pb-Free)	1500 / Tape & Reel
NVMFS5C410NLWFAFT1G	410LWF	DFNW5 (Pb-Free, Wettable Flanks, Full-cut SO-8FL WF)	1500 / Tape & Reel
NVMFS5C410NLWFET1G	410LWF	DFNW5 (Full-cut SO-8FL WF)	1500 / Tape & Reel
NVMFS5C410NLWFET3G	410LWF	DFNW5 (Full-cut SO-8FL WF)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

onsemiTM



SCALE 2:1

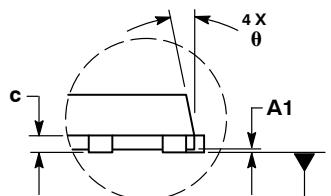
**DFN5 5x6, 1.27P
(SO-8FL)**
CASE 488AA
ISSUE N

DATE 25 JUN 2018

NOTES:

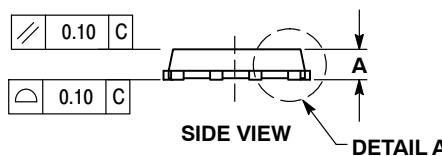
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°

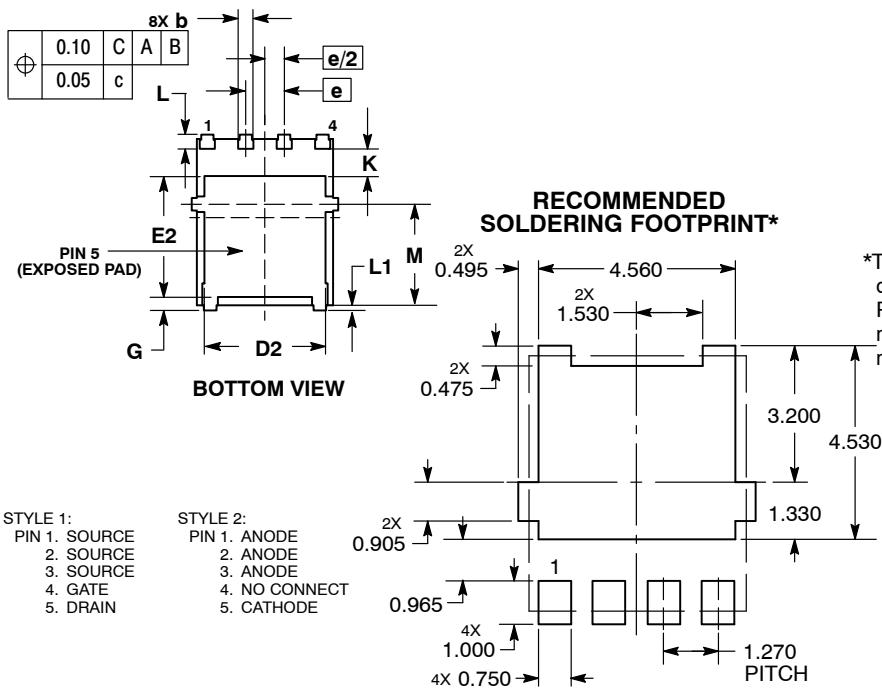


DETAIL A

SEATING PLANE



DETAIL A

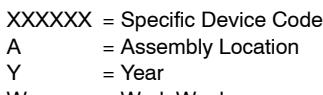


STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

DIMENSIONS: MILLIMETERS

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

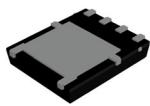


XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

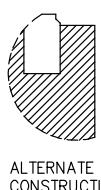
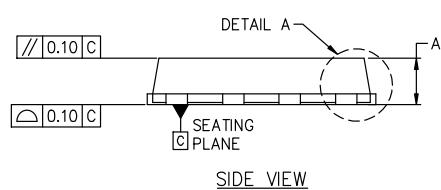
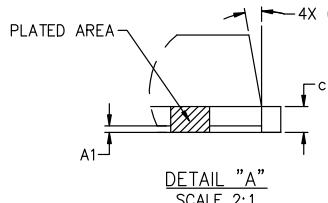
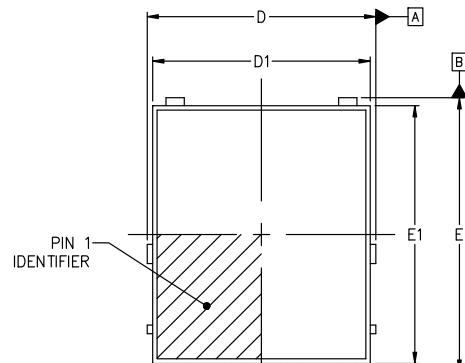
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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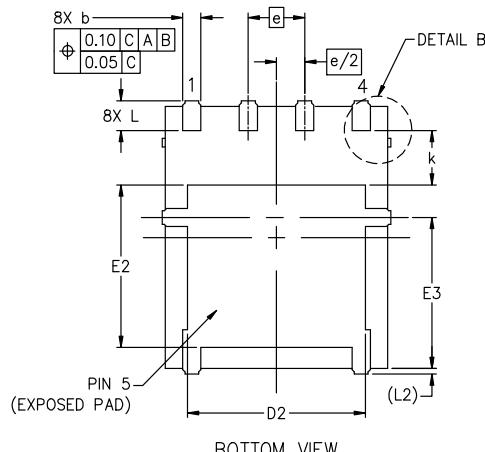
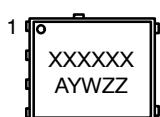
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DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BE
ISSUE B

DATE 19 SEP 2024



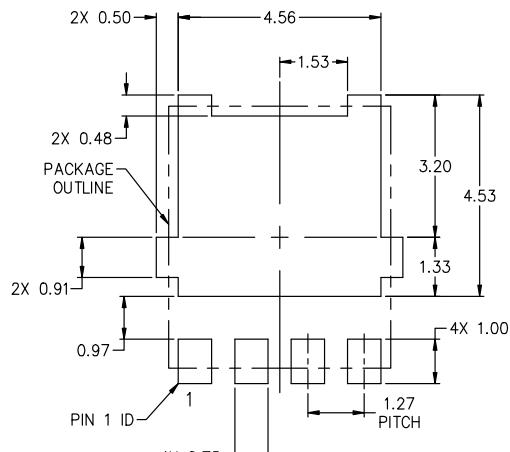
DETAIL "B" SCALE 2:1


**GENERIC
MARKING DIAGRAM***


XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking.
 Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
E3	3.00	3.40	3.80
e	1.27 BSC		
k	1.20	1.35	1.50
L	0.51	0.57	0.71
L2	0.15 REF.		
θ	0°	6°	12°



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SODERM/D.

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DESCRIPTION:	DFNW5 4.90x5.90x1.00, 1.27P	PAGE 1 OF 1

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