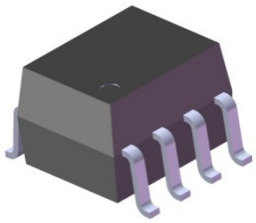
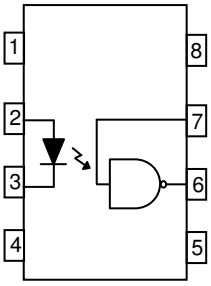
DATASHEET

8 PIN SOP 3.3V HIGH SPEED - 10MBit/s LOGIC GATE PHOTOCOUPLER EL060L



Schematic



A 0.1μF bypass capacitor must be connected between pins 8 and 5 *1

Pin Configuration
1, No Connection
2, Anode
3, Cathode
4. No Connection
5, Gnd
6, Vout
7, V_E
8, V_{CC}

Features

- •Compliance Halogen Free (Br <900 ppm ,Cl <900 ppm , Br+Cl < 1500 ppm)
- 3.3 and 5 V dual supply voltage
- High speed 10Mbit/s
- 10kV/μs min. common mode transient immunity
- Guaranteed performance from -40 to 85℃
- Logic gate output, Fan out 10
- High isolation voltage between input and output (Viso=3750 V rms)
- Compliance with EU REACH
- Pb free and RoHS compliant
- UL and cUL approved(No. E214129)
- VDE approved (No. 40028116)
- SEMKO approved
- NEMKO approved
- DEMKO approved
- FIMKO approved Description

Description

The EL060L consists of an infrared emitting diode optically coupled to a high speed integrated photo detector logic gate with a strobable output. It is packaged in a 8-pin SOP package and is suitable for surface mounting technology.

Applications

- Ground loop elimination
- LSTTL to TTL, LSTTL or 5 volt CMOS
- Line receiver, data transmission
- Data multiplexing
- Switching power supplies
- Pulse transformer replacement
- Computer peripheral interface
- High speed logic ground isolation

Truth Table (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

Absolute Maximum Ratings (T_A=25℃)

Parameter		Symbol	Rating	Unit
Input	Forward current	I_F	50	mA
	Enable input voltage Not exceed V_{CC} by more than 500mV	V_E	V_{CC} + 0.5	V
	Enable Input Current	I_E	5	mA
	Reverse voltage	V_R	5	V
	Power dissipation	P_D	45	mW
Output	Power dissipation	P_C	85	mW
	Output current	I_O	50	mA
	Output voltage	V_O	7.0	V
	Supply voltage	V_{CC}	7.0	V
Output Power Dissipation		P_O	85	mW
Isolation voltage *2		V_{ISO}	3750	V rms
Operating temperature		T_{OPR}	-40 ~ +85	℃
Storage temperature		T_{STG}	-55 ~ +125	℃
Soldering temperature *3		T_{SOL}	260	℃

Notes:

*1 The V_{CC} supply must be bypassed by a 0.1μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins

*2 AC for 1 minute, R.H.= 40 ~ 60% R.H. In this test, pins 1, 2, 3 & 4 are shorted together, and pins 5, 6, 7 & 8 are shorted together.

*3 For 10 seconds

Electrical Characteristics (T_A=-40 to 85℃ unless specified otherwise)

Input

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Forward voltage	V_F	-	1.4	1.8	V	I_F = 10mA
Reverse voltage	V_R	5.0	-	-	V	I_R = 10μA
Temperature coefficient of forward voltage	$\Delta V_F/\Delta T_A$	-	-1.8	-	mV/℃	I_F =10mA
Input capacitance	C_{IN}	-	60	-	pF	V_F=0, f=1MHz

Output

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level supply current	I_{CCH}	-	5	10	mA	I_F=0mA, V_E=0.5V, V_{CC}=3.3V
Low level supply current	I_{CCL}	-	9	13	mA	I_F=10mA, V_E=0.5V V_{CC}=3.3V
High level enable current	I_{EH}	-	-	-1.6	mA	V_E=2.0 V, V_{CC}=3.3V
Low level enable current	I_{EL}	-	-	-1.6	mA	V_E=0.5 V, V_{CC}=3.3V
High level enable voltage[*4]	V_{EH}	2.0	-	-	V	I_F=10mA, V_{CC}=3.3V
Low level enable voltage	V_{EL}	-	-	0.8	V	I_F=10mA, V_{CC}=3.3V

Transfer Characteristics (T_A=-40 to 85℃ unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
High level output current	I_{OH}	-	5.0	100	uA	V_{CC}=3.3V, V_O=3.3V, I_F=250μA, V_E=2.0V
Low level output voltage	V_{OL}	-	0.35	0.6	V	V_{CC} = 3.3V, I_F=5mA, V_E=2.0V,I_{OL}=13mA
Input threshold current	I_{FT}	-	3	5	mA	V_{CC}= 3.3V, V_O=0.6V, V_E =2.0V,I_{OL}=13mA

Switching Characteristics (T_A=-40 to 85℃, V_{CC}=3.3V, I_F=7.5mA unless specified otherwise)

Parameter	Symbol	Min	Typ.	Max.	Unit	Condition
Propagation delay time to output high level*5 (Fig.12)	t_{PHL}	-	50	75	ns	C_L = 15pF, R_L=350Ω, T_A=25℃
Propagation delay time to output low level*6 (Fig.12)	t_{PLH}	-	45	75	ns	C_L = 15pF, R_L=350Ω, T_A=25℃
Pulse width distortion	$\|t_{PHL} - t_{PLH}\|$	-	5	35	ns	C_L = 15pF, R_L=350Ω
Output rise time*7 (Fig.12)	t_r	-	50	-	ns	C_L = 15pF, R_L=350Ω
Output fall time*8 (Fig.12)	t_f	-	10	-	ns	C_L = 15pF, R_L=350Ω
Enable propagation delay time to output High Level*9 (Fig.13)	t_{ELH}	-	30	-	ns	I_F = 7.5mA , V_{EH}=3.0V, C_L = 15pF, R_L=350Ω
Enable propagation delay time to output low level*10 (Fig.13)	t_{EHL}	-	15	-	ns	I_F = 7.5mA , V_{EH}=3.0V, C_L = 15pF, R_L=350Ω
Common mode transient Immunity at logic high*11	CM_H	10,000	-	-	V/μS	I_F = 7.5mA , V_{OH}=2.0V, R_L=350Ω, T_A=25℃ V_{CM}=400Vp-p (Fig.14)
Common mode transient immunity at logic low*12	CM_L	10,000	-	-	V/μS	I_F = 0mA , V_{OL}=0.8V, R_L=350Ω, T_A=25℃ V_{CM}=400Vp-p (Fig.14)

Typical Electro-Optical Characteristics Curves

Figure 1. Forward Current vs. Forward Voltage

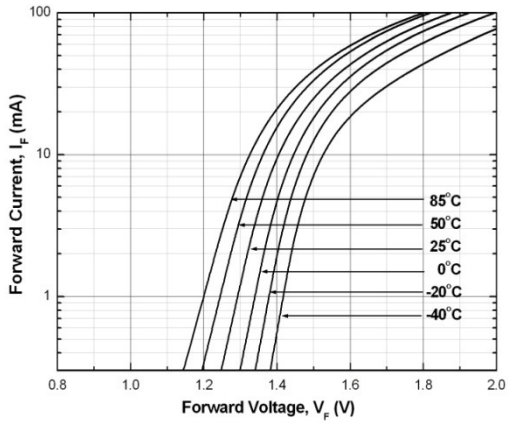


Figure 2. Low Level Output Voltage vs. Ambient Temperature

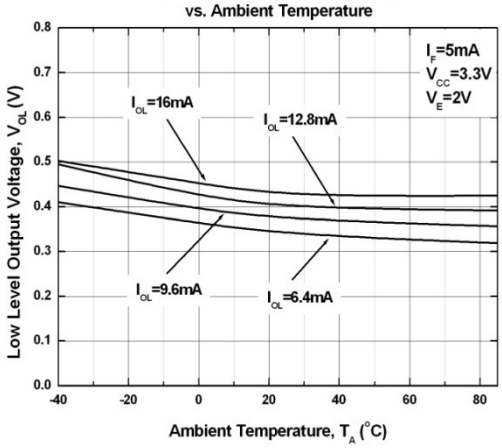


Figure 3. Low Level Output Current vs. Ambient Temperature

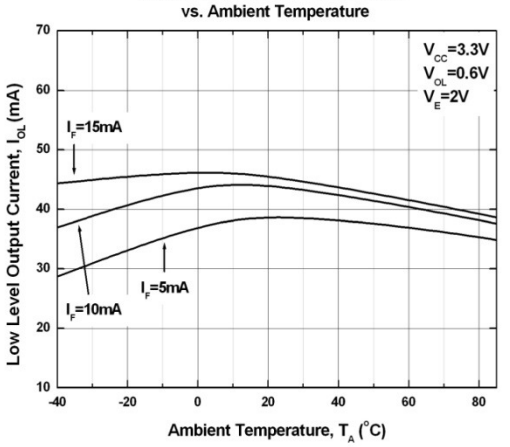


Figure 4. Input Threshold Current vs. Ambient Temperature

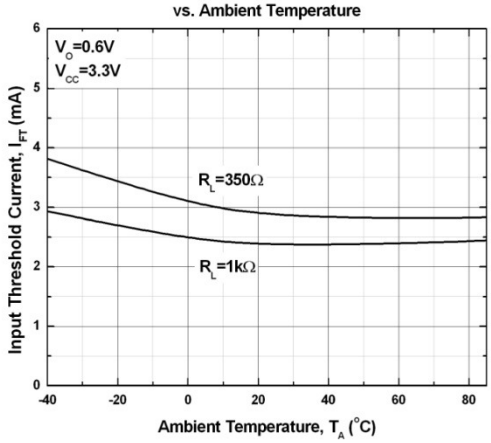


Figure 5. Input Current vs. Output Voltage

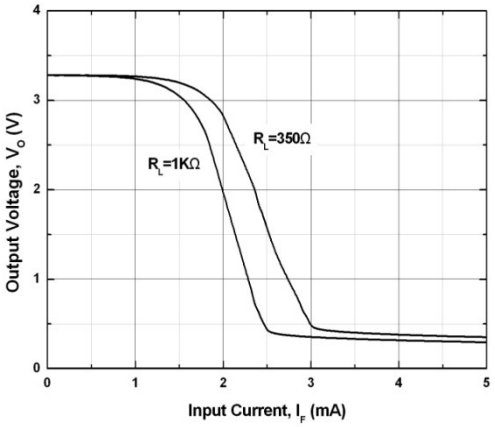


Figure 6. High Level Output Current vs. Ambient Temperature

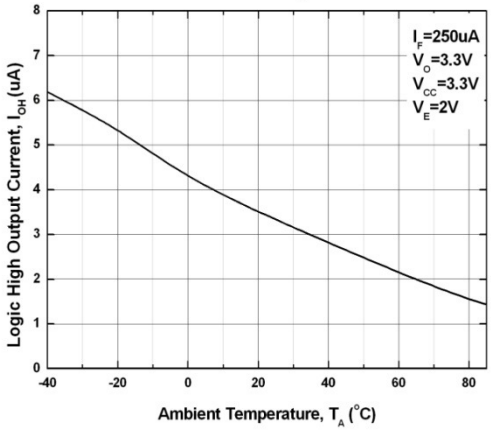


Figure 7. Propagation Delay vs. Forward Current

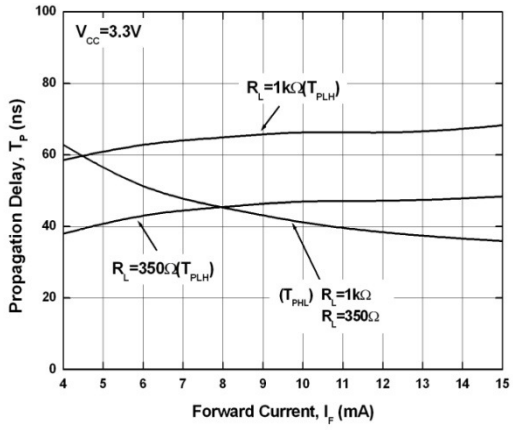


Figure 8. Propagation Delay vs. Temperature

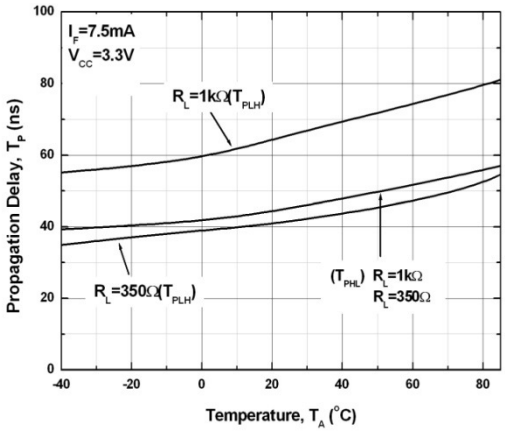


Figure 9. Pulse Width Distortion vs. Temperature

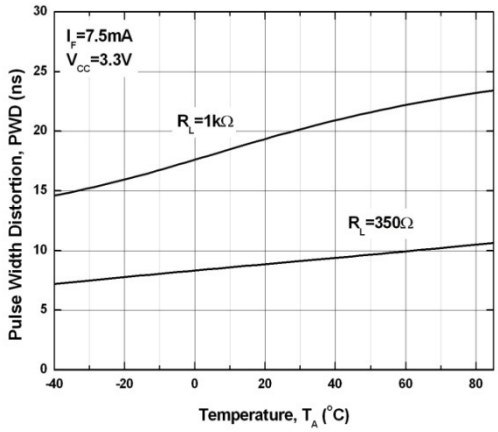


Figure 10. Rise and Fall Time vs. Temperature

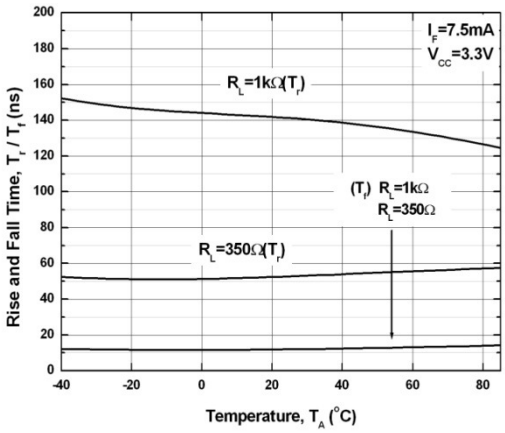


Figure 11. Enable Propagation Delay vs. Temperature

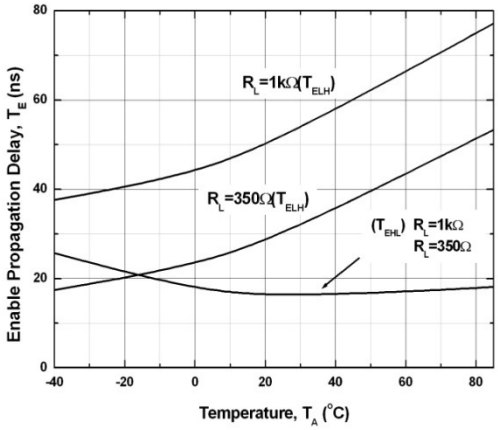


Fig. 12 Test circuit and waveforms for t_{PHL}, t_{PLH}, t_r, and t_f

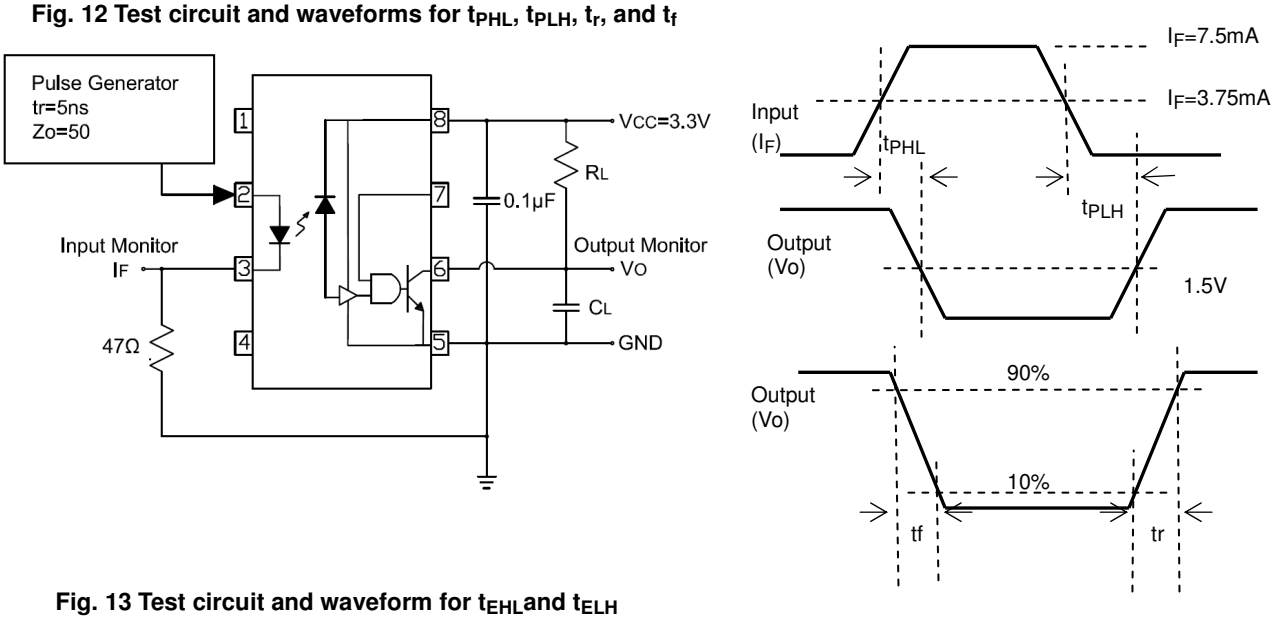


Fig. 13 Test circuit and waveform for $t_{EHL}$and t_{ELH}

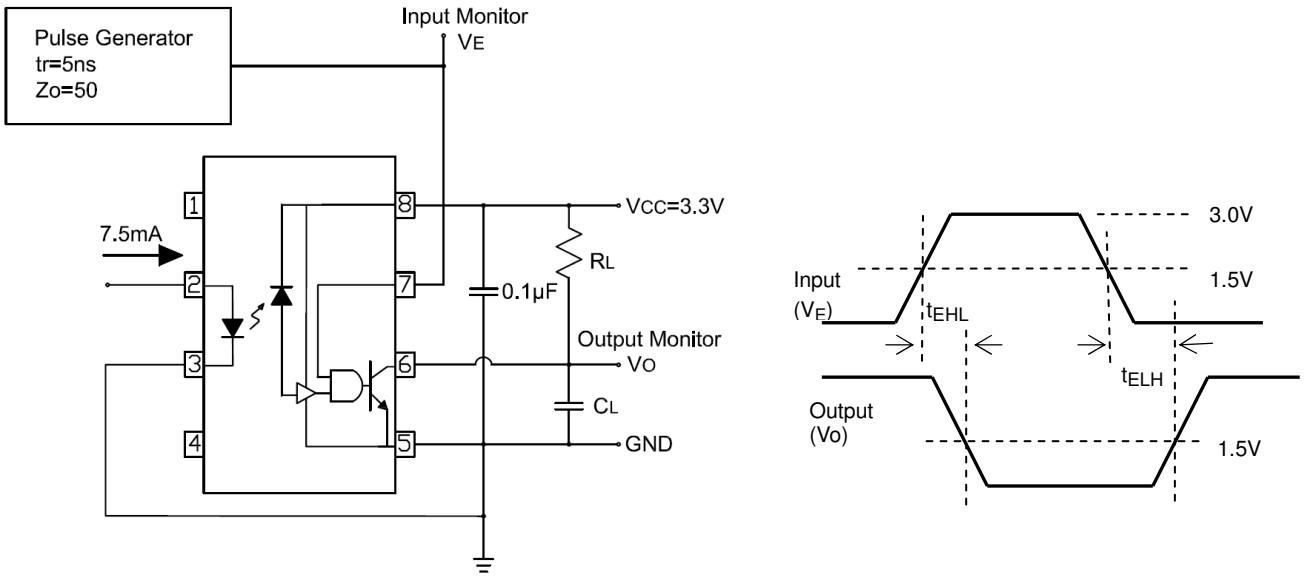
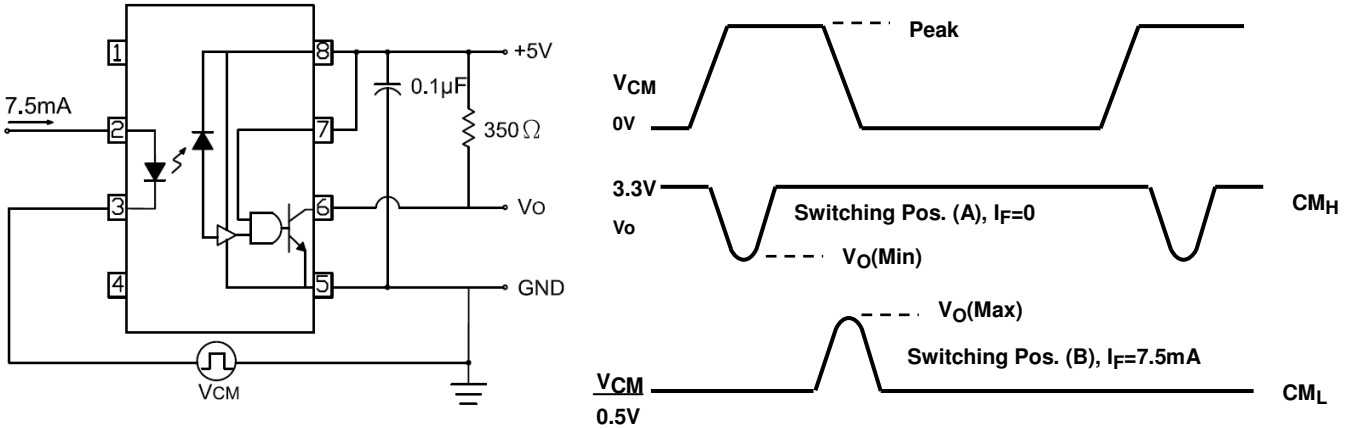


Fig. 14 Test circuit Common mode Transient Immunity



Note
*4. Enable Input – No pull up resistor required as the device has an internal pull up resistor.
*5. t_{PLH} – Propagation delay is measured from the 3.75mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
*6. t_{PHL} – Propagation delay is measured from the 3.75mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
*7. t_r – Rise time is measured from the 90% to the 10% levels on the LOW to HIGH transition of the output pulse.
*8. t_f – Fall time is measured from the 10% to the 90% levels on the HIGH to LOW transition of the output pulse.
*9. t_{ELH} – Enable input propagation delay is measured from the 1.5V level on the HIGH to LOW transition of the input voltage pulse to the 1.5V level on the LOW to HIGH transition of the output voltage pulse.
*10. t_{EHL} – Enable input propagation delay is measured from the 1.5V level on the LOW to HIGH transition of the input voltage pulse to the 1.5V level on the HIGH to LOW transition of the output voltage pulse.
*11 CM_H– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the HIGH state (i.e., V_{OUT} > 2.0V).
*12 CM_L– The maximum tolerable rate of rise of the common mode voltage to ensure the output will remain in the LOW output state (i.e., V_{OUT} < 0.8V).

Order Information

Part Number

EL060L(Z)-V

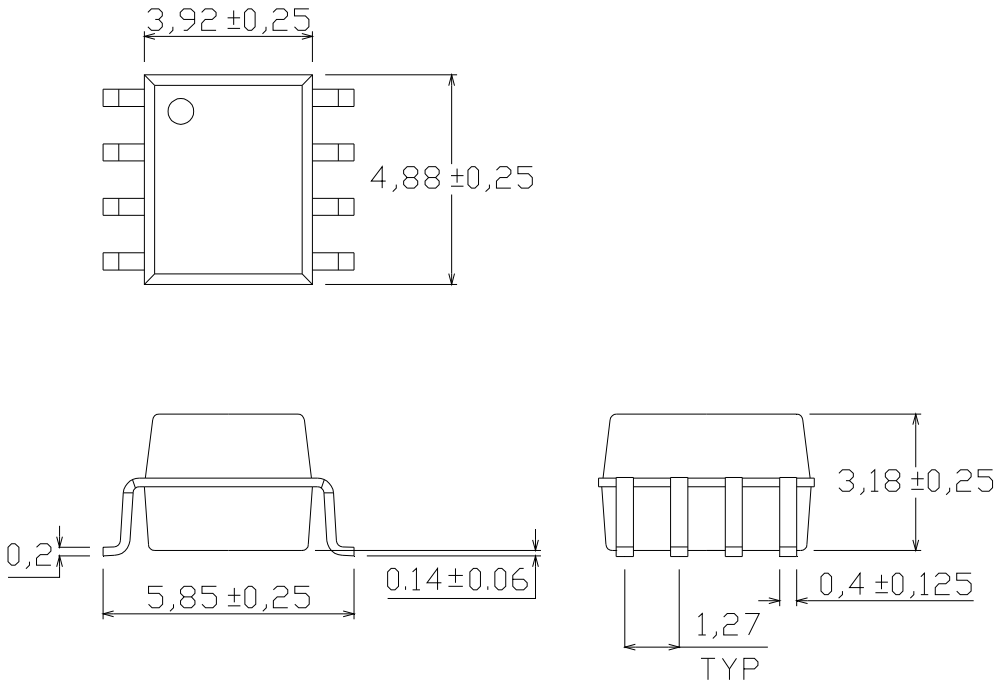
Note

Z = Tape and reel option (TA, TB or none).
V = VDE (optional)

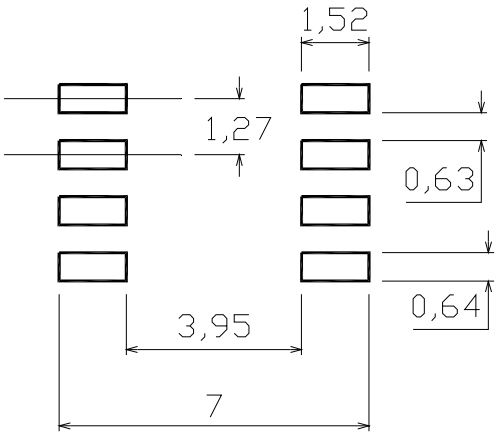
Option	Description	Packing quantity
None	Standard	100 units per tube
-V	Standard + VDE	100 units per tube
(TA)	TA tape & reel option	2000 units per reel
(TB)	TB tape & reel option	2000 units per reel
(TA)-V	TA tape & reel option + VDE	2000 units per reel
(TB)-V	TB tape & reel option + VDE	2000 units per reel

Package Dimension

(Dimensions in mm)



Recommended pad layout for surface mount leadform



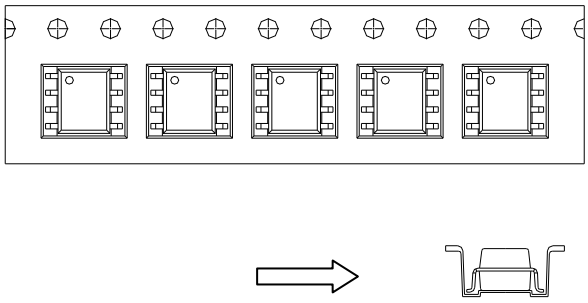
Device Marking

Notes

EL	denotes EVERLIGHT
060L	denotes Device Number
Y	denotes 1 digit Year code
WW	denotes 2 digit Week code
V	denotes VDE (optional)

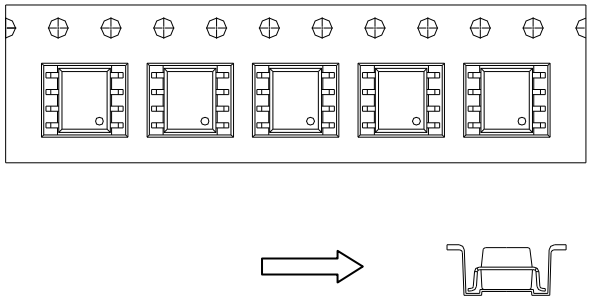
Tape & Reel Packing Specifications

Option TA



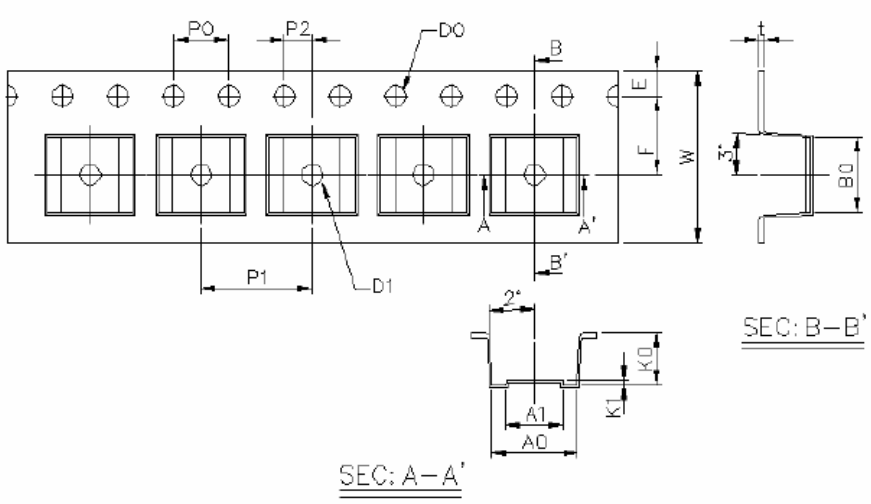
Direction of feed from reel

Option TB



Direction of feed from reel

Tape dimension

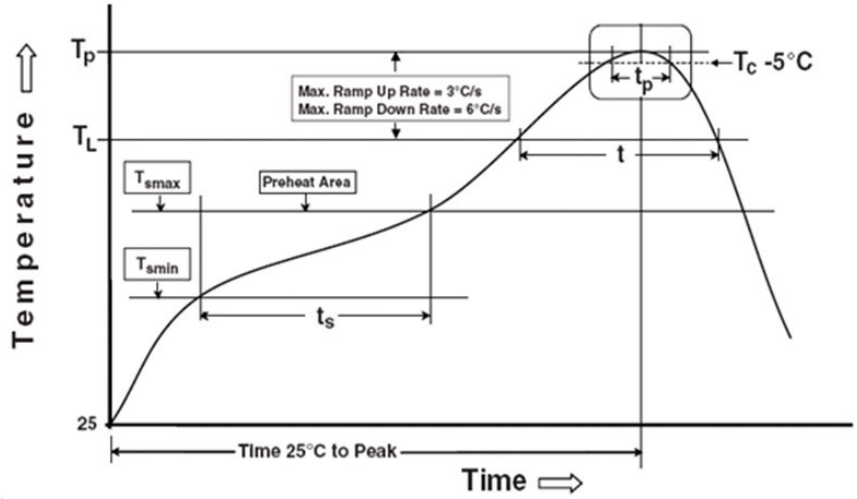


Dimension No.	A0	A1	B0	D0	D1	E	F
Dimension(mm)	6.2±0.1	4.1±0.1	5.28±0.1	1.5±0.1	1.5±0.3	1.75±0.1	5.5±0.1
Dimension No.	Po	P1	P2	t	W	K0	K1
Dimension(mm)	4.0±0.1	8.0±0.1	2.0±0.1	0.4±0.1	12.0+0.3/ -0.1	3.7±0.1	0.3±0.1

Precautions for Use

1. Soldering Condition

1.1 (A) Maximum Body Case Temperature Profile for evaluation of Reflow Profile



Note: Reference: IPC/JEDEC J-STD-020D

Preheat	
Temperature min (T_{smin})	150 ℃
Temperature max (T_{smax})	200℃
Time (T_{smin} to T_{smax}) (t_s)	60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 ℃/second max
Other	
Liquidus Temperature (T_L)	217 ℃
Time above Liquidus Temperature (t_L)	60-100 sec
Peak Temperature (T_P)	260℃
Time within 5 ℃ of Actual Peak Temperature: T_P - 5℃	30 s
Ramp- Down Rate from Peak Temperature	6℃ /second max.
Time 25℃ to peak temperature	8 minutes max.
Reflow times	3 times

Disclaimer

1. Above specification may be changed without notice. EVERLIGHT will reserve authority on material change for above specification.
2. When using this product, please observe the absolute maximum ratings and the instructions for using outlined in these specification sheets. EVERLIGHT assumes no responsibility for any damage resulting from use of the product which does not comply with the absolute maximum ratings and the instructions included in these specification sheets.
3. These specification sheets include materials protected under copyright of EVERLIGHT corporation. Please don't reproduce or cause anyone to reproduce them without EVERLIGHT's consent.