OBSOLETE PRODUCT
RECOMMENDED REPLACEMENT
HC55120

August 2003 FN2799.8

ITU CO/Loop Carrier SLIC

The HC-5509B telephone Subscriber Line Interface Circuit integrates most of the BORSCHT functions on a monolithic IC. The device is manufactured in a Dielectric Isolation (DI) process and is designed for use as a high voltage interface between the traditional telephone subscriber pair (Tip and Ring) and the low voltage filtering and coding/decoding functions of the line card. Together with a secondary protection diode bridge and “feed” resistors, the device will withstand 1000V lightning induced surges, in plastic packages. The SLIC also maintains specified transmission performance in the presence of externally induced longitudinal currents. The BORSCHT functions that the SLIC provides are:

Battery Feed with Subscriber Loop Current Limiting

- Overvoltage Protection
- Ring Relay Driver
- Supervisory Signaling Functions
- Hybrid Functions (with External Op Amp)
- Test (or Battery Reversal) Relay Driver

In addition, the SLIC provides selective denial of power to subscriber loops, a programmable subscriber loop current limit from 20mA to 60mA, a thermal shutdown with an alarm output and line fault protection. Switch hook detection, ring trip detection and ground key detection functions are also incorporated in the SLIC device.

The HC-5509B SLIC is ideally suited for line card designs in PBX and CO systems, replacing traditional transformer solutions.

Part Number Information

PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. DWG. #
HC9P5509B-5	0 to 75	28 Ld SOIC	M28.3

Features

- DI Monolithic High Voltage Process
- Compatible with Worldwide PBX and CO Performance Requirements
- Controlled Supply of Battery Feed Current with Programmable Current Limit
- Operates with 5V Positive Supply (V_B+)
- Internal Ring Relay Driver and a Utility Relay Driver
- High Impedance Mode for Subscriber Loop
- High Temperature Alarm Output
- Low Power Consumption During Standby Functions
- Switch Hook, Ground Key, and Ring Trip Detection
- Selective Power Denial to Subscriber
- Voice Path Active During Power Denial
- On-Chip Op Amp for 2-Wire Impedance Matching

Applications

- Solid State Line Interface Circuit for PBX or Central Office Systems, Digital Loop Carrier Systems
- Hotel/Motel Switching Systems
- Direct Inward Dialing (DID) Trunks
- Voice Messaging PBXs
- High Voltage 2-Wire/4-Wire, 4-Wire/2-Wire Hybrid
- Related Literature
  - AN9607, Impedance Matching Design Equations
  - AN9628, AC Voltage Gain
  - AN9608, Implementing Pulse Metering
  - AN549, The HC-5502S/4X Telephone Subscriber Line Interface Circuits (SLIC)

Absolute Maximum Ratings (Note 1)

Relay Drivers . . . . . -0.5V to 15V
Maximum Supply Voltages
(V_{B+}) . . . . . -0.5V to 7V
(V_{B+})-(V_{B-}) 75V

Operating Conditions

Operating Temperature Range
HC-5509B-5 . . . . . 0^oC to 75^oC
Relay Drivers . . . . . 5V to 12V
Positive Power Supply (V_{B+}) . . . . . 5V ±5%
Negative Power Supply (V_{B-}) . . . . . -42V to -58V
Loop Resistance (R_L) . . . . . 200Ω to 1750Ω (Note 2)

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
SOIC Package	72	N/A

Maximum Junction Temperature Plastic . . . . . 150^oC
Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(For SMD; SOIC - Lead Tips Only)

Die Characteristics

Transistor Count 224
Diode Count 28
Die Dimensions . . . . . 174 x 120
Substrate Potential . . . . . Connected
Process . . . . . Bipolar-DI

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. May Be Extended to 1900Ω With Application Circuit.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

Unless Otherwise Specified, Typical Parameters are at $T_A = 25^oC$, Min-Max Parameters are Over Operating Temperature Range, V_{B-} = -48V, V_{B+} = 5V, AG = DG = BG = 0V. All AC Parameters are specified at 600Ω 2-Wire Terminating Impedance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
AC TRANSMISSION PARAMETERS					
RX Input Impedance	300Hz to 3.4kHz (Note 4)	-	100	-	kΩ
TX Output Impedance	300Hz to 3.4kHz (Note 4)	-	-	20	Ω
4-Wire Input Overload Level	300Hz to 3.4kHz R_L = 1200Ω, 600Ω Reference	1.5	-	-	V_{PEAK}
2-Wire Return Loss	Matched for 600Ω (Note 4)				
SRL LO		26	35	-	dB
ERL		30	40	-	dB
SRL HI		30	40	-	dB
2-Wire Longitudinal to Metallic Balance Off Hook	Per ANSI/IEEE STD 455-1976 (Note 4) 300Hz to 3400Hz	58	63	-	dB
4-Wire Longitudinal Balance Off Hook	300Hz to 3400Hz (Note 4)	50	55	-	dB
Low Frequency Longitudinal Balance	R.E.A. Test Circuit	-	-	-67	dBmp
	I_{LINE} = 40mA, $T_A = 25^oC$ (Note 4)	-	-	23	dBrnC
Longitudinal Current Capability	I_{LINE} = 40mA, $T_A = 25^oC$ (Note 4)	-	-	30	mA_{RMS}
Insertion Loss	0dBm at 1kHz, Referenced 600Ω				
2-Wire/4-Wire		-	±0.05	±0.2	dB
4-Wire/2-Wire		-	±0.05	±0.2	dB
4-Wire/4-Wire		-	-	±0.2	dB
Frequency Response	300Hz to 3400Hz (Note 4) Referenced to Absolute Level at 1kHz, 0dBm Referenced 600Ω	-	±0.02	±0.05	dB
Level Linearity	Referenced to -10dBm (Note 4)				
2-Wire to 4-Wire and 4-Wire to 2-Wire	+3 to -40dBm	-	-	±0.05	dB
	-40 to -50dBm	-	-	±0.1	dB
	-50 to -55dBm	-	-	±0.3	dB

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Delay	(Note 4)				
2-Wire/4-Wire	300Hz to 3400Hz	-	-	1	µs
4-Wire/2-Wire	300Hz to 3400Hz	-	-	1	µs
4-Wire/4-Wire	300Hz to 3400Hz	-	-	1.5	µs
Transhybrid Loss, THL	(Note 4) See Figure 1	-	40	-	dB
Total Harmonic Distortion 2-Wire/4-Wire, 4-Wire/2-Wire, 4-Wire/4-Wire	Reference Level 0dBm at 600Ω 300Hz to 3400Hz (Note 4)	-	-	-52	dB
Idle Channel Noise	(Note 4)				
2-Wire and 4-Wire	C-Message	-	-	5	dBrnC
	Psophometric	-	-	-85	dBmp
	3kHz Flat	-	-	15	dBrn
Power Supply Rejection Ratio	(Note 4)				
V_{B+} to 2-Wire	30Hz to 200Hz, R_L = 600Ω	20	29	-	dB
V_{B+} to 4-Wire		20	29	-	dB
V_{B-} to 2-Wire		20	29	-	dB
V_{B-} to 4-Wire		20	29	-	dB
V_{B+} to 4-Wire	(Note 4)	30	-	-	dB
V_{B-} to 2-Wire	200Hz to 16kHz, R_L = 600Ω	30	-	-	dB
V_{B-} to 4-Wire		20	25	-	dB
V_{B-} to 4-Wire		20	25	-	dB
Ring Sync Pulse Width		50	-	500	µs
DC PARAMETERS					
Loop Current Programming					
Limit Range		20	-	60	mA
Accuracy		10	-	-	%
Loop Current During Power Denial	R_L = 200Ω	-	±3	±5	mA
Fault Currents					
TIP to Ground		-	30	-	mA
RING to Ground		-	60	-	mA
TIP and RING to Ground		-	90	-	mA
Switch Hook Detection Threshold		-	12	15	mA
Ground Key Detection Threshold		-	10	-	mA
Thermal $\overline{ALARM}$ Output	Safe Operating Die Temperature Exceeded	140	-	160	^oC
Ring Trip Detection Threshold	$V_{RING} = 105V_{RMS}$, f_{RING} = 20Hz	-	10	-	mA
Ring Trip Detection Period		-	100	150	ms
Dial Pulse Distortion		-	0.1	0.5	ms
Relay Driver Outputs					
On Voltage V_{OL}	I_{OL} ($\overline{PR}$) = 60mA, I_{OL} ($\overline{RD}$) = 30mA	-	0.2	0.5	V
Off Leakage Current	V_{OH} = 13.2V	-	±10	±100	µA
TTL/CMOS Logic Inputs (F0, F1, RS, TEST, PRI)					
Logic '0' V_{IL}		-	-	0.8	V
Logic '1' V_{IH}		2.0	-	5.5	V
Input Current (F0, F1, RS, $\overline{TEST}$, PRI)	$0V \le V_{IN} \le 5V$	-	-	±100	µA

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Logic Outputs					
Logic '0' V_{OL}	I_{LOAD} = 800µA	-	0.1	0.5	V
Logic '1' V_{OH}	I_{LOAD} = 40µA	2.7	-	-	V
Power Dissipation On Hook	Relay Drivers Off	-	200	-	mW
I_B+	V_{B+} = 5.25V, V_{B-} = -58V, R_{LOOP} = ∞	-	-	6	mA
I_B-	V_{B+} = 5.25V, V_B- = -58V, R_{LOOP} = ∞	-6	-	-	mA
UNCOMMITTED OP AMP PARAMETERS					
Input Offset Voltage		-	±5	-	mV
Input Offset Current		-	±10	-	nA
Differential Input Resistance	(Note 4)	-	1	-	MΩ
Output Voltage Swing	R_L = 10kΩ	-	±3	-	V_{P-P}
Small Signal GBW	(Note 4)	-	1	-	MHz

NOTE:

4. These parameters are controlled by design or process parameters and are not directly tested. These parameters are characterized upon initial design release, upon design changes which would affect these characteristics, and at intervals to assure product quality and specification compliance.

Pin Descriptions

SOIC	SYMBOL	DESCRIPTION
1	AG (Note 5)	Analog Ground - To be connected to zero potential. Serves as a reference for the transmit output and receive input terminals.
2	V_B+	Positive Voltage Source - most positive supply.
3	C_1	Capacitor #C_1 - An external capacitor to be connected between this terminal and analog ground. Required for proper operation of the loop current limiting function.
4	F1	Function Address #1 - A TTL and CMOS compatible input used with F0 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table. F1 should be toggled high after power is applied.
5	F0	Function Address #0 - A TTL and CMOS compatible input used with F1 function address line to externally select logic functions. The three selectable functions are mutually exclusive. See Truth Table.
6	RS	Ring Synchronization Input - A TTL - compatible clock input. The clock is arranged such that a positive pulse (50µs - 500µs) occurs on the zero crossing of the ring voltage source, as it appears at the RFS terminal. For Tip side injected systems, the RS pulse should occur on the negative going zero crossing and for Ring injected systems, on the positive going zero crossing. This ensures that the ring delay activates and deactivates when the instantaneous ring voltage is near zero. If synchronization is not required, the pin should be tied to 5.
7	$\overline{SHD}$	Switch Hook Detection - An active low LS, TTL-compatible logic output. A line supervisory output.
8	$\overline{GKD}$	Ground Key Detection - An active low LS, TTL-compatible logic output. A line supervisory output.
9	$\overline{TST}$	A TTL logic input. A low on this pin will set a latch and keep the SLIC in a power down mode until the proper F1, F0 state is set and will keep $\overline{ALM}$ low. See Truth Table.
10	$\overline{ALM}$	An LS TTL-compatible active low output which responds to the thermal detector circuit when a safe operating die temperature has been exceeded. When $\overline{TST}$ is forced low by an external control signal, $\overline{ALM}$ is latched low until the proper F1, F0 state and $\overline{TST}$ input is brought high. The $\overline{ALM}$ can be tied directly to the $\overline{TST}$ pin to power down the part when a thermal fault is detected and then reset with F0, F1. See Truth Table. It is possible to ignore transient thermal overload conditions in the SLIC by delaying the response to the $\overline{TST}$ pin from the $\overline{ALM}$. Care must be exercised in attempting this as continued thermal overstress may reduced component life.
11	I_{LMT}	Loop Current Limit - Voltage on this pin sets the short loop current limiting conditions using a resistive voltage divider.
12	OUT1	The analog output of the spare operational amplifier.
13	-IN1	The inverting analog input of the spare operational amplifier.

Pin Descriptions (Continued)

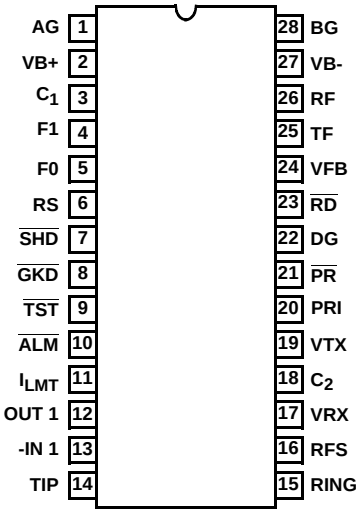
SOIC	SYMBOL	DESCRIPTION
14	TIP	An analog input connected to the TIP (more positive) side of the subscriber loop through a feed resistor and ring relay contact. Functions with the RING terminal to receive voice signals from the telephone and for loop monitoring purpose.
15	RING	An analog input connected to the RING (more negative) side of the subscriber loop through a feed resistor. Functions with the TIP terminal to receive voice signals from the telephone and for loop monitoring purposes.
16	RFS	Ring Feed Sense - Senses RING side of the loop for Ground Key Detection. During Ring injected ringing the ring signal at this node is isolated from RF via the ring relay. For Tip injected ringing, the RF and RFS pins must be shorted.
17	V_{RX}	Receive Input, 4-Wire Side - A high impedance analog input. AC signals appearing at this input drive the Tip Feed and Ring Feed amplifiers differentially.
18	C_2	Capacitor #C_2 - An external capacitor to be connected between this terminal and ground. It prevents false ring trip detection from occurring when longitudinal currents are induced onto the subscriber loop from power lines and other noise sources. This capacitor should be nonpolarized.
19	V_{TX}	Transmit Output, 4-Wire Side - A low impedance analog output which represents the differential voltage across TIP and RING. Transhybrid balancing must be performed beyond this output to completely implement 2-Wire to 4-Wire conversion. This output is referenced to analog ground. Since the DC level of this output varies with loop current, capacitive coupling to the next stage is necessary.
20	PRI	A TTL compatible input used to control $\overline{PR}$. PRI active High = $\overline{PR}$ active low.
21	$\overline{PR}$	An active low open collector output. Can be used to drive a Polarity Reversal Relay.
22	DG (Note 5)	Digital Ground - To be connected to zero potential. Serves as a reference for all digital inputs and outputs on the SLIC.
23	$\overline{RD}$	Ring Relay Driver - An active low open collector output. Used to drive a relay that switches ringing signals onto the 2-Wire line.
24	V_{FB}	Feedback input to the tip feed amplifier; may be used in conjunction with transmit output signal and the spare op amp to accommodate 2-Wire line impedance matching.
25	TF	Tip Feed - A low impedance analog output connected to the TIP terminal through a feed resistor.
26	RF	Ring Feed - A low impedance analog output connected to the RING terminal through a feed resistor.
27	V_B-	The battery voltage source. The most negative supply.
28	BG (Note 5)	Battery Ground - To be connected to zero potential. All loop current and some quiescent current flows into this ground terminal.

NOTE:

5. All grounds (AG, BG, and DG) must be applied before V_B+ or V_B-. Failure to do so may result in premature failure of the part. If a user wishes to run separate grounds off a line card, the AG must be applied first.

Pinout

HC-5509B (SOIC)
TOP VIEW

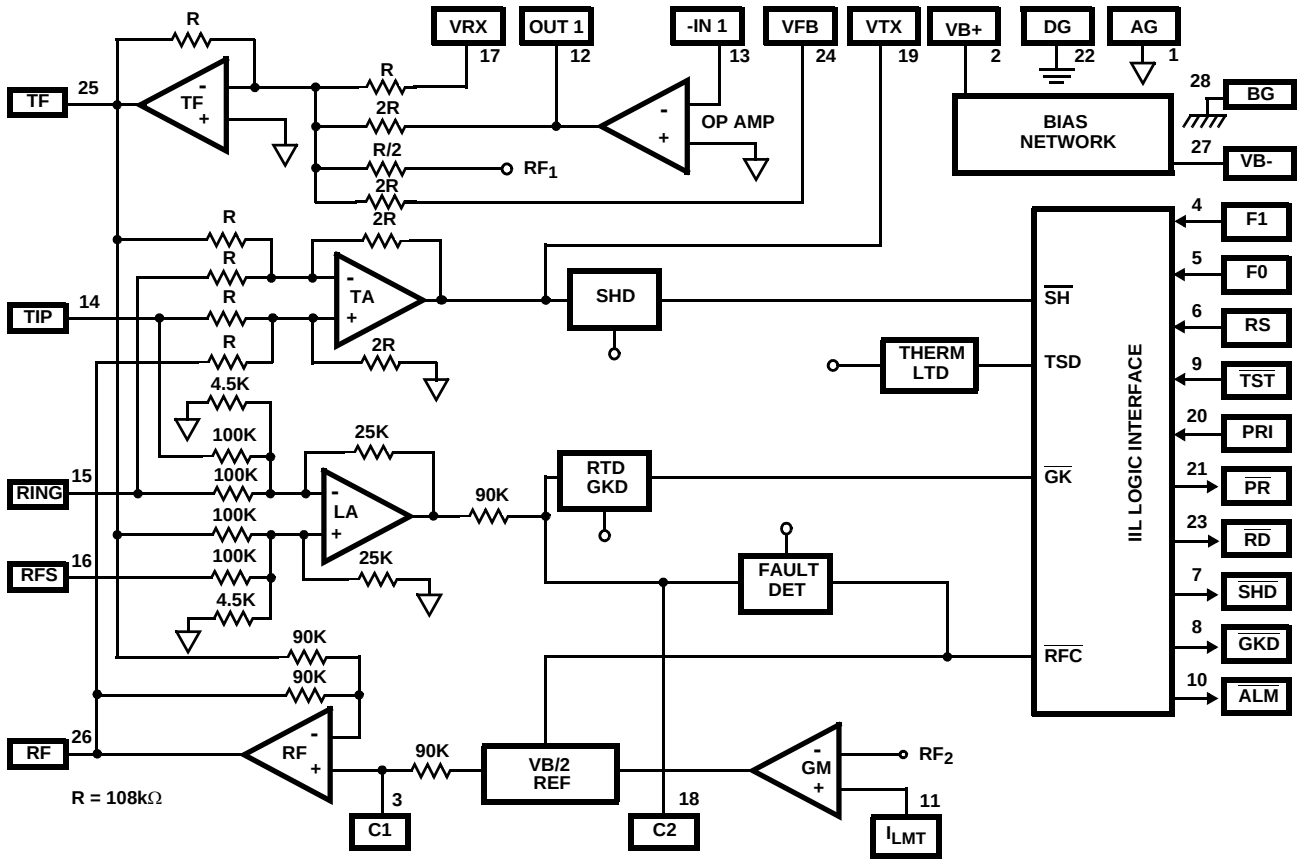


TRUTH TABLE

F1	F0	ACTION
0	0	Normal Loop Feed
0	1	$\overline{RD}$ Active (Ringing)
1	0	Power Down Latch RESET
1	0	Power On RESET
1	1	Loop Power Denial Active

Functional Diagram

SOIC



Overvoltage Protection and Longitudinal Current Protection

The SLIC device, in conjunction with an external protection bridge, will withstand high voltage lightning surges and power line crosses.

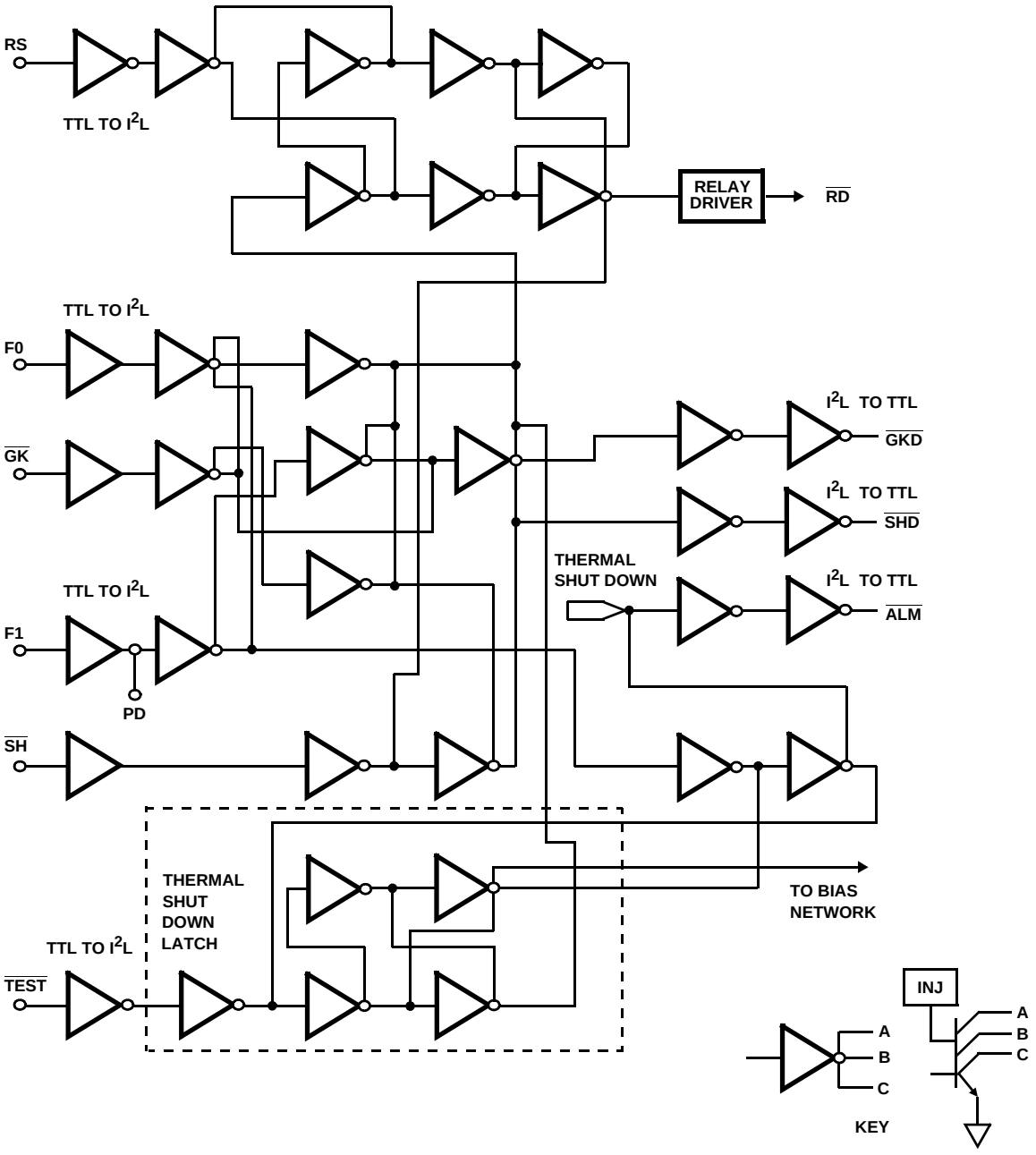
High voltage surge conditions are as specified in Table 1.

The SLIC will withstand longitudinal currents up to a maximum or $30mA_{RMS}$, $15mA_{RMS}$ per leg, without any performance degradation.

TABLE 1.

PARAMETER	TEST CONDITION	PERFORMANCE (MAX)	UNITS
Longitudinal Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
Metallic Surge	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
T/GND, R/GND	10µs Rise/ 1000µs Fall	±1000 (Plastic)	V_{PEAK}
50/60Hz Current T/GND, R/GND	11 Cycles, Limited to $10A_{RMS}$	700 (Plastic)	V_{RMS}

Logic Diagram



Typical Applications

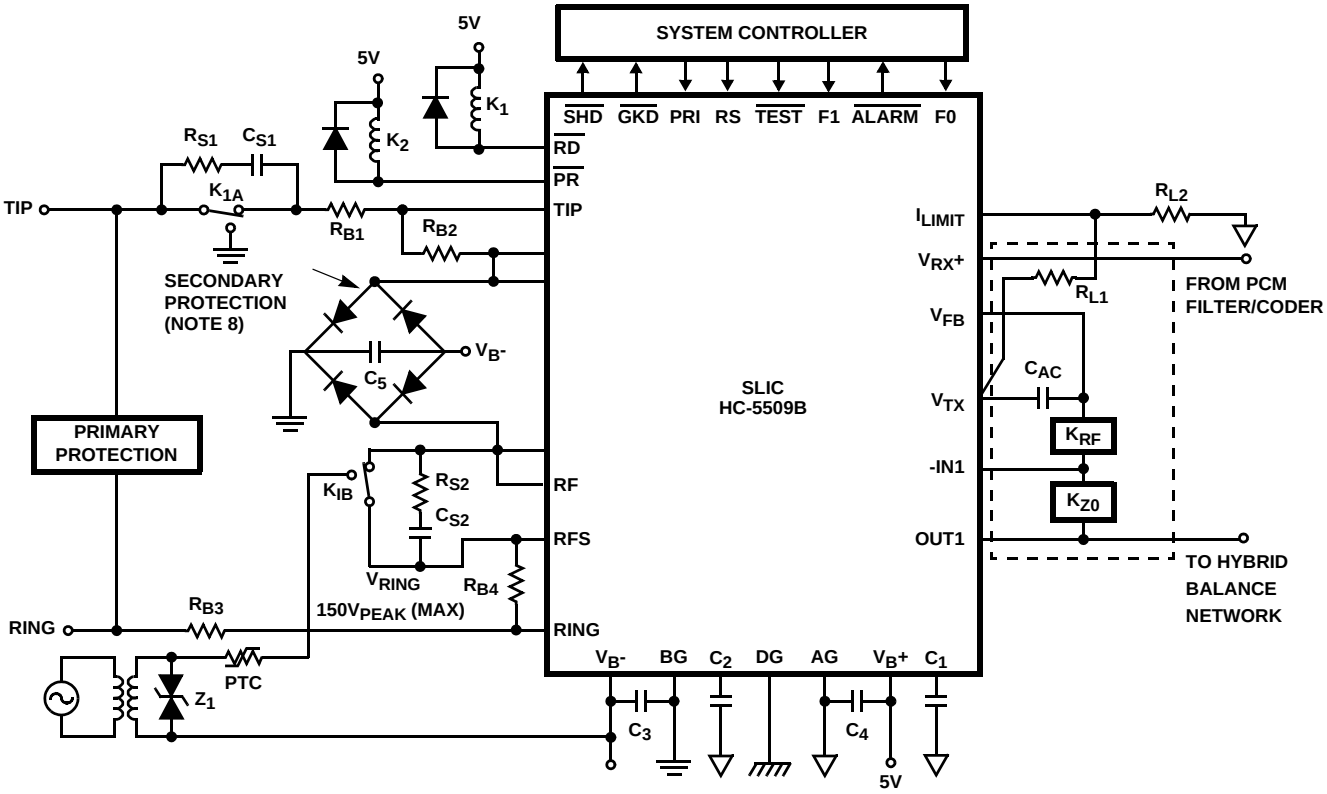


FIGURE 1. TYPICAL LINE CIRCUIT APPLICATION WITH THE MONOLITHIC SLIC

Typical Component Values

C_1 = 0.5µF, 30V.

C_2 = 1.0µF ±10%, 20V (for other values of C_2, refer to AN9667).

C_3 = 0.01µF, 100V, ±20%.

C_4 = 0.01µF, 100V, ±20%.

C_5 = 0.01µF, 100V, ±20%.

C_{AC} = 0.5µF, 20V.

KZ_0 = 60kΩ, (Z_0 = 600Ω, K = Scaling Factor = 100).

R_{L1}, R_{L2}; Current Limit Setting Resistors:

$R_{L1} + R_{L2} > 90k\Omega \rightarrow$ offset.

$I_{LIMIT} = (0.6)\ (R_{L1} + R_{L2})/(200 \times R_{L2})$, R_{L1} typically 100kΩ.

K_{RF} = 20kΩ, RF = 2(R_{B2} + R_{B4}), K = Scaling Factor = 100).

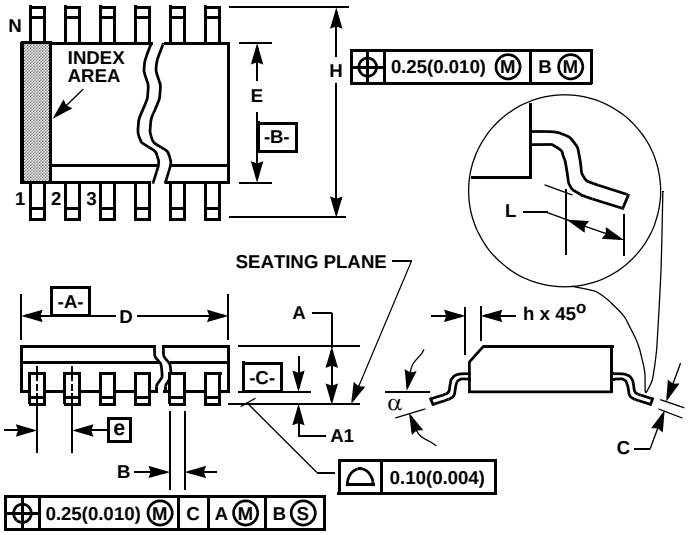
$R_{B1} = R_{B2} = R_{B3} = R_{B4}$ = 50Ω (1% absolute, matching requirements covered in a Tech Brief).

$R_{S1} = R_{S2}$ = 1kΩ, typically.

$C_{S1} = C_{S2}$ = 0.1µF, 200V typically, depending on V_{Ring} and line length.

Z_1 = 150V to 200V transient protector. PTC used as ring generator ballast.

Small Outline Plastic Packages (SOIC)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.