

MOS FIELD EFFECT TRANSISTORS 2SK2365/2SK2366

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK2365, 2SK2365-Z/2SK2366, 2SK2366-Z is N-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

· Low On-Resistance

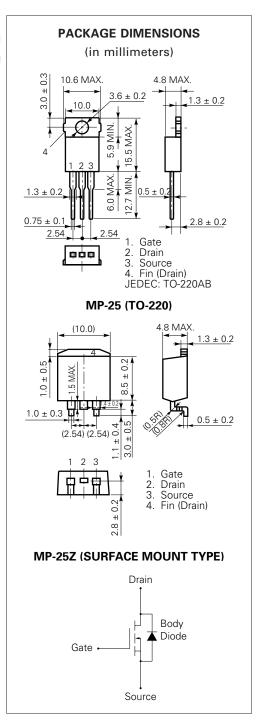
2SK2365: $R_{DS(on)} = 0.5 \Omega$ (Vgs = 10 V, ID = 5.0 A) 2SK2366: $R_{DS(on)} = 0.6 \Omega$ (Vgs = 10 V, ID = 5.0 A)

- Low Ciss Ciss = 1 600 pF TYP.
- High Avalanche Capability Ratings
- · Isolate TO-220 Package

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage (2SK2365/2SK2366)	VDSS	450/500	V
Gate to Source Voltage	Vgss	±30	V
Drain Current (DC)	ID(DC)	±10	Α
Drain Current (pulse)*	ID(pulse)	±40	Α
Total Power Dissipation ($T_c = 25$ °C)	P _{T1}	75	W
Total Power Dissipation (TA = 25 °C)	P_{T2}	1.5	W
Channel Temperature	T_ch	150	°C
Storage Temperature	T _{stg}	–55 to +150	°C
Single Avalanche Current**	las	10	Α
Single Avalanche Energy**	Eas	143	mJ

- * PW \leq 10 μ s, Duty Cycle \leq 1 %
- ** Starting T_{ch} = 25 °C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0



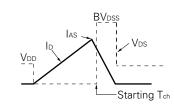


ELECTRICAL CHARACTERISTICS (TA = 25 °C)

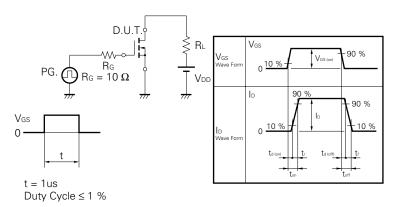
CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS	
Drain to Source On-State Resistance	R _{DS(on)}		0.4	0.5	Ω	Vgs = 10 V	2SK2365
			0.5	0.6		ID = 5.0 A	2SK2366
Gate to Source Cutoff Voltage	V _{GS(off)}	2.5		3.5	V	V _{DS} = 10 V, I _D = 1 mA	
Forward Transfer Admittance	l yfs l	4.0			S	V _{DS} = 10 V, I _D = 5.0 A	
Drain Leakage Current	IDSS			100	μΑ	V _{DS} = V _{DSS} , V _{GS} = 0	
Gate to Source Leakage Current	Igss			±100	nA	Vgs = ±30 V, Vps = 0	
Input Capacitance	Ciss		1 600		pF	V _{DS} = 10 V	
Output Capacitance	Coss		310		pF	V _G S = 0	
Reverse Transfer Capacitance	Crss		30		pF	f = 1 MHz	
Turn-On Delay Time	td(on)		30		ns	ID = 5.0 A	
Rise Time	tr		20		ns	V _G S = 10 V	
Turn-Off Delay Time	td(off)		80		ns	V _{DD} = 150 V	
Fall Time	tf		20		ns	$R_G = 10 \Omega R_L$	= 30 Ω
Total Gate Charge	Qg		42		nC	ID = 10 A	
Gate to Source Charge	Qgs		10		nC	V _{DD} = 400 V	
Gate to Drain Charge	Q _{GD}		20		nC	V _{GS} = 10 V	
Body Diode Forward Voltage	V _{F(S-D)}		1.0		V	IF = 10 A, VGS	= 0
Reverse Recovery Time	trr		350		ns	IF = 10 A, VGS	= 0
Reverse Recovery Charge	Qrr		1.5		μC	$di/dt = 50 A/\mu s$	

Test Circuit 1 Avalanche Capability

$\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \Omega \\ \text{V} \\ \text{Ves} = 20 - 0 \text{ V} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{S} \\ \text{S} \\ \text{O} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{No.} \\ \text{No.} \end{array}$



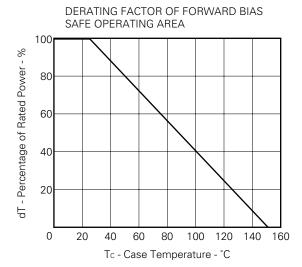
Test Circuit 2 Switching Time



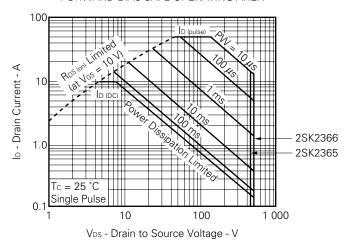
Test Circuit 3 Gate Charge

The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

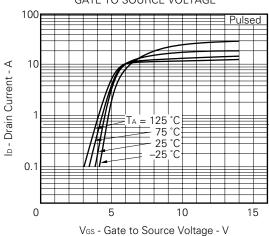
TYPICAL CHARACTERISTICS (TA = 25 °C)

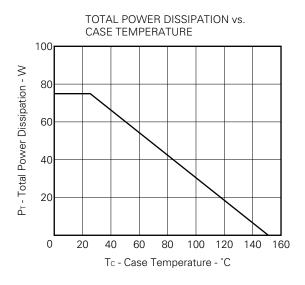


FORWARD BIAS SAFE OPERATING AREA

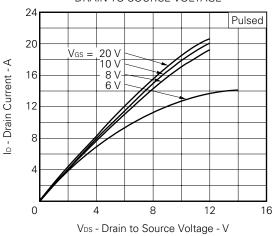


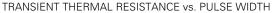
DRAIN CURRENT vs. GATE TO SOURCE VOLTAGE

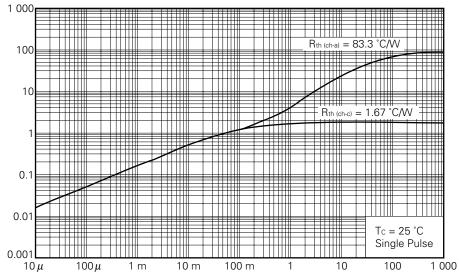




DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

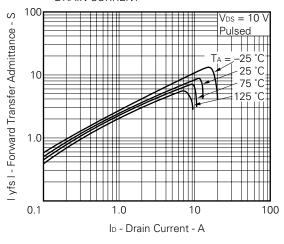




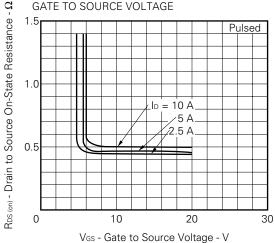


PW - Pulse Width - s

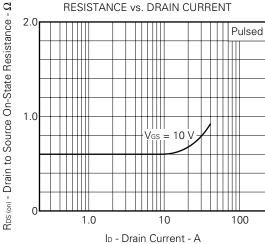
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



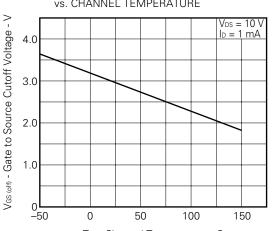
DRAIN TO SOURCE ON-STATE RESISTANCE vs.



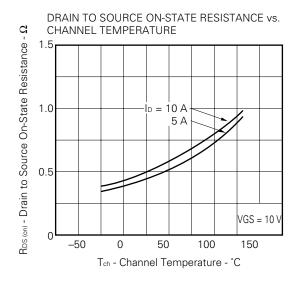
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

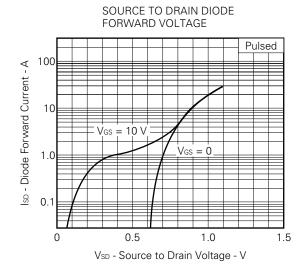


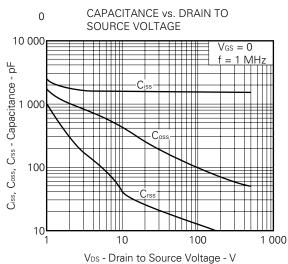
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

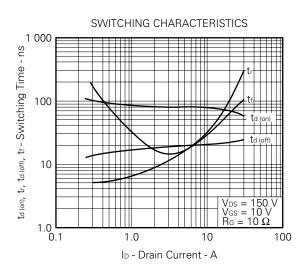


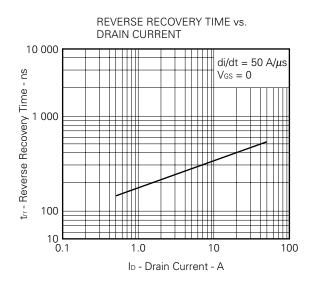
T_{ch} - Channel Temperature - C

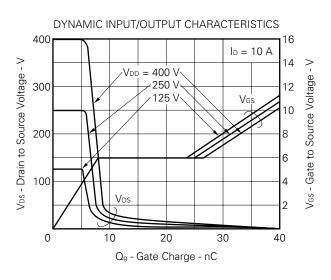


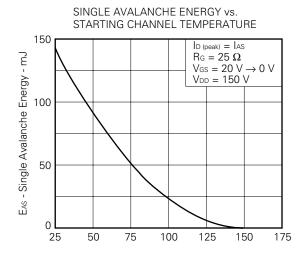


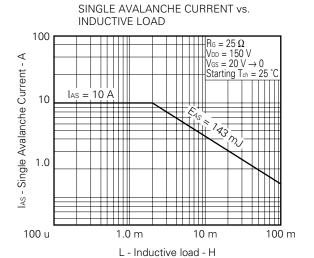












REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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Anti-radioactive design is not implemented in this product.